January 1994
Edition 1.0

FUJITSU

DATA SHEET

MB8316200B

CMOS 16M-BIT MASK READ ONLY MEMORY

1M x 16 (2M x 8) CMOS MASK READ ONLY MEMORY

The Fujitsu MB8316200B is a CMOS Si-gate mask-programmable static read only memory organized as 1,048,576 words by 16 bits or 2,097,152 words by 8 bits.

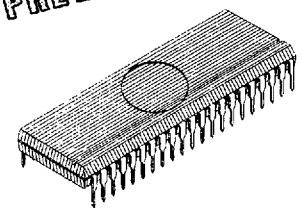
The MB8316200B has TTL-compatible I/O 3-state output level with fully-staticoperation (i.e. no need of clock signal) with single +5V power supply.

Also, the MB8316200B is designed for applications such as character generator and program storage which require large memory capacity and high-speed/low-power operation.

The memory organization of MB8316200B is configurable between 16 bits and 8 bits by User. (ex. The system using 8 bits CPU and 16 bits CPU can use common data on the same chip.)

- Organization: 1,048,576 words x 16 bits
  2,097,152 words x 8 bits
- Access time: 150ns max.
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three-state output
- Single +5V power supply
- Power dissipation: 385mW max. (Active)
  5.5mW max. (Standby, TTL input level)
  0.055mW max. (Standby, CMOS input level)
- Standard 42-pin Plastic DIP: Suffix: P
- 44-pin bend-type(Gull-wing) Plastic SOP: Suffix: PF
- 48-pin Plastic bend-type(Gull-wing) TSOP:
  Suffix: PFTN(Normal Bend)
  Suffix: PFTR(Reversed Bend)

PRELIMINARY



PLASTIC PACKAGE
DIP-42P-M01

FPT-44P-M05 See Page 7-44, 7-45
FPT-48P-M07 See Page 7-46, 7-47
FPT-48P-M08 See Page 7-48, 7-49

PIN ASSIGNMENT

(TOP VIEW)

A_{18}	1	42	A_{19}
A_{17}	2	41	A_8
A_7	3	40	A_9
A_6	4	39	A_{10}
A_5	5	38	A_{11}
A_4	6	37	A_{12}
A_3	7	36	A_{13}
A_2	8	35	A_{14}
A_1	9	34	A_{15}
A_0	10	33	A_{16}
$\overline{CE}$	11	32	$\overline{BYTE}$
*1 V_{SS}	12	31	V_{SS} *1
$\overline{OE}$	13	30	$(A_{-1})/O_{16}$
O_1	14	29	O_8
* O_9	15	28	O_{15} *
O_2	16	27	O_7
* O_{10}	17	26	O_{14} *
O_3	18	25	O_6
* O_{11}	19	24	O_{13} *
O_4	20	23	O_5
* O_{12}	21	22	V_{CC}

This pin (*) is High-Z, the device is used 8 bits.

*1: All pins should be connected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

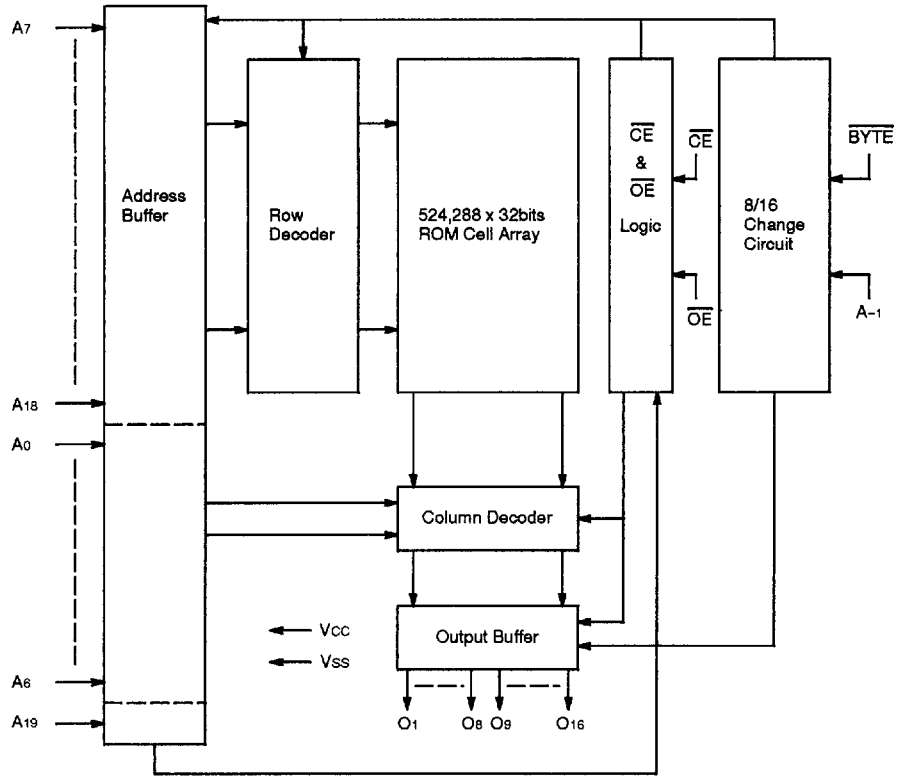
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0 *	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5 *	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5 *	V
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

*** Referenced to GND**

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB8316200B BLOCK DIAGRAM



OUTPUT MODE SELECTION A-1 is LSB.

BYTE	O1 to O8	O9 to O15	(A-1)/O16
H	O1 to O8	O9 to O15	O16
L	O1 to O8	High-Z	A-1 ("L" INPUT)
L	O9 to O16	High-Z	A-1 ("H" INPUT)

TRUTH TABLE

CE	OE	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	NOT SELECTED	High-Z	STANDBY
L	H	NOT SELECTED	High-Z	ACTIVE
L	L	SELECTED	DOUT	ACTIVE

CAPACITANCE (TA=25° C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (VOUT=0V)	COUT			15	pF
Input Capacitance (VIN=0V)	CIN			15	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}$=V_{IL}, Minimum Cycle	I_{CC}			70	mA
Standby Supply Current	$\overline{CE}$=V_{IH}	I_{SB1}			1	mA
	$\overline{CE}$=V_{CC}=V_{IH}, V_{IN}=V_{SS} or V_{CC}	I_{SB2}			10	µA
Input Leakage Current	V_{IN}=0 to V_{CC}	I_{LI}	-10		10	µA
Output Leakage Current	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IH}	$I_{LI/O}$	-10		10	µA
Output High Voltage	I_{OH}=-400µA	V_{OH}	2.4			V
Output Low Voltage	I_{OL}=2.1mA	V_{OL}			0.4	V

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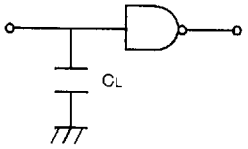
AC TEST CONDITIONS

Fig.2 — AC TEST CONDITIONS

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : t_T=5ns
- Timing Reference Levels : Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V
- Output Load : 1 TTL Gate and 100pF



AC CHARACTERISTICS

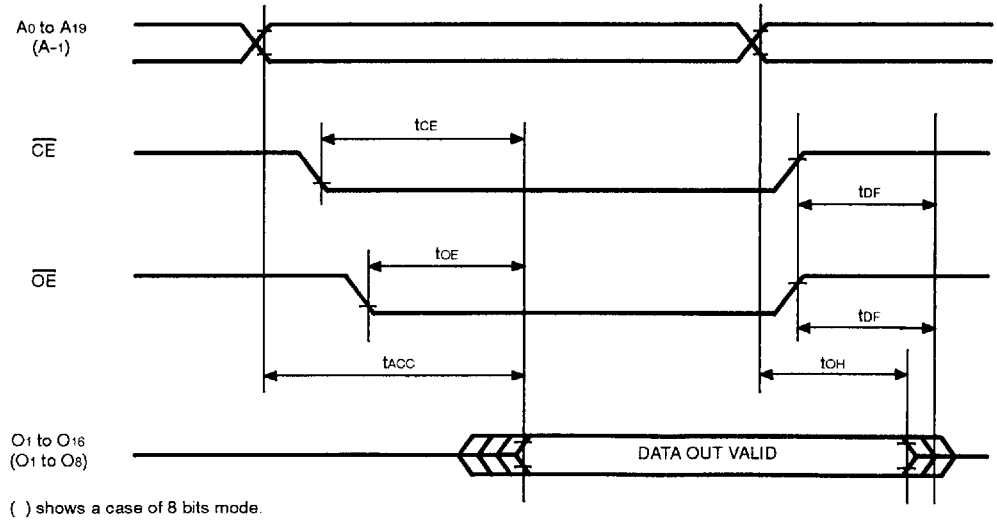
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	t_{ACC}		150	ns
Chip Enable Access Time	$\overline{OE}$=V_{IL}	t_{CE}		150	ns
Output Enable Access Time	Note 1	t_{OE}		70	ns
Output Disable Time	Note 2	t_{DF}		50	ns
Output Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	t_{OH}	0		ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{ACC} is $t_{ACC} - t_{OE}$.

Note 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to High earlier.

TIMING DIAGRAM

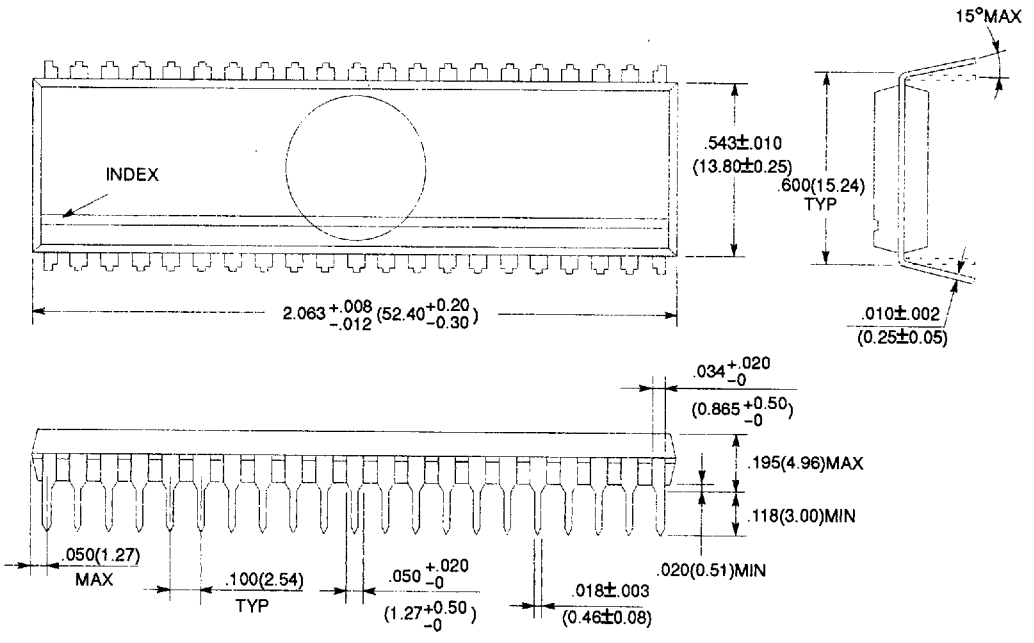


( ) shows a case of 8 bits mode.

PACKAGE DIMENSIONS

(Suffix: P)

42-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42P-M01)



Dimensions in
inches (millimeters)

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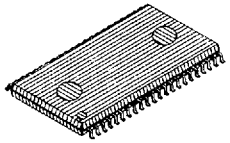
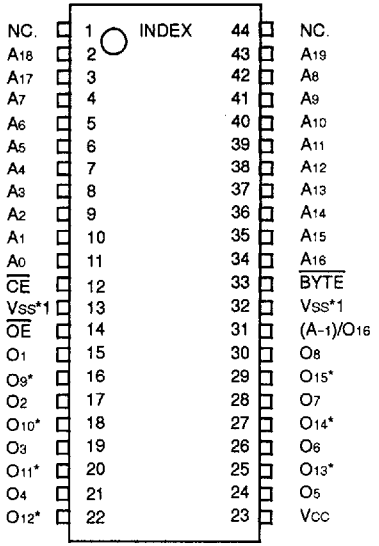
PACKAGE DIMENSIONS (Continued)

(Suffix: PF)



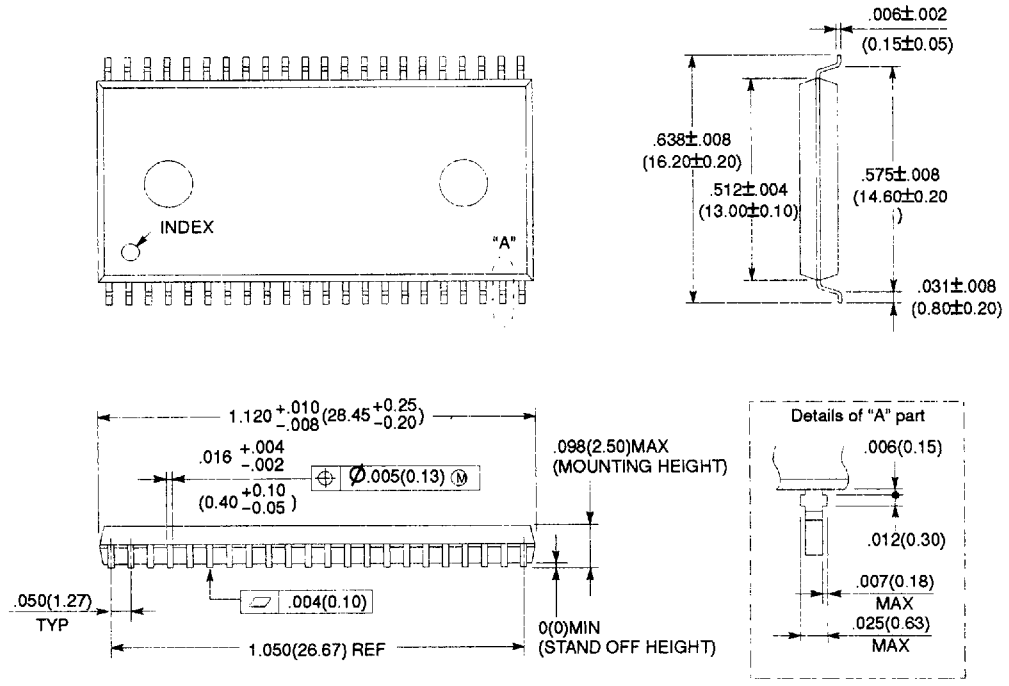
PLASTIC PACKAGE
FPT-44P-M05

PIN ASSIGNMENT



This pin (*) is High-Z, the device is used 8 bits.
*1: All pins should be connected.

44-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-44P-M05)



Dimensions in
inches (millimeters)

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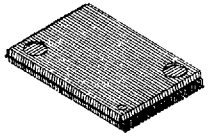
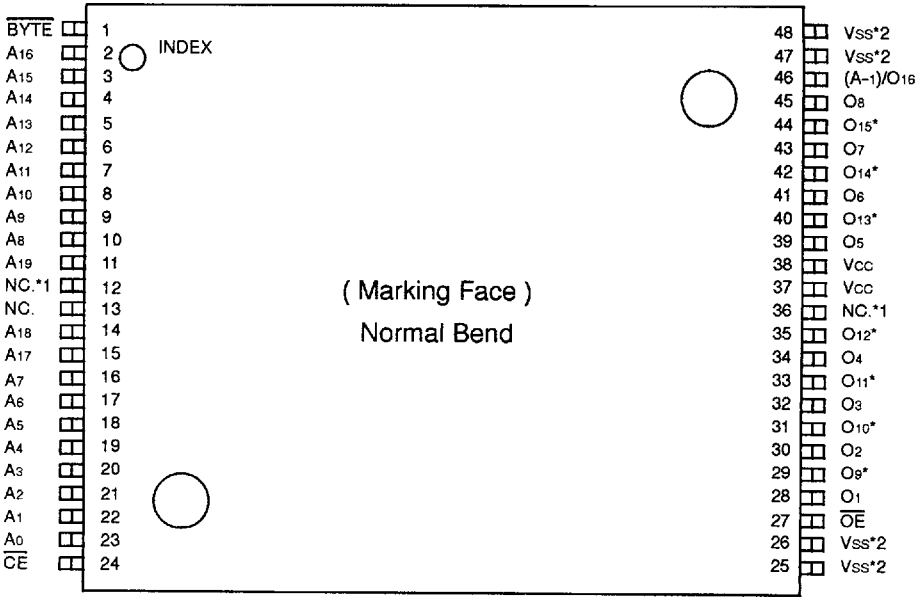
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)



PLASTIC PACKAGE
FPT-48P-M07

PIN ASSIGNMENT



This pin (*) is High-Z, the device is used 8 bits.
*1: If the voltage is applied externally, it should be connected to VSS.
*2: All pins should be connected.

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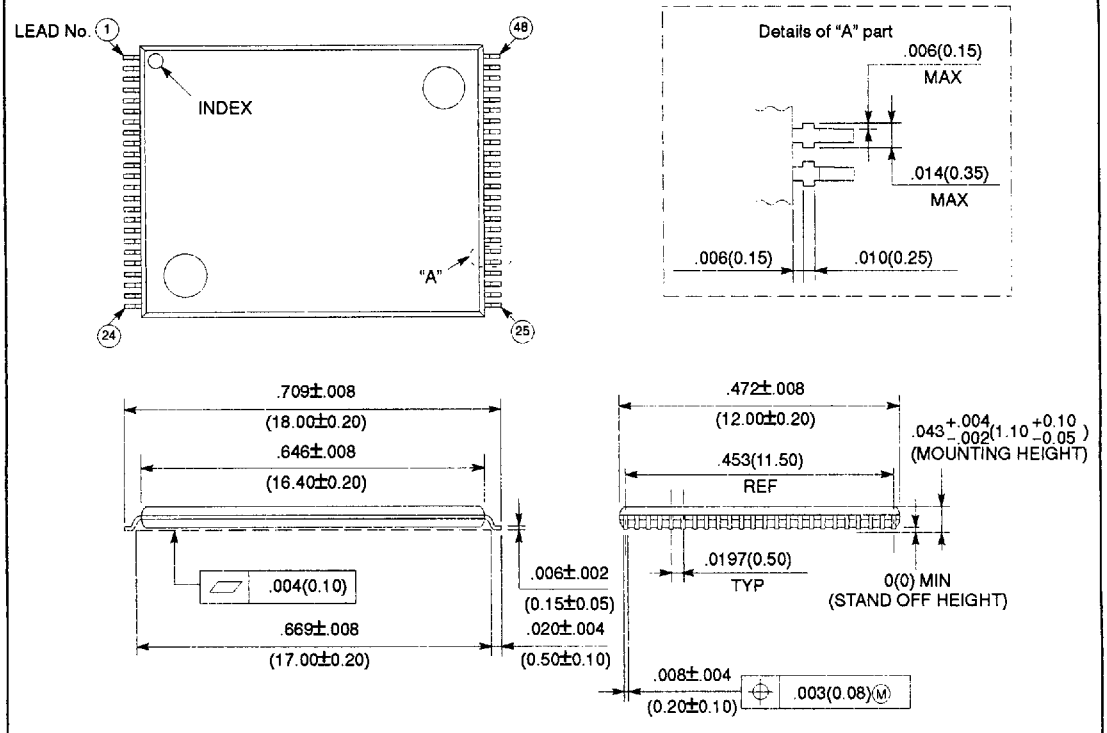
48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M07)

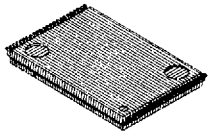


Dimensions in
inches (millimeters)

7

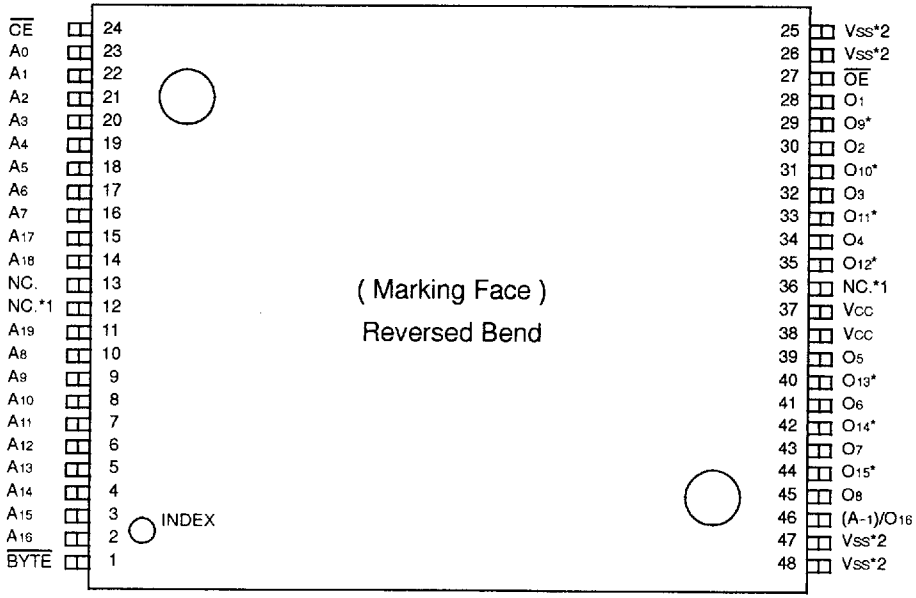
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



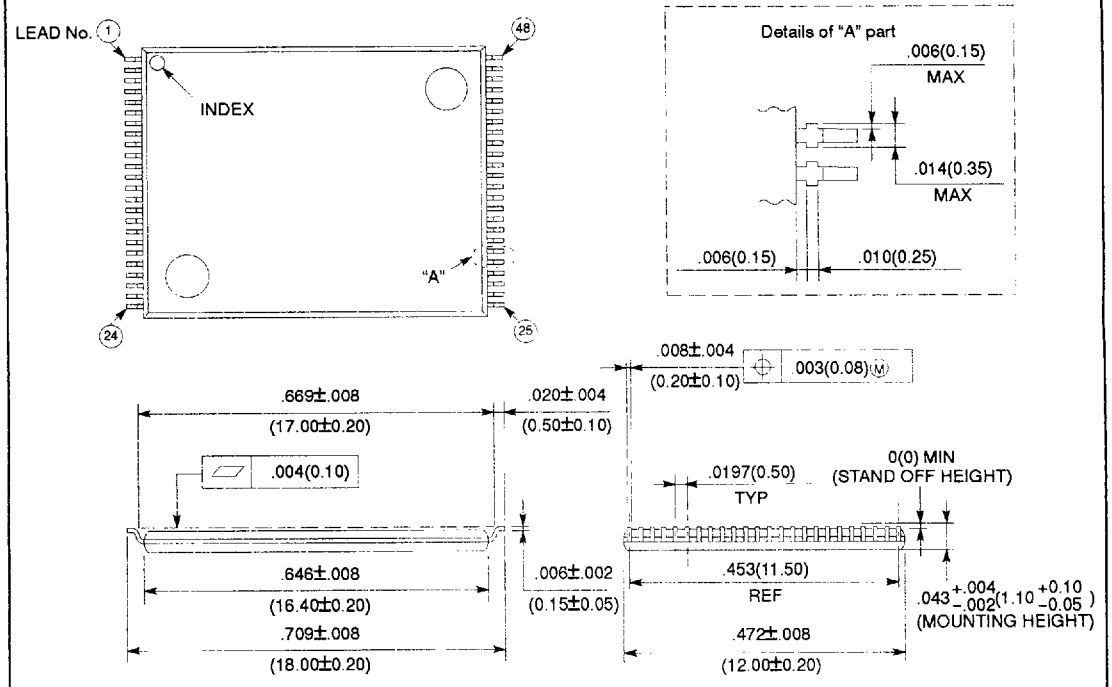
PLASTIC PACKAGE
FPT-48P-M08

PIN ASSIGNMENT



This pin (*) is High-Z, the device is used 8 bits.
*1: If the voltage is applied externally, it should be connected to Vss.
*2: All pins should be connected

48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M08)



Dimensions in
inches (millimeters)

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