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CIRCLE 2

UP FRONT

Agreement on standards for 5¼″ Winchesters

Xebec and Priam, respectively manufacturers of disk drive controllers and Winchester disk drives, have reached a mutual agreement to promote the adoption of an interface standard for the next generation of high performance, high capacity 5¼″ Winchester disk drives. Originally developed for 8″ Winchesters, the BSR X3.101 standard has been accepted by the International Standards Organization and the American National Standards Institute (ANSI). Company representatives claim that the interface is supported by numerous 8″ Winchester makers and disk drive controller companies. Semiconductor firms are already shipping ANSI-compatible ICs that will ease implementation of drives into existing systems.

A 32-bit Multibus standard under development

Intel has joined 12 other companies in developing specifications for a new microprocessor data bus, Multibus® II, to meet the needs of 8-, 16-, and 32-bit microprocessor systems. The participating companies include Advanced Micro Devices, Compagnie des Machines Bull, Dataindustrier AB, Hewlett-Packard, International Computer Ltd, Intersil Systems, Matra, Mupac, Nixdorf Computer, Siemens AG, Tektronix, and Zilog. Many of these companies will develop products based on the new bus, and Intel expects to publish Multibus II specifications in the second half of this year. Multibus II will provide an upgrade path for current Multibus users and vendors, so that existing Multibus board-level products can operate in Multibus II environments.

Protocol enables dissimilar microcomputers to share data

The first data communication protocol to allow file transfer to and from a variety of microcomputers over ordinary voice-grade telephone lines, the Microcom Networking Protocol (MNP) is said to accommodate realtime interactive communications as well as provide the industry's first standard file transfer protocol. Microcom, Inc (Norwood, Mass) claims that MNP can be used on any existing microcomputer system and is flexible enough to take advantage of the higher performance capabilities of new machines and future design advances. According to the company, MNP is independent of any microprocessor, personal computer, or operating system. It can be utilized over a range of physical connections, asynchronous or synchronous, at a range of speeds, on leased lines or dial-up, or in local area networks. The protocol also allows the implementation of future communication enhancements within its layered architecture.

MNP uses five of the seven protocol layers in the International Standards Organization reference model. Each layer in the model provides services for the layers above it, but the operation of each layer is independent. This enables the protocol at one layer to change without affecting any other layer. The protocol defines the interaction between systems at each layer. Interfaces between the layers can be different for each implementation and are optimized for each system.

In a separate announcement, GTE Telenet Communications said that its Telenet Public Data Network will support direct transmissions between personal computers and host computers, or other systems utilizing MNP. During the protocol's implementation, GTE Telenet collaborated closely with Microcom, assisted with testing, and suggested enhancements to improve the protocol's performance over the Telenet packet-switching network.

UP FRONT

Pretriggers

An entry level microprocessor-based data communications minicomputer from Honeywell offers up to 1M byte of main memory and more than 1G byte of online disk storage. The DPS 6/40 can communicate concurrently with Honeywell or IBM computers in a distributed data processing environment.

A ROM-resident realtime operating system kernel for Z80-based machines used in embedded applications avoids the time and difficulty of creating one from scratch. Produced by Hunter & Ready and endorsed by Zilog, the kernel allows software written in high level languages on 16-bit machines to run on Z80s without significant alterations.

Ability to emulate any of over 60 different RP/ and RM/ disk drive combinations on its four ports is claimed for the Emulex SC31 emulating controller. It also can lower per-byte storage costs by mapping multiple logical disk drives on a high capacity physical drive.

Distributed processor architecture allows the FPS5000 family of array processors from Floating Point Systems to accelerate computations three times faster than its previous generation products. Calculations now occur at a rate of 26M- to almost 62M-flops.

Data transfers to half-inch tape drives at speeds approaching 125 ips are possible with Western Peripherals' Tape Dimension III controller. A separate Unibus frontend processor handles handshaking for TS-11 emulation on DEC computers.

A high performance Pascal compiler fully integrated into the Unix operating system on the MC68000 has been introduced by Oregon Software. An optimizing compiler, Pascal-2 produces smaller, faster code than C, FORTRAN 77, or other Pascals on Unix.

High speed vector graphics in a fully programmable unit that produces 2048 x 1513 pixels of addressable resolution is provided by Hewlett-Packard's 1347A HP-IB directed-beam display. Data can be scrolled horizontally and bidirectionally across the 6″ screen.

Picture resolution 4 to 16 times greater than current low end CAD/CAM systems is claimed for the Telesis Systems Graphics Processor. Operational features included were previously available only on high end systems.

Control of instrumentation systems in factory or laboratory environments is the purpose of the Fluke 1722A instrument controller. Standard operating system software includes system and utility command file capability for automatic startup.

Fully modular in 16-channel increments, the 64-channel 64300 series logic analysis systems for Dolch Logic Instruments includes 48, 25/50-MHz synchronous/asynchronous channels for timing/state analysis.

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BPA ABP

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System technology

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System design

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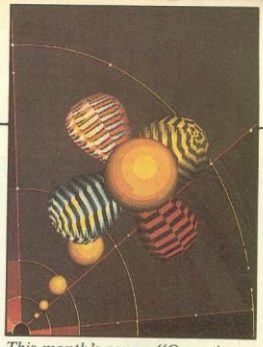
Midcon/83 Mini/Micro-Midwest

Vol 22, No 9
Aug 1983

Special report on microsystems software



This month's cover, "Operating System Core," was created by Mark Lindquist, Alan Green, and Joe Pasquale on the Digital Effects Video Palette III.

System components

Departments

Designers' preference survey*

*Appearing in Domestic issues only

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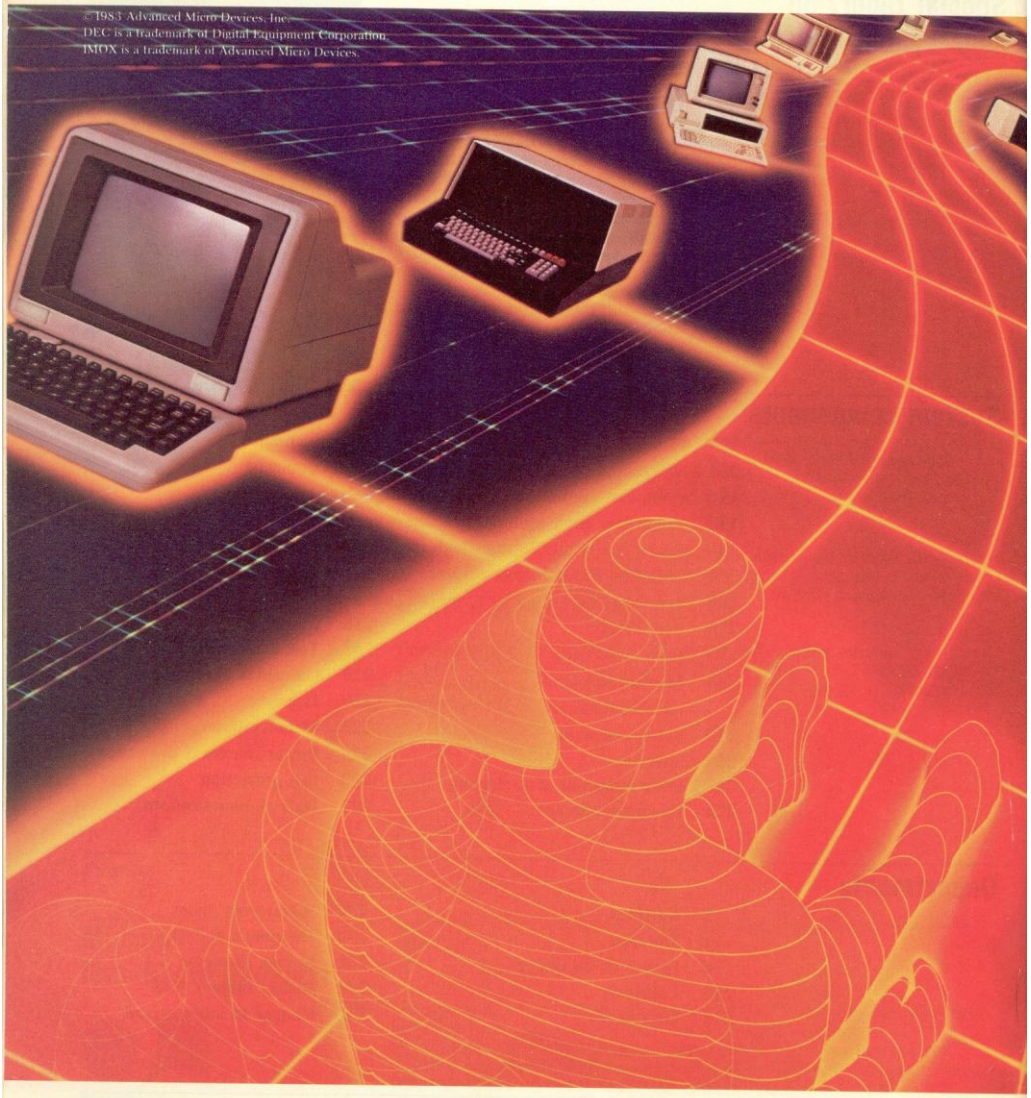
Brian Pollard

GET THE



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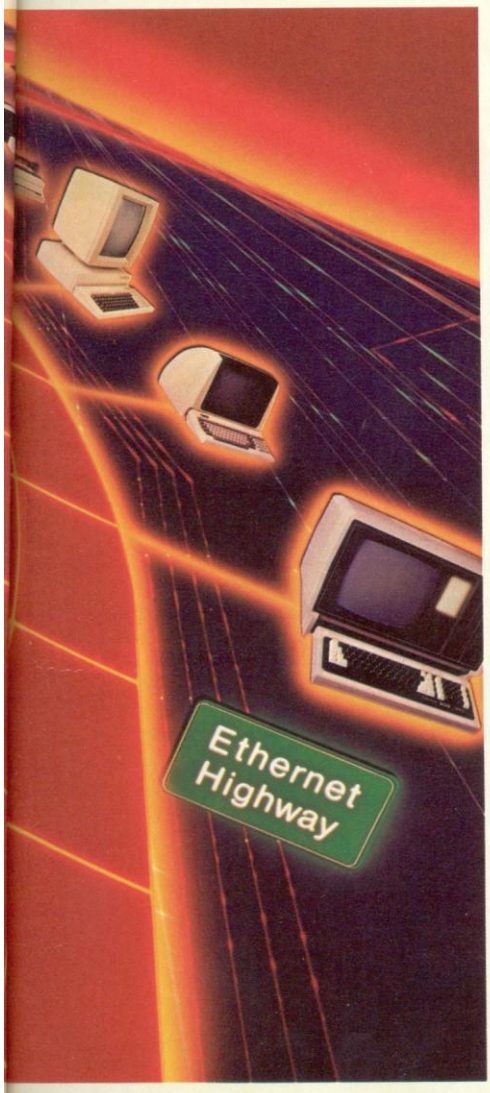

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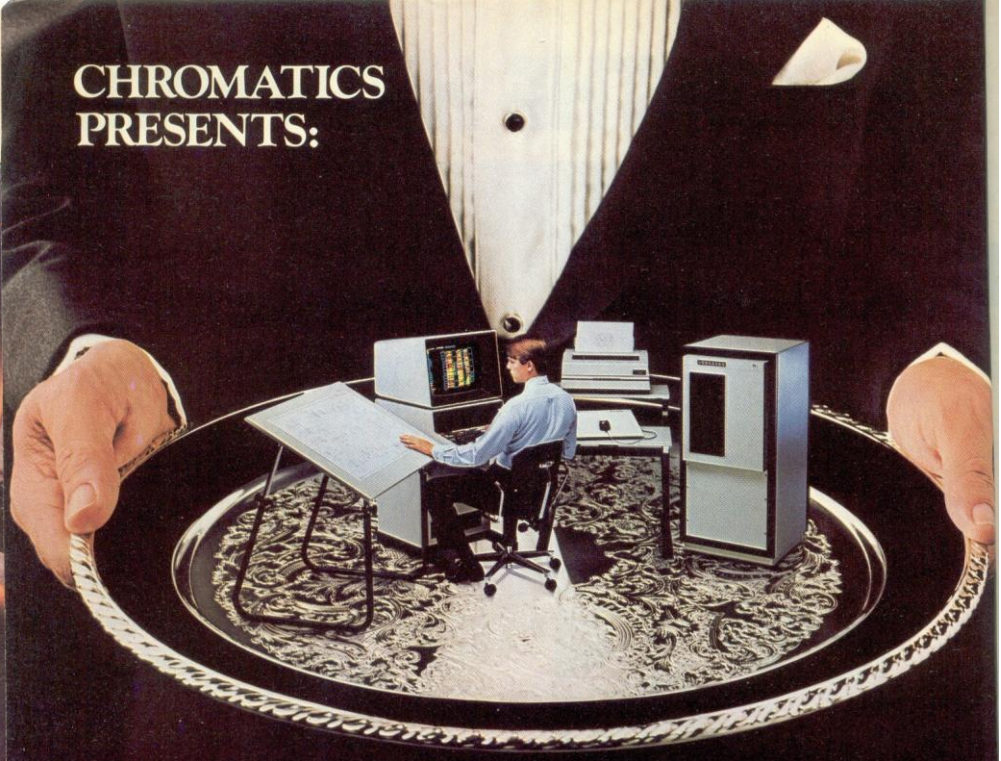

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CIRCLE 6

LESSONS FROM THE RECESSION

In a cyclical industry—which the computer business has become—one can often get a better picture of management performance during lean years than during boom years. When business is good, almost everybody makes money, whereas, in a downturn only the best managed companies gain relative strength. So, now that business is slowly improving, it may prove instructive to look back and see what happened during the latest industry slowdown.

The key to management performance, of course, is asset deployment. The ways in which a company chooses to make expenditures can vitally affect the company's future. For example, reduced advertising may lead to loss of market share, deferred capital investment may lead to inadequate production capacity, and R&D cutbacks may impact the flow of new products. Of these, the area of most vital concern to computer designers is, of course, R&D investment.

Most industry analysts believe that computer companies did a better job of maintaining R&D activity this time compared with earlier recessions. Certainly, the actual dollar expenditures support that observation. One study by Schonfeld & Associates (Evanston, Ill) shows that the computer industry now leads all other U.S. industries in total R&D spending. The Schonfeld study indicates that the annual compound R&D growth rate for electronic computing equipment is running at 13.2%, while that for computer software is even higher at 21.1%. Similar figures emerge from another study by McGraw-Hill (New York, NY), which shows that selected high technology electronics firms increased their R&D expenditures for 1982 by percentages ranging from 16% to 23%.

Analysts also argue that major computer and semiconductor companies employed better strategies this time to control their R&D expenditures. Companies like IBM, Digital Equipment, and Intel avoided the mass layoffs that had characterized earlier recessions. Instead, they employed such techniques as hiring freezes and salary freezes to trim costs. It is argued that by avoiding layoffs, the leading companies were able to retain their highly trained pools of engineering talent. We're not so sure, however.

The problem with salary freezes (and the problem is compounded with salary reductions or an extended workweek for salaried professionals) is that the best engineers tend to vote with their feet and move on to greener pastures, while relatively overpaid engineers remain. Because overall R&D expenditures climbed while many leading companies had frozen their salaries, this suggests that a lot of engineers did, in fact, get raises by job hopping. Of course, companies that also had hiring freezes were doubly handicapped. Not only did they lose good people, they were unable to replace them.

If our analysis is valid—and it is difficult to prove or disprove because changes in the quality (as opposed to quantity) of an R&D investment only become apparent much later—it would suggest that a carefully planned layoff would be preferable to a salary freeze or reduction. But this must be balanced against the shocking effect that layoffs have on employee and investor confidence—especially the sort of unplanned cutbacks still occurring in the video game and home computer segments of our industry. All that can be said, then, is that engineering management may have done a better job this time than in earlier recessions, but it may take a few more business cycles before we really learn to do it right.

Michael Elphick
Editor in Chief

The results are now in for the winner of our 1982 editorial excellence award. It is with great pleasure that we award the Caribbean Windjammer Cruise for two to Lan Nguyen of Zilog, Inc for his article entitled "Expanding the Z80's Memory," which appeared in the Oct 1982 issue.

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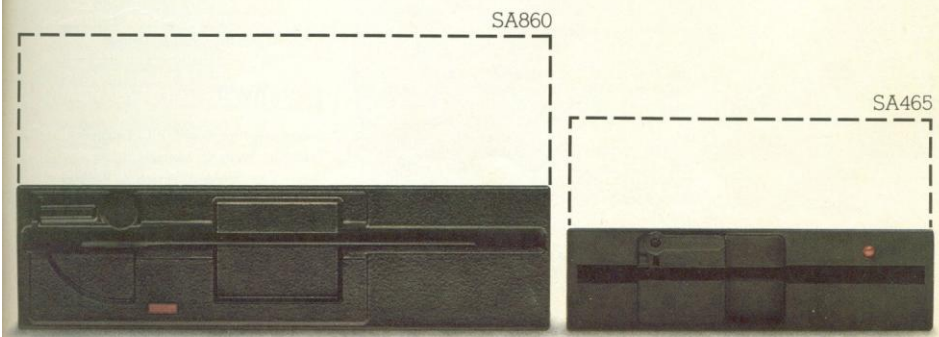

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CIRCLE 9

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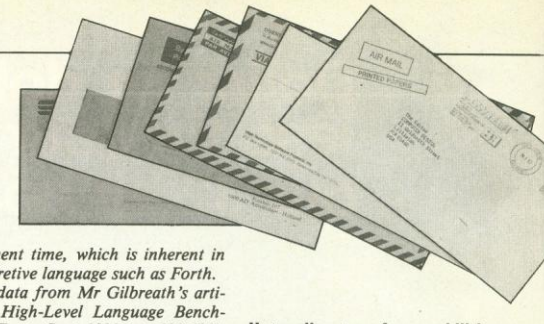
LETTERS TO THE EDITOR



Bringing Forth conclusions

I found some of the conclusions drawn in Bruce Sweet's article, "Adapting Forth to a Multi-User World" (Apr 5, 1983, p 111), difficult to understand. The article explained the movement of a Forth compiler to the Motorola M68000 and the subsequent performance. The accomplishment is impressive; and, compared to other Forth compilers, so is the performance.

However, both the concluding paragraphs and the format of the benchmark tables place the accomplishment in a different context. One of the final paragraphs states, "Forth running on Motorola's M68000 outpaces its competitors." In Table 2, Hemenway/Forth outpaces only Forth compilers. Yet, by grouping Hemenway/Forth with other non-Forth M68000 compilers, the reader is tempted to compare them. This comparison does not favor Forth—the benchmarks in Table 2 show all three M68000 Pascals faster than Hemenway/Forth by at least a factor of two.

Incidentally, my results for 10 iterations of the Sieve of Eratosthenes benchmark, using Oregon Software's Pascal-2 on the Motorola M68000/VERSAdos (8 MHz), was 3.63 s. On the Digital Equipment Corp VAX-11/780, in RSX compatibility mode, the benchmark was 1.32 s. Initially, I agree that "modern Forth is proving to be an efficient development language," but when Pascal is drawn into the comparison, I am quite reluctant to agree.

David Billstrom
Oregon Software
2340 SW Canyon Rd
Portland, OR 97201

Compiler is the key word

Mr Billstrom has brought out a good point in that Pascal compilers running on the M68000 do outpace Hemenway/Forth. But, the key word in this discussion is compiler, not Pascal.

Indeed, all Forths do compile source code, but this compilation results in threaded code, which is interpretive at execution time. In contrast, the Pascal compilers compared in my article all produce native machine code. The fact that Hemenway/Forth can be favorably compared with any compiled language is in itself impressive.

Perhaps the conclusion that Mr Billstrom should have come to is that compiled (native) code executes more quickly than interpretive code. This is a well-documented fact that I will not dispute. In many cases, one is willing to sacrifice execution speed for faster development time, which is inherent in an interpretive language such as Forth.

*Using data from Mr Gilbreath's article, "A High-Level Language Benchmark," (*Byte*, Sept 1981, pp 180-198), we can compare Forth with some other interpretive as well as compiled languages. For instance, BASIC (a popular interpretive language) ran the sieve in 60.0 s when run on an HP 3000. In contrast, the same machine executed a compiled Pascal in 20.0 s. The following comparison carries an even more startling result:*

Microsoft Compiled BASIC (Z80)	18.6 s
Microsoft MBASIC (interpreter) (Z80)	1920.0 s

The above shows evidence of how dramatic the contrast between a compiler and an interpreter can be. It is differences like these that make the concept of Forth and its impressive speed for an interpreter so exciting.

Finally, in studying the benchmarks for the UCSD p-System Pascal, we see the following:

UCSD Pascal	(Z80)	239.0 s
Fig-Forth	(Z80)	85.0 s
JKL Forth	(Z80)	112.0 s
UCSD Pascal	(6502)	516.0 s
Forth	(6502)	265.0 s

In these cases, we see Forth outperforming a compiled Pascal. But, on closer examination, we notice that UCSD Pascal compiles to p-code, which must then be interpreted at execution time.

As in statistics, benchmarks can be made to show most any result you want. In my article, they were provided to show that Hemenway/Forth is a viable, fast interpreter and can be considered as an alternative to a slower interpreter or a slightly faster yet noninteractive compiler. Mr Gilbreath himself made a Freudian slip when he said, "You will notice . . . that many of the newer high level compilers that translate into machine are similar in execution time. The interpreters such as UCSD Pascal and the BASICs are, as expected, much slower." As stated in my article, Forth does not belong with the slower interpreters.

Bruce Sweet
Digital Equipment Corp
1925 Andover St
Tewksbury, MA 01876

Untangling transfer capabilities

The excellent article, "Untangling Local Area Networks," by Richard Parker and Sydney Shapiro (Mar 1983, p 159), was unfortunately in error concerning the data transfer capabilities of the WangNet local area network.

On p 164, the maximum rate of the WangNet is quoted as "64k bps." In fact, the signaling rate of the CSMA based WangBand, used for the interconnection of Wang CPUs, is 10M bps. Additionally, multiple 5M-bps channels are provided for Wang Peripheral attachment, as well as 9.6k-bps and 64k-bps interconnect services using standard data communications interfaces.

Terence S. Bentley
Wang Laboratories, Inc
1 Industrial Ave
Lowell, MA 01851

Can't figure it out

In Fig 1 (p 162) of the article, "Untangling Local Area Networks," the IEEE 802 Committee on LAN standards hierarchy was presented. I think there is an error in the subcommittee P802.4(BUS) presentation of the baseband. As far as I understand baseband, the signal transmitted on the cable is the data, represented by voltage shifts only. That is, data are not modulated without any carrier present. Hence, I cannot understand how baseband without a carrier can be either phase continuous or phase coherent.

D.J. Morris
Elbit Computers Ltd
10, Ben-Gurion St
PO Box 201
Nes-Ziona 70 400, Israel

Take out the baseband

Mr Morris is correct. The art (Fig 1, p 162) should have been labeled single-channel FSK or frequency shift keying in place of the word "baseband" under the line "P802.4(BUS)." I guess I'm human and can make mistakes.

Richard Parker
Contributing Editor

Designer Note #2

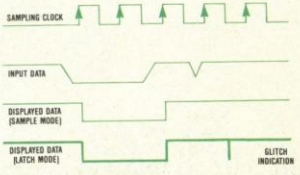
The Elusive Glitch.

From the early computer days, there's a story told about a Computer Wizard who secretly loaded in a routine which drove the other programmers wild. At random intervals, this routine would automatically activate itself and print out the following message: "I AM THE ELUSIVE GLITCH . . . CATCH ME IF YOU CAN!" Then it would reset, disappear deep into the memory of the machine, and patiently wait for the next unsuspecting moment before activating again. There was no way to find it.

Engineers debugging today's complex digital systems know all too well that the "Elusive Glitch," or other troubles induced by hardware problems such as race conditions and noise, can occur even without the help of the Computer Wizard. In the world of logic timing analyzers, a glitch is defined as an unwanted signal that passes through a threshold twice between sample clock edges. Since a glitch, by definition, is never sampled by a logic timing analyzer, it's no wonder that it often falls into the "elusive" category.

When logic analyzers were first introduced, users were sometimes frustrated with the instrument because it was not capable of solving glitch-induced problems that ranged from illegal states and extraneous counts to major, unrecoverable system crashes.

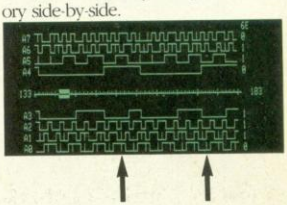
As a first attempt to remedy the situation, logic analyzer manufacturers included a latch mode in their timing analyzers. In this mode, the analyzer "remembers" the previous sample and arms a latch to capture any transitions occurring before the next sample clock edge. If a transition did occur, the latch is set and sampled at the next clock edge. Latch circuits are generally sensitive to transitions of five nanoseconds duration or longer. Thus, a glitch that is latched into the analyzer's memory is always displayed as a pulse one clock sample period wide as shown below:



Although the latch mode was a step in the right direction, engineers have found that the display of a glitch in the form of a clock pulse made it difficult to identify. A means of highlighting the occurrence of a glitch was needed. Nicolet Paratronics solved this problem by splitting its 1000-word, 16-channel timing memory into 8-channel data memory plus an 8-channel glitch memory. Using the same sample clock, both memories receive data through an 8-channel timing probe. However, since the glitch memory incorporates the latch circuit described above on each of its 8-channels, glitches are latched and clocked into the glitch memory when a glitch occurs. By contrast, the data memory does not have this latch mechanism, so it will not "see" the glitches.

To achieve the glitch display shown below, the two memories are simply superimposed. At each location where the memories differ, the display software draws a vertical line.

The NPC-700 series also includes a binary display mode that allows you to view the contents of the data memory and glitch memory side-by-side.



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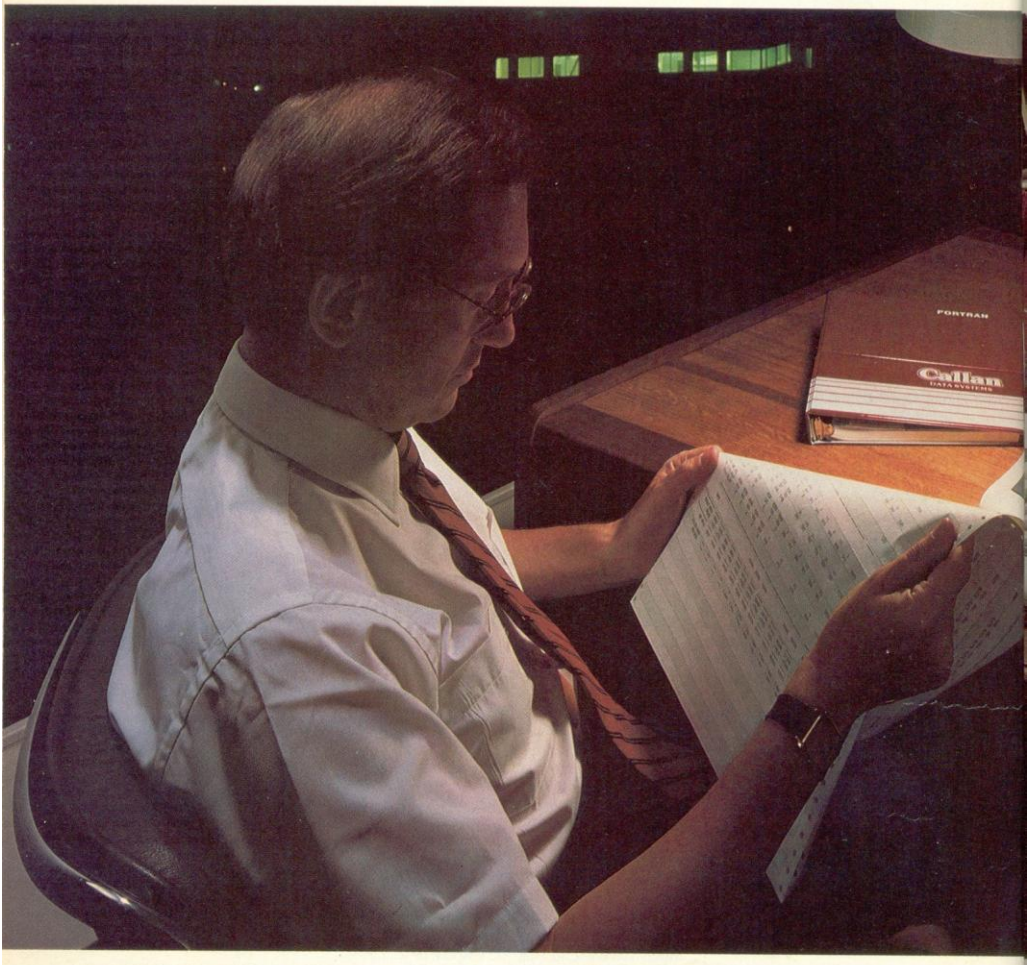

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CIRCLE 11

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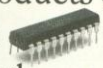
Our name is found inside the best selling computer based products on the market. We're SPI. A semiconductor firm that  understands the demands of big business.

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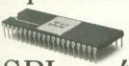
Plus, we're now the first semiconductor company in the world to produce its own silicon gate CMOS products on 5″ wafers  in-house.

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Solutions In Silicon

Zilog's 32-bit microprocessor allows smooth design migration

Zilog Corp's entry into the 32-bit microprocessor arena, planned for the second quarter of 1984, will be based on a register-oriented CPU aimed at maintaining continuity with the company's existing microprocessor family. The Z80,000 will have full 32-bit address and data paths and will support software that is a binary compatible extension of Z8000 software.

The company is thus trying to ensure a smooth migration path from 16- to 32-bit designs that will preserve the investment in existing software. Meanwhile, present designs can be planned with the coming 32-bit capabilities in mind. In addition, the Z80,000 will be hardware compatible with the company's Z-bus so that all present Z8000 peripherals will work with it. Indeed, it will use the same control signals as the Z800 and the Z8000. With this type of compatibility, the Z800 can, for example, be used as an I/O processor for the Z80,000.

The Z80,000 also preserves processor family continuity in its addressing scheme. The 32-bit logical and physical address space supports three representation modes beyond the full linear 32-bit representation. A 16-bit compact address mode is compatible with the Z8000 nonsegmented mode. Two types of 32-bit segmented addresses include a 16-bit offset compatible with Z8000 segmented mode, and a 24-bit segmented mode that lends itself to virtual memory schemes on the Z80,000.

Onchip memory management

Although the Z80,000 can address 4G bytes of physical memory, an onchip memory management unit (MMU) translates logical addresses to physical pages to be accessed from disk in a virtual memory system. The CPU cooperates with the operating system in address translation and protection. It also implements a paging translation mechanism while the operating system creates translation tables in memory. The CPU references these tables via pointers placed in its control registers by the operating system.

The CPU divides logical address spaces into pages and physical address spaces into frames. Each is 1K byte in size. Pages and frames are specified by the 22 MSBs of logical or physical address space, respectively. A logical page can thus be mapped into any physical frame. The 10 LSBs specify bytes within a page or frame and are not translated. This page/frame mapping scheme also comes in handy in multiprocessor systems that can share areas of physical memory by mapping their individual logical pages into the same physical frames.

Z80,000 address space can be set in system or normal mode; each mode can be further addressed as either a data or instruction mode. System mode protects the operating system from unauthorized access and is also required for the execution of certain privileged instructions. Separate stacks are provided for system and normal operations.

A general purpose register file, consisting of sixteen 32-bit registers, is designed to allow certain registers to easily manipulate bytes and 16-bit words of data. This leaves the other registers free to handle addresses, counters, and other data. The first four such registers (16 bytes) can thus be used as accumulators for byte data, or the first eight can be used as accumulators for 16-bit data, or for 16-bit memory addresses in compact mode. Registers can also be used as long-word registers for linear or segmented memory addresses, or as quad-word registers for Multiply, Divide, or Extend Sign instructions.

Exception handling by the Z80,000 takes four forms. Reset resets the CPU while Bus Error saves the CPU status on detecting a hardware fault. Three types of interrupt—vectored, nonvectored, and nonmaskable—and twelve trap conditions constitute the other types of exceptions.

The extended instruction trap is part of the Z80,000's support of the company's extended processing architecture (EPA). EPA allows operations defined in the CPU to be passed either to software, via the trap, or to extended processing hardware, such as the Z8070 arithmetic processing unit (APU). If the APU is in the system, the EPA flag in the flag and control word register indicates its presence and the arithmetic instruction is sent to the APU. If the APU is not present, the trap sends the instruction to the operating system which invokes software processing.

Cache memory is included

To keep onchip copies of the most frequently-used memory locations for both instructions and data, the Z80,000 has a fully associative cache mechanism. The cache stores data in 16 blocks of 16 bytes each, for 256 bytes of cache memory. An LRU algorithm replaces least recently used data on a cache miss. On store references, data references that hit in the cache are automatically written to the cache. Software can selectively enable the cache for specific instruction or data references or cause the MMU to inhibit caching for individual pages.

The Z80,000 uses a 5-MHz internal processor cycle. A 5-stage pipeline combined with the cache can be interrogated by instruction and operand fetch on the same cycle. This allows a peak performance of 5M instructions/s (MIPS). With cache misses and pipeline gaps, the performance runs from 1.7 to 5 MIPS, according to Zilog.

Die size of the Z80,000 is about 307 mils; the chip is packaged in a 68-pin leaderless carrier. Data and address lines are multiplexed. The initial version of the chip will be driven by a 10-MHz external clock, but subsequent versions using clock speeds up to 25 MHz can be expected. **Zilog Corp**, 1315 Dell Ave, Campbell, CA 95008.

—Tom Williams, West Coast Managing Editor

Circle 240

SYSTEM TECHNOLOGY
(continued on page 24)

Coming in September—
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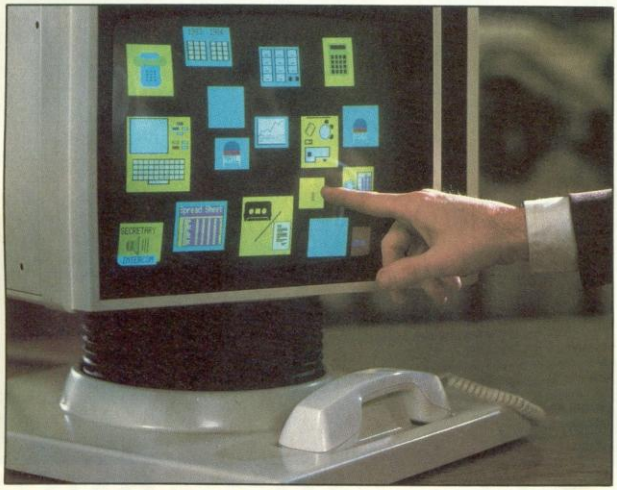
Circle 12 for Literature

Circle 13 for Sales Contact

Keyboardless office system uses touch screen



A man/machine interface for a cluster-type multi-user office system integrates voice store-and-forward with a keyboardless color touch display. The hardware configuration of the SBDL Executive System by Santa Barbara Development Laboratories differentiates between those who use information (executives) and those who enter or prepare data (secretarial and staff-level employees).

For the executive level user the system all but eliminates use of the keyboard. In its place are color icons, or "virtual device metaphors" representing familiar office objects that function as if they were real. Thus the voice telephone can be represented on the screen as a touch pad with HOLD and COM line buttons alongside a scrolling directory listing; touching a name in the list causes the system to auto-dial.

On the other hand, the secretarial or staff-level console has a dual CRT display, consisting of a duplicate of the executive touch screen and a normal alphanumeric display and keyboard. A third major component is the electronics package, which contains the processor, memory, and I/O boards along with an 80M-byte Winchester disk drive. A cluster built around one such electronics package can accommodate up to four users; clusters can be linked together using an Ethernet interface.

The electronics package forms the hub of the SBDL cluster and is built on a Multibus architecture. Each user on the system requires three circuit cards. The CPU is built around an iAPX 186 16-bit processor with 256K bytes of memory. In addition, each user has a color graphics processing card. The color graphics card not only supports the touch screen icon I/O, but also translates the virtual device metaphors to interface with the CP/M-86 operating system. The third card in the set is the voice telecommunication card.

The full-duplex voice card has an onboard codec for digitizing voice to a 7-kHz audio bandwidth. The company estimates that an 80M-byte disk could store approximately 3 h of speech. In addition, the voice card has touchtone detection that allows remote access to the system. This allows the user to either listen to voice data or leave voice messages.

OEMs will be provided with software tools for setting up the touch screen and creating virtual device icons. The screen interface is divided into sections which allow traversing the graphics icon menus. For a menu that consists of a series of screens, touching one quadrant takes the user forward in the menu; touching another takes him back a level.

Optionally included are a room camera control and a freeze-frame board for remote teleconferencing. In order to move the camera to the proper direction, zoom, and focus settings, the system allows the user to set up an icon that is a floor plan of the conference room. Touch areas within this floor plan can be associated with various camera settings and, when they are touched, the camera controller will automatically bring the camera to the predefined settings.

The freeze-frame board allows storing and forwarding of screen frames. These can be TV camera images or displays of text or graphics data. Such frames can be filed in the virtual filing cabinet, sent via the electronic mail facility, or used as slides for a live teleconference.

Although an optional plug-in keyboard is available for the executive terminal, the company does not anticipate that the executive user will need one very often. For those rare occasions that require a full keyboard, there is, perhaps, the ultimate virtual device icon: a simulation of an alphanumeric terminal on the graphics display, complete with touch-sensitive keyboard. **Santa Barbara Development Labs,** 224 Anacapa St, Santa Barbara, CA 93101.

Circle 241

SYSTEM TECHNOLOGY

(continued on page 26)

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Applied Microsystems

CIRCLE 14

Multiprocessor systems are becoming more sophisticated

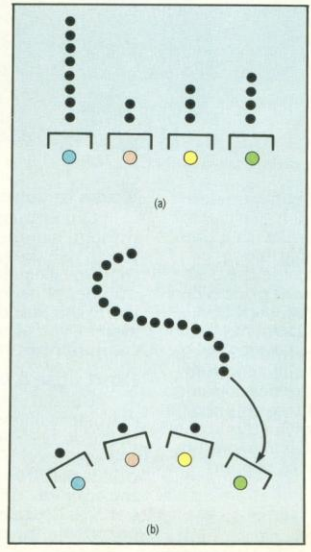
The ready availability of low cost microprocessors and memories have made multiprocessor systems more attractive. Such systems can increase system throughput at relatively small increments of cost. Expensive resources such as printers and modems can be economically shared over a larger number of users than is possible with a single-CPU system. Multiprocessor systems are also increasing in sophistication as the first generation that focused on peripheral sharing and fixed load processing gives way to a new generation that emphasizes dynamic load allocation and distributed peripheral management.

To understand the evolution of these systems, it is important to discuss the design of the first-generation machines. Typically these systems loosely couple several autonomous elements consisting of 8- or 16-bit CPUs and local program and data storage, as well as serial I/O ports. Communications largely involve data transfers between each processor element and shared peripherals like disk drives and printers. Tasks are dedicated to each processor so that all computation occurs locally. As a result, processor loads remain static once they are fixed at the system design phase.

In general, first-generation machines revolve around the S-100/IEEE 696 bus as the communications interface. Its bus protocol strictly enforces a master/slave relationship among processors, so all requests for resources are funneled to a single processor with a polling scheme. As such, S-100 based systems closely resemble a conventional single CPU servicing multiple smart peripherals (eg, disk and printer controllers).

In keeping with the task orientation of the hardware design, operating systems are split across processors. Typically, interrupt handling and resource allocation portions of the OS reside in the master processor, while terminal control and necessary tables for service requests reside in the task processors actually executing the application programs. TurboDOS from Software 2000 (Los Alamitos, Calif) is an example of this distributed OS.

These systems fit ideally in workstation-type environments that have large local processing requirements but little interaction with shared peripherals. Vendors such as Action Computer Enterprises (Pasadena, Calif), Advanced Micro Digital Corp (Garden Grove, Calif), Micromation (San Francisco, Calif), MuSYS Corp (Irvine, Calif), and OSM Computer Corp (San Jose, Calif) have focused on small business applications that use CP/M based application programs.



A drawback to first-generation systems was the dedication of tasks to multiple servers that resulted in uneven processor loads (a). Newer generation systems dynamically allocate tasks from one queue to multiple servers (b). (Courtesy: Synapse Computer Corp.)

As database requests and resource calls increase in such applications as word processing and spreadsheet calculations, the extensive overhead associated with loosely coupled systems for communications noticeably degrades performance. Data transfers across the S-100 bus are limited to 20k to 80k bytes/s due to overhead with programmed I/O.

A second bottleneck is the static processor load imposed during system design. If one processor gets bogged down with excessive computations (eg, the master processor in an S-100 system), there is no means to reallocate the work, and that processor becomes a bottleneck for the rest of the system.

In applications such as online transaction processing, bottlenecks occur when multiple processors deal with random database accesses by multiple terminals. According to queueing theory, it is easier to allocate tasks to multiple servers from a single queue than to give each server a unique dedicated list. (See the Figure.) Dedicated CPU/memory nodes rapidly become bogged down when any given terminal tends to randomly access a data base distributed over all disk devices, according to Mark Lewis, president of Synapse Computer (Milpitas, Calif).

Dynamic allocation of tasks to several processors is the common ingredient in the latest generation of multiprocessor systems. Other systems besides Synapse that use a distributed architecture include Convergent Technology (Santa Clara, Calif), Auragen Systems (Fort Lee, NJ), and Sydis Corp (San Jose, Calif).

A popular means of distributing tasks is to have several processors handle one function for the entire system. Typical choices include separate database processors, communications, and applications processing. Operating systems such as Unix are modified to handle message-passing schemes like task semaphores and

(continued on page 28)

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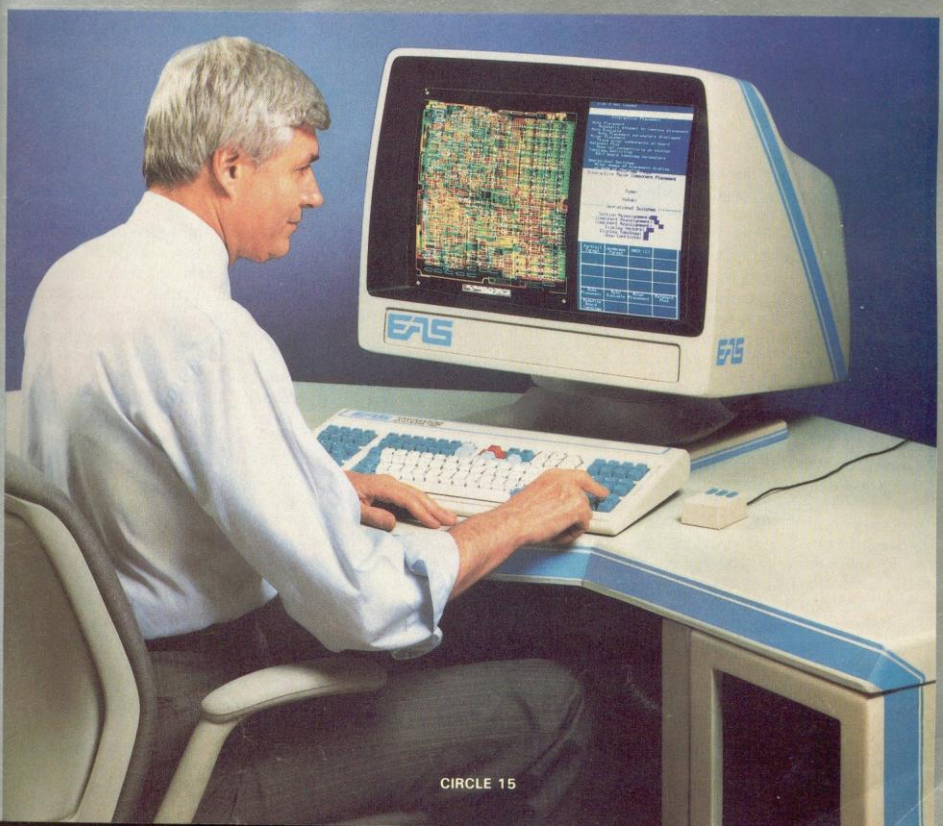

CIRCLE 15

Multiprocessor systems

(continued from page 26)

mailboxes so that processes can be synchronized across several processors. A master control processor is used in the Sydis and Convergent systems to oversee the system. This master processor acts as a gatekeeper as it schedules tasks to execute on the first available slave processor.

Lewis notes that a master processor in such configurations can be the bottleneck of the system. Even if there is a backup to the master processor in a redundant architecture, he notes that it can only handle about 50% of the work that contributes to the overall system performance degradation.

The Synapse attempts to bypass the need for a master control processor by having three queues (database access, applications processing, and I/O), all access a common memory in a tightly coupled architecture. Object-oriented programming techniques treat each task as a discrete instance that contains both data and methods to process those data. Pointers to a task's memory location are placed in the queue for the first available processor to execute any necessary function. Since both data and programs are encapsulated in a common area, there is no need for extensive message passing schemes to synchronize tasks. Object-oriented programming techniques also prevent one processor from updating files without notifying other concurrently executing processors, since there is only one copy of the file for all processors to access.

Distributed or tightly coupled, this latest generation of multiprocessor systems is rivaling minicomputers and mainframes with processing speeds from 5 to 35 MIPS. As these systems begin to use the newly introduced 32-bit processors, performance may reach the supercomputer class.

—Joseph Aseo, Field Editor

Array processor combines synchronous and asynchronous techniques

Basically peripheral CPUs that calculate quickly, array processors typically incorporate either synchronous or asynchronous timing architectures. Numerix has built its MARS-432 using a combination of the two approaches.

The full floating point MARS-432 is priced in the same range as other high performance array processors yet operates three times faster, and has larger memories. Add and multiply times of 100 ns result from direct addressability for up to 16M words of data memory, direct access to the high speed internal bus, and DMA transfers at I/O bus rates of 20M bytes/s.

Key architectural elements are the interface processor and the data processor. Data transfers over the data bus (DBUS) between data memory and host computer or data memory and external digital I/O ports are controlled by the interface processor (IP). The IP provides bus arbitration with a 200-ns cycle. Eight prioritized channel levels supply 32-bit transfers to any of eight bus destination devices.

The data processor's structure explicitly separates data memory and program memory to attain additional speed in arithmetic processing. Data memory contains up to 512k words of 100-ns RAM and has a

16M-word address space. Memory is interleaved to provide a 100-ms cycle up to the 16M-word addressing limit. Program memory has a 64k address space with a 4k cache broken into 64-word pages. It can be DMA loaded from host or data memory. Data paths between the two allow data memory to be used as bulk storage for large program segments. However, this results in performance degradation.

Supplying 100-ns multiply, 100-ns add arithmetic performance, the data processor responds to 72 arithmetic and logical instructions in a data dependent conditional instruction set. A 16-level address stack handles conditional branching and subroutine calls. Compatible 32-bit integer and logical operations permit mixed mode functions to be handled. Floating point operations use a 24-bit sign/magnitude mantissa and 8-bit radix-2 exponent format. Typically, a 1024 complex in-place fast Fourier transform algorithm requires 1.7 ms to complete. Total throughput is claimed as 30M floating point operations/s.

Primary arithmetic elements are a multiplier and two adders. Interconnected with multiple data paths, all elements may execute in parallel. Digital input and digital output modules (DIM and DOM) provide auxiliary input and output data paths, supplying a standardized interface to the DBUS and communications lines. The host data interface (HDI) serves as an equivalent interface for the host computer. Program and data are transferred from the host's memory through this interface using DMA techniques. DMA to host memory and to data and program memory components allows programs to be written without reference to I/O transactions.

(continued on page 30)

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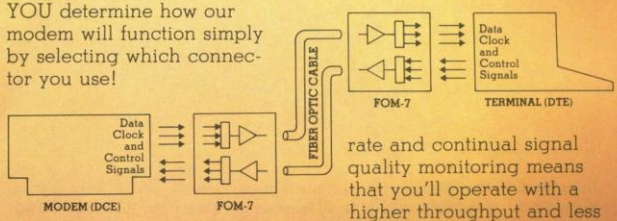

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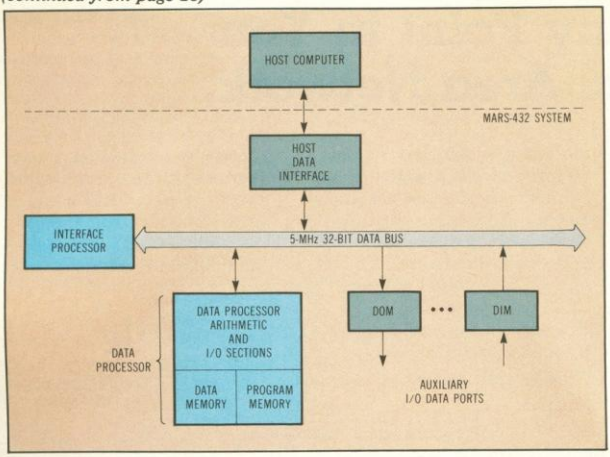
CIRCLE 16

Sync/async processor

(continued from page 28)



Using the interface processor to arbitrate transfers over the 32-bit data bus, Numerix' MARS-432 performs full floating point calculations at 30M FLOPS. This performance results from the unit's large memories and directly accessed high speed internal bus.

A second, slower control bus (CBUS) is threaded through the HDI, CP, and DP elements and through DIM and DOM. This bus supplies comprehensive addressing capabilities that aid in software development and diagnostics.

Software tools for the system include a FORTRAN development system for high level language access. This package consists of compiler, linker, and debugging monitor. An automatic code optimization utility automates the writing of pipelined code at the assembly language level. The application library includes math signal processing, and image processing routines.

Configured with 64k words of data memory, the unit sells for between $80,000 and $100,000, depending on external interface and software options. Production quantities are scheduled for availability in Oct 1983. **Numerix Corp,** 320 Needham St, Newton, MA 02161.
Circle 242

Mini and micros divide system work tasks

Separating resource allocation from task processing, the Omnix 186 multi-user system from Computer Automation's Naked Mini Division dedicates the company's model 4/04 minicomputer to peripheral management and I/O processing while a 16-bit Intel 80186 microprocessor takes over program execution. Thus, applications running under industry standard operating systems such as CP/M-86, MP/M-86, and Concurrent CP/M from Digital Research can coexist with applications running under the proprietary Opus-1 operating system.

Minicomputers are ideal candidates to handle resource allocation since their multitasking operating systems are optimized for disk and peripheral management as well as for handling I/O processing at data rates approaching 19.2k bps. However, program execution typically takes up a considerable amount of CPU time, with noticeable performance degradation as users are added to the system.

Microprocessors can execute single-task code quickly with rapid screen updates. Yet, execution speed is often compromised by transfers to peripherals and other I/O-bound operations. Elaborate scheduling algorithms must be used in conventional single-CPU systems (whether minicomputer or microcomputer based) to accommodate these competing needs. Distributing functions to processors best able to handle these divergent requirements greatly reduces the need for such detailed scheduling.

Acting in synergy, the 4/04 processor intercepts resource calls from up to four 80186 microprocessors executing programs under different operating systems. A 128K-byte buffer memory onboard the 4/04 handles all DMA transfers along the Multibus-like backplane. Traffic includes interprocessor communications, as well as transfers to the 4-port serial I/O cards (up to four possible) and disk controllers.

Each 80186 processor has its own 256K-byte dynamic RAM, to which all memory fetches are routed. Such a set allows each processor to think it has exclusive control of peripherals and disks. To the 4/04, each microprocessor looks like an intelligent peripheral such as a printer or disk controller generating service calls. The conventional multitasking Opus-1 operating system can be used to schedule resource services for multiple 80186s.

Processor selection is transparent to the user. Since terminal I/O is handled by the 4/04, users log on under the auspices of Opus-1. If programs are executed under a different operating system, Opus-1 transfers files containing the desired operating system and application program into the first available microprocessor. Complete programs are passed from a central data base to the working memory of the microprocessor so that further bus activity only involves peripheral service calls to the 4/04. Separate file directories are maintained for each operating system, with files passed transparently without alterations by Opus-1.

Multiple users of the same program are treated differently from a

(continued on page 32)

The Lundy UltraGraf® is absolutely the fastest draw in the West or anywhere else.

This is the fastest, most intelligent 3-D computer graphics workstation available. The superlatives would seem to indicate a high price, too. But the Lundy UltraGraf workstation is surprisingly low cost considering its unmatched performance features.

At Lundy we don't develop technology for its own sake; we develop it to meet your needs. In the case of 3-D computer graphics workstations, you needed more speed, higher IQ, larger display and easier operation. UltraGraf delivers all four.

The Lundy UltraGraf is first when it comes to speed and IQ.

Keys to UltraGraf's instant response are a high speed microcomputer and a high resolution vector display, both developed by Lundy.

Besides these features, we've designed more intelligence into the workstation, so UltraGraf places fewer demands on your host computer.

The result is unmatched interaction while freeing up your host computer to concentrate on other operations.

19×15 inches sets a new screen standard.

UltraGraf's 21-inch CRT has the largest viewing area—19×15 inches—in the industry. Fast vector drawing and minimum operator time produce easy-to-read, flicker-free images. Spot size is only one ten thousandths of an inch, which produces remarkable crispness and clarity.

Lundy UltraGraf sets 3-dimensional standards.

Furthermore, UltraGraf is easier to use. You send a picture only once, instead of resending over and over as with many other systems. And you have local storage of all control functions for the interactive input devices. This provides maximum input flexibility, with minimum keyboarding.

Lundy helps you see more in graphics.

When you take a close look at our graphics terminals, service, support, software, systems capability, enhancements—and our company—you'll understand why Lundy can help you see more in graphics now and in the long term.

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LUNDY®

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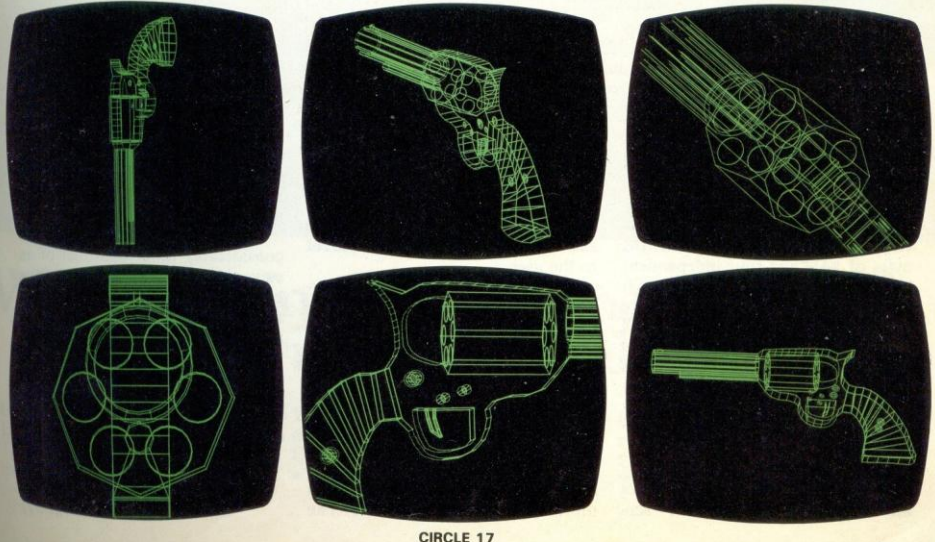


CIRCLE 17

Minis and micros divide tasks

(continued from page 30)

single user executing multiple tasks. The former case would require that MP/M-86 be configured on one 80186, while the latter case would cause Concurrent CP/M to be called. In either situation, Opus-1 transfers user control to the executing processor. The 4/04 then acts as a background processor since the I/O and disk handling portions of the resident operating systems already contain the necessary translation tables to convert service calls to Opus-1 calls. Although programs are executed by the microprocessors, overall system control will reside with the 4/04 processor.

Users may develop application programs in Trans-BASIC, the company's business language compiler with multikey ISAM file manager; CBASIC-86 can be used for CP/M and MP/M environments. COBOL, FORTRAN, and Pascal compilers are also available. Each 80186 board contains 32K bytes of EPROM for custom software packages, with an optional 8087 floating point processor available to increase throughput.

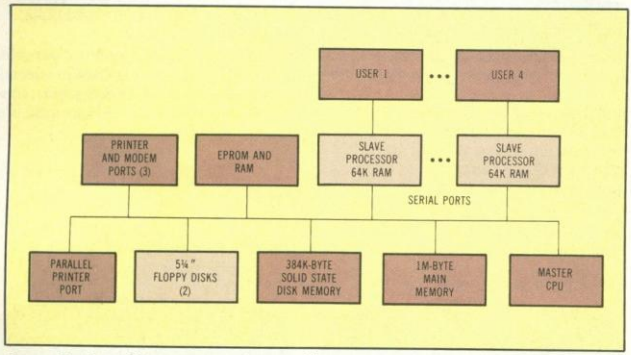
Systems can be configured either with a single 1M-byte 5¼" floppy disk and up to two 5¼" Winchester drives, or a single quarter-inch tape drive with one Winchester drive. Formatted capacities for the Winchester drives range from 5M to 20M bytes. Internal memory will be expandable to 1M byte as 256K-bit RAMs become available.

Single-unit prices begin at $899 for a system with a 5M-byte Winchester drive and 1M-byte floppy backup. A typical 20M-byte Winchester system is quoted at $12,490. Volume shipments will begin in Oct. 1983. **Computer Automation, Naked Mini Div,** 18651 Von Karman Ave., Irvine, CA 92713.

—Joseph Aseo, Field Editor

Circle 243

Multi-user system has 8- and 16-bit CPUs



CompuPro's multiprocessor system combines an 8088 main processor with up to four Z80B slaves, one for each user. System memory is shared by all processors, but with a portion accessible only to the master.

Developed first as a series of separate boards, then configured as a single-board computer, CompuPro's MultiPro 11 multi-user multiprocessor microcomputer system features a 16-bit, 8-MHz 8088 CPU with 1M bytes of RAM and four independent 8-bit, 6-MHz Z80B processors each with 64K-byte RAM. Solid state 384K-byte disk memory, two 5¼" floppy drives that store 1.6M bytes each, and seven serial RS-232 ports that include a modem port, plus a Centronics compatible parallel port are also part of the CompuPro system's standard features.

System memory is shared among the processors. The lower 768K bytes are accessible only by the 8088 master, while the upper 256K portion is divided into four 64K banks, one for each Z80B slave. Data and service requests are passed between the 8- and 16-bit processors via the shared memory, and are transparent to the user.

The company's MP/M® 8-16 operating system has been enhanced to handle the multiple processors and their requests for I/O or disk service. A 3K-byte basic input/output system (BIOS) in each slave processor's address space signals the master via a hardware interrupt line, puts pointers to data and operating system request codes in specific memory locations, and then waits until the master responds. The master CPU checks the slave BIOS locations to determine the required service, moves data to or from the slave memory, and then signals the slave to continue processing.

Each slave processor has one dedicated serial port for a terminal. The master controls the remaining system resources. These include an optional 8-MHz 8087 math coprocessor, three additional serial ports, one parallel port, the disk drives, and the RAM disk emulator. Facilities for increased memory and future networking options, possibly via the SASI bus, are also provided.

Unlike most systems, software was developed before the hardware. The system was emulated as a set of cards on a motherboard; then, interface protocols were verified, and operating system code was written. Engineering work on board design and layout began only after the system was shown to be workable.

The system's $4995 list price is considerably lower than that of an equivalent micro built from discrete boards, and marginally better performance is gained from the eliminated bus delays. Preproduction units will be shipped this month; volume orders are scheduled to arrive from Oct on. **CompuPro,** 3506 Breakwater Dr, Hayward, CA 94545.

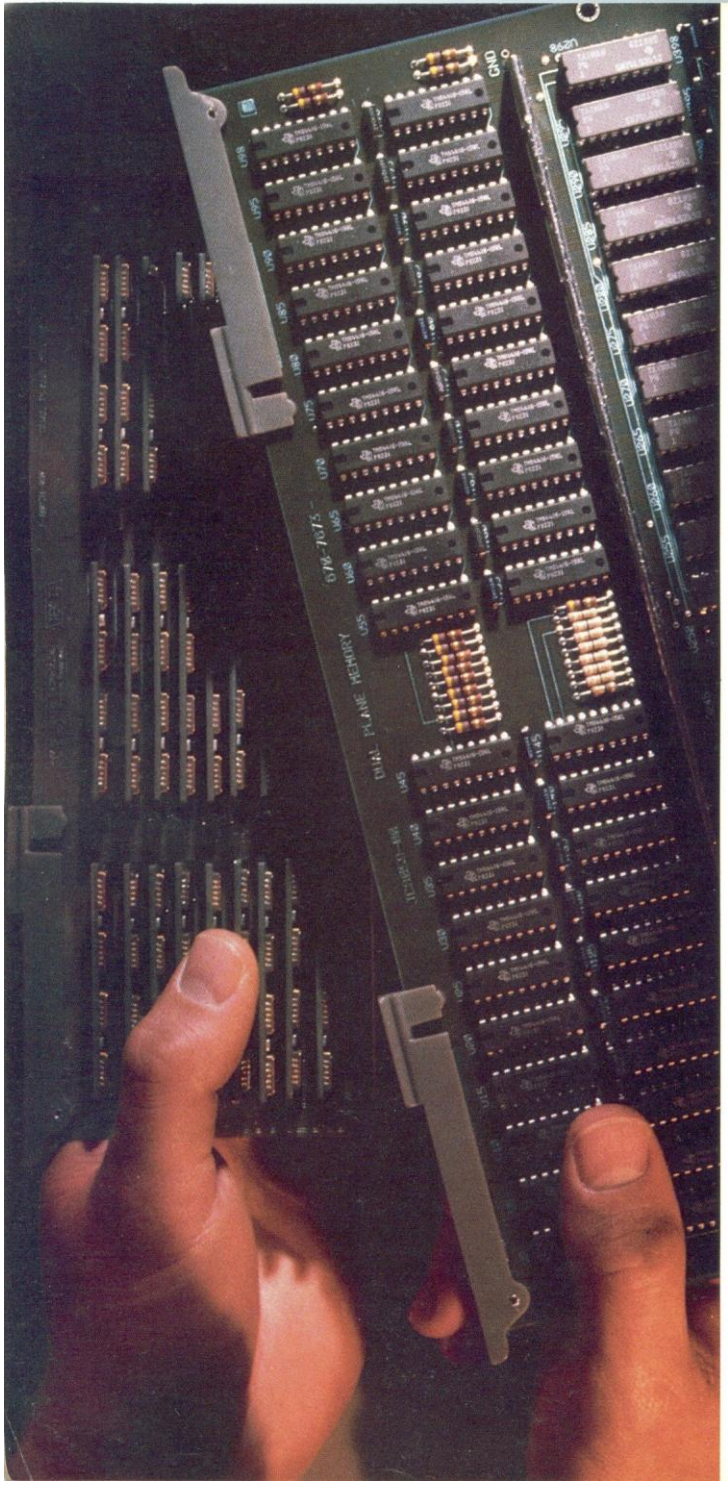
Circle 244

SYSTEM TECHNOLOGY

(continued on page 37)

When Texas Instruments and Tektronix team up, brilliant ideas take shape.

- **For high-resolution color graphics** and lower costs, Tektronix uses TI's TMS4416 64K DRAM in its top-of-the-line graphics terminal *(Page 2)*.
- **TI's comprehensive choice** for microprocessor-based systems: 64K DRAMs, static RAMs, controllers, and comparators *(Page 3)*.
- **First low-cost 64K DRAM chip carrier** doubles the density of DIPs and provides all the advantages of TI plastic J-lead design *(Page 4)*. ▶



TI's new memor

125 MHz pixel-rate performance. W memory part count cut by 75%. An cost savings more than 50%. The u TMS4416 16K × 4 DRAM from Te Instruments is the first 64K dynamic random-access memory (DRAM) in world that could provide this perfor mance at that price. And that's why was chosen for the new, advanced Tektronix 4115B Computer Display Terminal.

Designed for the most demanding CAD/CAM applications, the Tektr 4115B features a high-resolution col raster-scan display. This 60-Hz, non interlaced, flicker-free display provid resolution of 1280 × 1024 pixels. Up 256 colors can be displayed at one ti from its palette of 16 million colors!

System-wide cost savings

By upgrading from four 16K devices single in-line package to one TMS4 ByFour* DRAM (see photo), Tektro cut costs by more than 50% and me part count by four times.

System costs also were lowered, du fewer interconnects and support circ This reduced inventory, cut power re quirements, and enhanced reliability

Lower power, higher reliability

With one 5-V power supply at 130 m per 64K, the TMS4416 significantly power consumption. This increased power supply margins and reduced no Plus, lower heat dissipation and fewer terconnects improved system reliabili

Equally important, TI met Tektro critical delivery schedule.

Meets many design needs

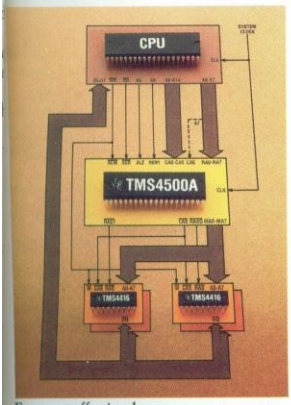
Where can the TMS4416 help you? personal and small business computer Intelligent terminals requiring 16K- a 32K-byte memory modularity. Single board microcomputers. And more.

The output/enable feature makes i facing the TMS4416 with micro processors simple. ■

◀ **An exceptionally "clean solution,"** TI's TMS4416 16K × 4 DRAM enabled Tektronix to reduce memory component count by four in its new 4115B Computer Display Terminal. Each TMS4416 replaces four 16K devices mounted on a single in-l package.

*Trademark of Texas Instrume

16K x 4 DRAM cuts costs by 50% for Tektronix.



For a cost-effective, low-power memory system that uses minimum board space, combine the TMS4416 or the TMS4164 64K DRAM with the TMS4500A.

One TI chip links DRAMs with CPUs.

TI's TMS4500A DRAM controller saves design time and IC costs.

Easy to use, the TMS4500A supplies a reliable, single-chip interface between dynamic memory and the microprocessor.

The TMS4500A speeds and simplifies your design task by providing address multiplexing, cycle timing, arbitration logic, and refreshing—all on one chip. It saves substantial design time, circuitry, board space, and power. Plus replaces as many as 15 discrete support ICs.

Highly versatile, the TMS4500A interfaces with all popular microprocessors. And is compatible with DRAMs from 4K up—*from any manufacturer.*

Think of the board space and time savings and power reductions possible when you combine TMS4416 or TMS4164 64K DRAMs with a TMS4500A.

Using the TMS4500A, you can easily handle up to 256K bytes per controller with TMS4416s or TMS4164s. With additional decodes, you can go to 512K bytes and more.

For details on the TMS4500A, check number 1 on the next page. ■

TI's fast 64K DRAM just got faster.

Now, TI's pacesetting TMS4164 64K × 1 DRAM comes in a still speedier version. Our new TMS4164-12 provides 120-ns access time, 230-ns cycle time, and just 175-mW typical power consumption per device. Two other speeds also are available: 150 and 200 ns.

We've also taken another positive step. To increase board density and lower costs, the TMS4164 now can be yours in 0.285 in. × 0.425 in. plastic chip carriers.

Like the TMS4416, the TMS4164 requires only a single 5-V power supply. This—combined with fewer sense amplifiers—reduces power dissipation and increases system reliability.

In addition, both the TMS4164 and the TMS4416 employ interlocked internal clocks, which provide more precise timing sequences. This allows all chips to run at maximum speeds without the danger of race conditions. And these clocks reduce power consumption by ensuring that each clock is activated only as long as necessary.

When you need high-quality 64K DRAMs, rely on TI's two outstanding choices. For high speed and low power, select the TMS4164. For high bandwidth and modularity, choose the TMS4416. Both are cost effective. Easy to design with. And state of the art.

For more information on the TMS4416 and TMS4164, check number 2 on the coupon. ■

Fast, low-cost 16K static RAMs.

For an economical, high-density memory in smaller systems and peripherals, you can't do better than TI's TMS4016 static RAM.

Interchangeable with TI's TMS2516 and all other 16K, 5-V EPROMs, the TMS4016 makes board design simple and fast. This gives you flexibility to prototype and de-bug in RAM, then convert to EPROM or ROM for production. All in the same socket.

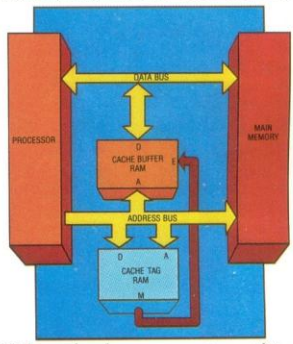
Just right for microprocessors, the TMS4016 features 2K-by-8 organization and single 5-V power supply. And operates at 120, 150, 200, or 250 ns with 385 mW maximum power dissipation.

For more facts on the low-cost TMS4016, check coupon number 3. ■

New cache-tag comparator speeds system throughput.

TI's new TMS2150 cache address comparator can improve high-performance microprocessor or bit-slice system throughput by up to three times. Plus reduce cache memory IC count, board area, power dissipation, and cost.

With the TMS2150, no wait states need to be implemented in microprocessor access cycles in response to slower-cycling DRAMs. The TMS2150,



High-speed cache memory systems utilizing the TMS2150 will enable high-performance microprocessors to set new cost-performance standards with large, low-cost dynamic main memory.

in combination with high-speed static RAMs, completes an entire high-performance cache memory system. With a maximum 45-ns delay from address to match valid, the TMS2150 can provide TTL performance at one-tenth the part count and 10% the power.

Operating from a single +5-V power supply, the TMS2150 consists of a high-speed 512 × 9 static RAM array, parity generator and checker, and a 9-bit high-speed comparator.

For more specifics, check number 4 on the coupon. ■

TI's 64K DRAM chip carrier. More memory for less money.

Increased board density can be achieved economically with TI's exclusive plastic 64K DRAM chip carriers—an industry first.

Now you can pack even more memory into less space for less money. TI's unique plastic TMS4164 chip carrier gives you the high-density memory option you need. At a price you can afford.

Dramatic reductions in board size

TI's low-cost 64K DRAM chip carrier provides twice the density of the conventional DIP. System size can be substantially reduced. And significant cost savings realized.

Unlike conventional DIPs, TI's advanced TMS4164 in chip carriers can be surface mounted. As a result, the number of layers in the printed circuit board is greatly reduced, and fewer boards are required.

Ideal for SIPs

TI's 0.285 in. × 0.425 in. surface-mounted chip carriers are designed to meet the critical height requirement of single in-line modules (SIPs), as well as offer the necessary low power dissipation. And, now TI has in development single in-line module arrays in various organizations to meet your future system needs.

For more information on the world's first low-cost 64K DRAM chip carrier, check number 5 on the coupon. ■

Texas Instruments P.O. Box 401560
Dallas, Texas 75240

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TEXAS INSTRUMENTS

Creating useful products and services for you.

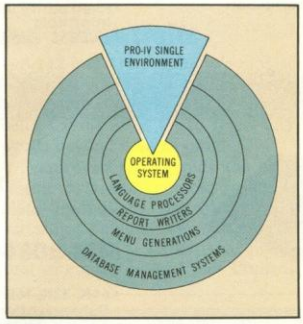
Reentrant code eases program development

An integrated applications environment for commercial users overcomes the limitations of program and application generators by not producing any code to be compiled and debugged. Instead, the PRO-IV applications system uses a threading algorithm to link machine language subroutines resident in main memory. Furthermore, since PRO-IV handles the necessary interfaces to the file system and peripherals, programs are isolated from hardware and operating system quirks.

Providing an integrated environment for program development and execution also ensures software portability between different vendors. PRO-IV can now execute as an application program on Digital Equipment Corp's (Merrimack, NH) PDP-11 computers with RSTS/E or RSX-11 operating systems, Microdata Corp's (Irvine, Calif) Sequel minicomputers, and CIE Systems' (Irvine, Calif) 68000 based machines using Regulus (a Unix look-alike). It can also be used on any 8086/8088 based personal computers with CP/M-86 or MS-DOS operating systems using packages licensed by Capro, Inc (Garden Grove, Calif). A version for IBM mainframes is expected soon.

Portability and speed result from a conscious effort to address a specific set of requirements. Since there is a well-defined set of functions common to all commercial applications (eg, interactive queries and file updates), machine language subroutines are written for all users, instead of recoded for individual applications. Users specify the functions needed for a given application through a series of menus displayed on a CRT screen.

During the generation process, a threading algorithm picks the necessary routines and generates a runtime link table for that application. Although the subroutines reside in main memory (32K bytes in all), user link tables and associated data can either be located in main memory user partitions (about 6K bytes each) or transferred to disk. The threading algorithm also seeks to optimize performance with careful subroutine ordering in the tables. However, multiple accesses to the same routine are not accounted for because event scheduling is left to the operating system's discretion.



Rather than having to cope individually with the operating system, language processor, report writer, menu generator, and database management system, PRO-IV provides a single environment that allows the application designer to integrate all functions into one set of procedures. PRO-IV's online logic debugger greatly decreases application design time and eliminates manual logic and syntax debugging.

Since coding in high level languages is no longer required, using menu-driven displays and reentrant subroutines increases the viability of software prototyping. Long development cycles are thus shortened because compilation and debugging are eliminated. Systems analysts can rapidly convert a user's specifications into PRO-IV link tables, generate the necessary screen masks and report formats, then let the user evaluate the results.

With PRO-IV, any necessary changes can be easily implemented since they only require modifications to the specifications, rather than to the code itself. Previously, extensive compilation and debugging made it difficult to make changes.

PRO-IV users claim an 80% reduction in programming effort as compared to similar applications coded in high level languages like COBOL.

Consequently, program design rather than coding technique becomes the prime performance criterion. Program design is critical since about 90% of the logic in commercial applications involves decision making; because little number crunching is involved in commercial applications, optimizing coded algorithms cannot increase performance. Also, machine language subroutines ensure the fastest possible execution, and I/O handling is fixed.

Furthermore, PRO-IV minimizes hardware and operating system dependencies. Although the bulk of the subroutines are written in machine language, only three routines are dependent on hardware configuration and operating system organization. These routines deal with interfaces to the file system and drivers for terminals and printers. Otherwise, PRO-IV provides a single environment for screen-oriented queries, database management, and report generation.

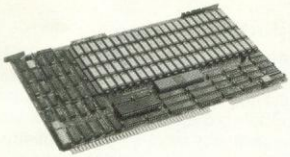
Future versions of PRO-IV will be coded in C to further reduce processor dependency by eliminating the need for machine language routines. Although a 20% performance degradation is noted, Sushil Garg, developer of PRO-IV for Data Technical Analysts (Honolulu, Hi), says that users will not notice the difference since commercial applications tend to be I/O bound rather than CPU bound. Any operating system (including Unix) that supports a C compiler could run the package as long as system calls are consistent with the C language kernel.

Operating system dependency will be further reduced when a universal file interface is implemented. Future versions will view all files as single key/single type, regardless of the actual file organization the operating system specifies. Thus, all subroutines will only get a logical look at

(continued on page 39)

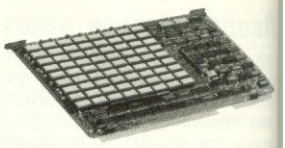
MULTIBUS* MEMORIES

DYNAMIC RAM (IEEE P796-COMPATIBLE)



MM-8086E

- 512K, 256K bytes
- Error detection and correction
- 1000_H boundaries/16 Mbyte address
- Access/Cycle: 300/500 nsec
- CSR/ESR for EDC control and LED error correction indication
- Battery backup option



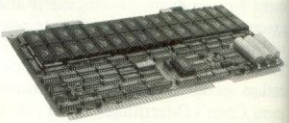
MM-8086D

- 512K, 256K, 128K, 64K bytes
- For 8 and 16-bit processors
- 1000_H boundaries/16 Mbyte address
- Even parity with output selectable to any of bus interrupts
- ACCESS/Cycle: 250/400 nsec

NON-VOLATILE CMOS RAM (IEEE P796-COMPATIBLE)

MM-8000C

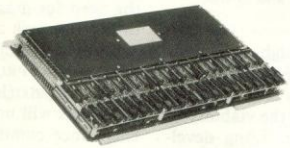
- 128K, 64K bytes
- Data retention (on-board batt.):
  2 weeks rechargeable batteries
- 4000_H boundaries/16 Mbyte address
- Access/Cycle: 220/220 nsec
- Battery status line allows monitored battery condition
- Redundant batteries provide improved reliability
- Accommodates 2716 EROM



MM-8086C

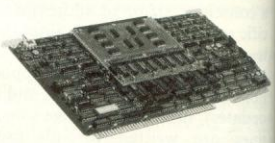
- 64K, 32K, 16K bytes
- Data retention (on-board batt.):
  3 weeks rechargeable batteries
  2 yrs. non-rechargeable batteries
- 1000_H boundaries/16 Mbyte address
- On-board calendar/clock
- Access/Cycle: 250/250 nsec
- Redundant batteries provide improved reliability
- Accommodates 2716 EROM

NON-VOLATILE CORE MEMORY



MM-8086

- 32K bytes
- For 8 and 16-bit processors
- 1000_H boundaries/1 Mbyte address
- Access/Cycle: 375/1200 nsec
- Power monitoring for data protection



MM-8086/16

- 16K bytes
- For 8 and 16-bit processors
- 4000_H boundaries/1 Mbyte address
- Access/Cycle: 280/800 nsec
- Power monitoring for data protection

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CIRCLE 19

Reentrant code eases development

(continued from page 37)

the files, rather than the physical description. Included with the universal file interface will be a universal record interface that converts external formats specific to a particular computer to an internal format all subroutines can recognize. A tag that describes the physical layout of the data will be attached with a logical name for the file. PRO-IV can then dynamically block or unblock files as they are transferred between the existing file system and the internal buffers.

Such an approach is feasible because the package contains its own relational database manager and does not rely on database managers developed for a specific computer. As such, any subroutine needing data can access a global data dictionary with field labels instead of physical locations. This allows data relationships to be created dynamically in the context of the operation being performed. This eliminates the need to anticipate all combinations beforehand, as in other database managers.

—Joseph Aseo, Field Editor

Recognition scheme ignores vocal traits

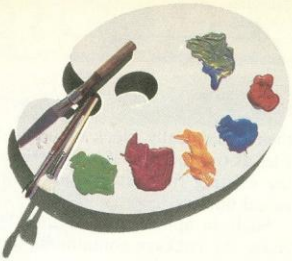
Automatic recognition of speech independent of the speaker's vocal qualities is Voice Control System's claim for its Universal Speech Access-II (USA-II) scheme. Such "coloring" components of speech as pitch, inflection, and accent are disregarded. This feature analysis technique focuses on the order of specific sounds instead of relying on entire phrases—a method other recognition schemes currently favor. Memory requirements are reduced since large reference vocabularies are not stored for matching.

Typical speech recognition systems analyze formant frequencies that occur in the speaker's voice range. For example, one such system takes 10-ms samples of incoming speech and measures the spectral peaks and valleys occurring in the frequency domain. Measured at 16 different frequencies with bandpass filtering, these peaks and valleys are encoded as "1s" when the slope is increasing at that frequency and "0s" when the slope is decreasing.

Once encoded in bits, the incoming phrase is compared against patterns (templates) of reference words stored in a vocabulary list. A threshold score (0 to 128) tracks how close each template comes to matching the uttered phrase. Templates are then put in rank order with a score of 128 designating a perfect match. Next, a delta score is calculated by taking the threshold score of the incoming phrase and subtracting the threshold score of each of the two closest reference words. For example, threshold scores of 120 for the uttered phrase and 112 and 110 for the two closest reference words would yield delta scores of 8 and 10, respectively. This delta score can be set to reject any words beyond a given limit.

Feature analysis avoids the processing overhead required for template analysis by searching for a pattern of only 42 basic sounds. Dr Thomas Schalk, senior vice president of consulting at Voice Control Systems, explains that humans distinguish words as unique combinations of consonant and vowel sounds, with consonant recognition more important for comprehension. The current algorithm implemented by the USA-II scheme spots these features as the voice is digitized, and sets unique flags as different sounds are encountered. There is no need

(continued on page 41)



A GOOD CREATOR NEEDS BETTER TOOLS

Everybody knows a creator needs the proper tools to create the 'perfect masterpiece'. Zax Corporation has the answer. The 'Box' computer used in conjunction with our Emulators creates an efficient tool that allows the design engineer to edit, assemble, link and debug to his specifications...in the simplest, most effective way, at a fraction of the cost.

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CIRCLE 21

Speech recognition system

(continued from page 39)

for the complex mathematical transformations (ie, normalizing the frequency with respect to time) required in template analysis. Instead, at a later time the processor just checks which flags were set during the utterance to determine the word.

Speaker differences due to accent, sex, age, and inflections are ignored because consonants are emphasized. On the other hand, template analysis requires a training period of three to five iterations of the same word so that averaging techniques can be used to make the templates themselves. Furthermore, Schalk states that response times stay the same as vocabulary size increases using feature analysis. He notes that there is no need to match every reference word with the incoming utterance, as required in template analysis. Response times for such systems can range from 50 ms for a 40-word vocabulary to over 200 ms as the vocabulary size exceeds 200 words.

However, the overall adequacy of a speaker independent system can be challenged. A manufacturer of a speech recognition system employing template analysis notes that feature analysis requires detailed knowledge of how words are constructed. This makes the technique language dependent. For example, it may be difficult to apply the feature analysis method to such languages as Japanese or Chinese because of inherent differences from English word structure.

Both feature analysis and template recognition techniques have difficulty with words that differ only by vowel sounds (eg, pit, pat, and pet). Although vowel sounds are characterized by their corresponding spectral peaks within the formant frequencies, each human voice projects different formant frequencies for the same vowel. Schalk claims that accurate vowel recognition is addressed in feature analysis using improved algorithms. Conversely, manufacturers of template systems recommend that reference vocabularies be used to minimize errors resulting from similar sounding words.

Memory requirements for the USA-II scheme are specified at 6K bytes of RAM, with possible reductions to 3K bytes if the processor used allows interrupts. Template analysis systems can require 500 bytes of buffer memory, with an additional 67-byte/word memory for storing reference templates. Both techniques work well with 8- or 16-bit processors. Licensing arrangements for the USA-II scheme are available. **Voice Control Systems, Inc,** 4660 Sunbelt, Dallas, TX 75248.

—Joseph Aseo, Field Editor

Circle 245

PERIPHERALS

Color terminals display NAPLPS graphics

Until recently, equipment for displaying North American Presentation Level Protocol Syntax (NAPLPS or PLPS) graphics has been rare. Now, Verticom Inc has introduced two color graphics terminals that provide this capability to users and system builders.

The model PLP100 is an intelligent ASCII terminal with moderate resolution, capable of decoding and displaying PLP graphics. It is also DEC VT100 and Tektronix 4010 compatible. Enhanced model PLP200 adds interactive generation of PLP data bases to the unit's features. Optional host resident C software provides for rapid generation of PLP frames. The enhanced terminal also has three optional Multibus slots for OEM use.

(continued on page 42)

Terminals display NAPLPS graphics

(continued from page 41)

Both models include dual Z80 microprocessors, an integral 105-key ergonomic keyboard, and two display memory pages with 640 x 480 x 4 resolution, allowing 16 of 4096 available colors to be displayed onscreen. Graphics primitives and text handling and local editing support for the host computer are available. The standard configuration includes a 12″ diagonal monitor.

NAPLPS is an extension of the Canadian Telidon graphics transmission standard that encodes text and graphics information in an efficient, terminal-independent format. AT&T has adopted the PLP standard for commercial video-text trials over broadcast TV, as have major vendors of computer hardware and software.

Limited acceptance of computer graphics has often been attributed to the lack of any standard protocol for transmitting graphic data. Most hardware and software vendors have developed individual ways of encoding, handling, and transmitting images. Very few of these techniques were compatible among machines, or among different programs running on the same machine. Although large graphics data bases and sophisticated data manipulating programs exist on mainframe computers, there has seldom been any way to transfer these data or display the results of image manipulation on mini or microcomputers. The PLP standard addresses this lack, and, given the number of prestigious vendors and organizations offering support, it may become the standard for graphics transmissions. Pictures can be transmitted over telephone lines, microwave links, local area networks, or any other communications link regardless of bandwidth.

Model PLP100 is priced under $5000 and the PLP200 is under $6000. Expected availability is in Nov 1983.
Verticom Inc, 545 Weddell Dr, Sunnyvale, CA 94089.
Circle 246

DEVELOPMENT SYSTEMS

Development system aims at 16-bit micros

Combining hardware and software tools, the Intellec Series IV simplifies the design of products based on iAPX 86, 88, 186, 188, and 286 microprocessors.

Intellec Series IV takes us one step closer to the virtual engineering environment of the future. To improve productivity of designing and developing complex 16-bit systems, models 430/431 incorporate network-like functionality in standalone workstations. Combination of hardware and software development tools results in improved designer productivity and shorter time to market for products.

Built on a multiple processor architecture, the system uses the 8088 running the iNDX operating system for 16-bit development projects. For 8-bit targets, projects run under the 8085 and the ISIS-N operating system. Even greater performance can be gained by upgrading the system with a 16-bit 8086-based board. This board increases throughput and adds 128K bytes of RAM to the system's basic 384K bytes. Peripheral configurations of the system combine two 5¼″ floppy disk drives with a standalone 35M-byte 8″ Winchester or one 5¼″ floppy with a 10M-byte Winchester disk drive.

Expansion with the NDS-II network development system improves productivity as shared peripherals and data bases are needed. With NDS, the foreground or background task of one workstation can be dedicated to a specific function, freeing other stations in the network for user interaction.

Embedded in the iNDX operating system are file sharing and security features. The system logically groups data, connects volumes, and further divides volumes into directory or data files. This structure allows each file to be addressed by a path name, eliminating the need to know the physical location of a file

(continued on page 44)

CalComp introduces the MBA.

Every computer system has the business basics—accounting, finance, administration.

But when end users or OEMs add CalComp's M-84 plotter, their system becomes an MBA (Master of Business Art) that produces presentation-quality graphics for less than $2,000.

The M-84 actually makes your system a little smarter. It's based on the Z80 microprocessor and has built-in firmware for five line styles, selectable character rotation, six different character sets and circle, arc and sector generation. It can also work as a printer and digitizer.

M-84 is fast, precise and quiet. It plots at speeds up to 17.7 inches per second with resolution of .004 inches on paper or film for overhead projection.

M-84 is analytical and easy to maintain. Diagnostics test and report on interface and plotting functions on your command.

The M-84 is versatile. There are three standard interface models—Centronics, IEEE and RS-232, and most popular applications software packages, including ISSCO's DISSPLA and TELL-A-GRAF, SAS/GRAF and Digital Research CP/M-based Graphic System Extension.

Our M-84 is colorful—8 pens, 8 colors. The high number of pens means faster plots and easier operation because users won't have to switch pens to get more colors.

Don't wait to get your M-84. Call your CalComp representative today.

California Computer Products, Inc., M/S3, 2411 West La Palma Ave., Anaheim, California 92801. In continental U.S. except California, call (800) 556-1234, ext. 156. In California (800) 441-2345, ext. 156.

CALCOMP
A Sanders Graphics Company
SANDERS

System combines tools

(continued from page 42)

to address it. The file system also possesses protection mechanisms that allow read-only, read-write, or read-write-delete rights to protect files from unauthorized or accidental entry.

Software changes are controlled and documented under the software version control system (iSVCS). This tool stores and retrieves different versions of a given program module and controls update privileges. The iMAKE software generation system automatically compiles and links the most recent versions of specified modules into a system. This ensures that software is current and correct, and eliminates redundant steps.

Another time-saving feature, the AEDIT text editor lets users create macrocommands, display and scroll text on the video monitor, view lines more than 80 characters long, and insert and delete characters anywhere in a file. Text manipulation features allow strings of characters or blocks of text to be moved or copied within a file or from one file to another.

Optical debugging tools provide more power to traditional functions such as setting breakpoints or tracing execution flow. PSCOPE, an interactive symbolic debugging system for Pascal, PL/M, and FORTRAN projects, allows users to modify code during debug without recompiling. It also permits extensive tests and consistency checks to be done on programs and automates much of the testing.

In conjunction with the integrated instrumentation and in-circuit emulator (I^2ICE) system, the workstation supports full display of logic timing analyzer outputs. I^2ICE combines 12-MHz in-circuit emulation, high level language debugging, and 100-MHz logic timing analysis for improved productivity.

The development system supports high level languages such as PL/M, Pascal, and C, as well as macro-assemblers such as ASM86. The high level compilers produce code for the target processors and contain run-time floating point arithmetic support for the 8087 numeric processor.

There are six system configurations, four standalone and two networked workstations. The iMDX 430 WD standalone with two floppies and separate 8″ 35M-byte Winchester sells for $30,900. Incorporating an 8086 upgrade kit, this system sells for $34,900. The iMDX 430 WS network workstation has two floppy disk drives plus communication boards; it sells for $19,900. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 247

DATA COMMUNICATIONS

Voice/data terminal looks to future

With its personal communications terminal, Rolm Corp takes a major technological step toward implementing a digital desk. Tightly integrating voice and data devices, Cypress supplies high functionality at low cost.

Four basic components make up the Cypress terminal. The 9″ CRT screen displays 25 lines of 80 characters, plus a status line in 3270 mode. A dashboard contains separate groups that function as telephone dialing pad, soft function keys, line keys, configurable phone keys, terminal control keys, and phone function keys. The desktop unit also

(continued on page 48)

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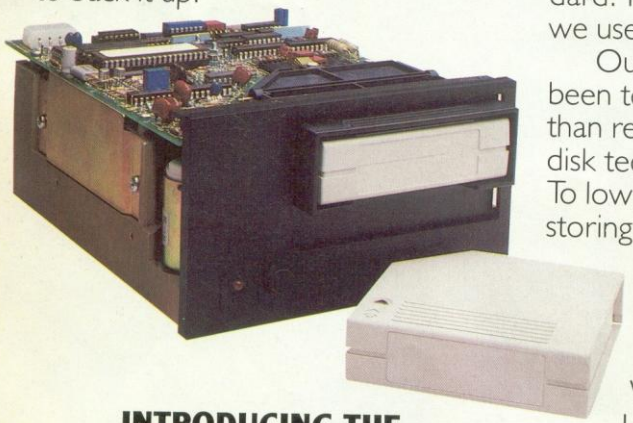
AND READ WITH US. AND DESIGN WITH US. AND DEPEND ON US.

Introducing the Tandon Tape Drive Company.

We're the newest of Tandon's advanced micro peripherals companies. Like all Tandon companies, we concentrate all our energies on a single related product line. And like them, we're dedicated to becoming the world's leading producer of what we make best.

That's a pretty brash goal for a company that just built its very first tape drive. But we have the product to back it up.



INTRODUCING THE TANDON TM951 TAPE DRIVE.

What's the world's biggest producer of micro peripheral disk drives doing in the tape drive business?

Building a half-inch tape drive with a capacity of 50 megabytes and an OEM price that's pure Tandon.

Everything about our streaming tape drive is pure Tandon. That's because we have the highest degree of vertical integration of any manufacturer in the business. Which means we can better control our costs and quality.

TO BUILD A DRIVE THIS GOOD, WE HAD TO USE OUR HEADS.

Tandon got its start as a head manufacturer. Our floppy heads quickly became the industry standard. Those are the very same heads we use on our new tape drive.

Our philosophy throughout has been to use evolutionary, rather than revolutionary, tape and floppy disk technology in our new drive. To lower costs and minimize risk for storing your back-up data.

That approach has paid off not only in a low price but also in high data reliability and performance. With a soft error rate of 1×10^9 and an MTBF of 8000 power-on hours.

FEATURES EVERYONE WILL WANT TO DUMP ON.

Our low cost and high reliability will help us become number one in disk back-up.

So will our drive's great features.

The TM951 is the same size as a standard 5¼" floppy drive. It records on half-inch tape on twenty tracks, arranged in a serpentine pattern, using standard MFM format. And dual heads allow instant data verification while writing.

We not only make the drives, we also make the cartridges. From a unique Tandon design, using a video-style, self-threading, single reel for high performance and reliability.

DISK BACK-UP THAT KEEPS COSTS DOWN.

Providing the most advanced technology at the lowest possible price has made all Tandon companies leaders in their fields.

That's exactly how we intend to succeed in ours.

Five years ago our floppy company was a newcomer in a highly competitive market. Today it's the world's leading supplier of 5¼" drives.

That success story gives us a lot to live up to. Which is just what we've set out to do.

For full information on the newest tape drive from the newest tape drive company, call us. It's your chance to dump on us before everyone else does.

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CIRCLE 26

Communications terminal
(continued from page 44)

Cypress, Rolm's personal communication terminal, combines functions of a smart data terminal and a digital telephone to supply simultaneous voice and data communication.

provides a digital telephone and a detachable alphanumeric keyboard that stows inside.

The unit can be used as a Digital Equipment Corp VT100 ASCII terminal. Connected through the Rolm IBM gateway, it operates in IBM 3270 environments. This gives users high speed access to a range of corporate and public data bases. A printer connects through the RS-232 port to provide permanent copies of the display. In addition to data communications, the concept offers a digital telephone that uses CBX telephone features plus augmented dialing and telephone messaging.

Because the terminal operates in conjunction with the CBX, simultaneous voice and data connection are possible using only a single twisted pair of standard telephone wire. The high speed digital communications path between desktop devices and the CBX is the Rolm link. Combining voice, data, control, and telephone power over the single twisted pair, the link operates at 256k bps, full duplex; 64k bps are used for digitized voice; 64k bps for data. The remaining bandwidth is used for control, error detection, and future enhancements. CMOS LSI chips at each end of the link perform all control and data transmission functions, and interface to industry standard codecs. The link operates at up to 3000′ (914 m). As a smart terminal, Cypress offers data rates ranging from 110 to 19.2k bps. Rates are set automatically. Hardware and software features furnish backup and reload in the event of a power failure.

All personal data—such as terminal profile and auto-log sequences—are stored in 8K bytes of nonvolatile RAM. This RAM is a portable module that can be taken out and placed in another unit, eliminating the need to reenter personal data when changing terminals.

Program code for applications resides in 128K bytes of dynamic RAM. This memory is battery powered for approximately 5 min should power failure occur. Operation can be restored to exactly the same state if power returns within that time. The telephone portion of the unit is powered from the CBX.

The digital phone allows voice calls to be dialed or received even while the terminal is receiving data from a data base or interacting with a computer. Users can connect to a computer while carrying on a telephone conversation. Information is displayed on the terminal's screen with no interruption of voice communication.

Available toward the end of this year, Cypress has a single-unit price of $1950. **Rolm Corp**, Office Systems Div, 4900 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 248

The Alps Advantage in keyboards:

Keyboards for modern product design. When you bring your keyboard requirement to Alps, you'll find yourself in good company, alongside many of the most prestigious OEM industry names in the world. From single key switches to complete keyboard units including matrix and encoder circuits, you'll discover the quality, reliability and customer service that have become such important parts of The Alps Advantage, together with everything you need to sharpen the competitive edge of your products:

Full-travel keyboard units. Standard or customized designs, mechanical or conductive rubber contacts, soft-push or tactile feedback with "snap" or "click" feeling.

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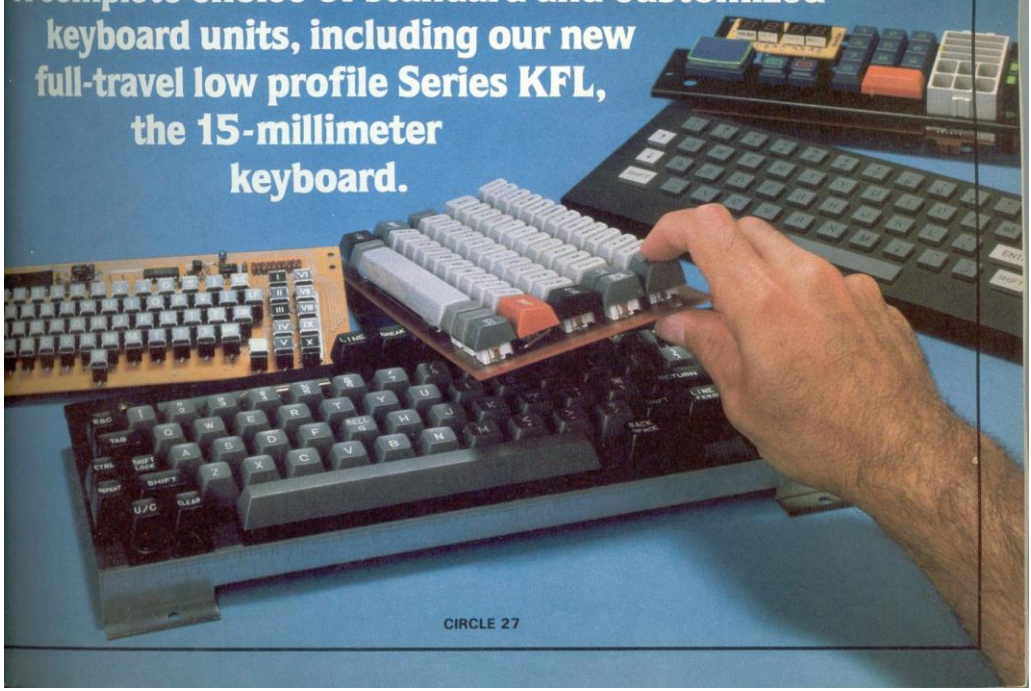


CIRCLE 27

Leapfrog

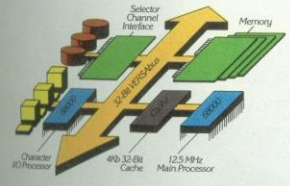
to 32 bits!

The 32-Bit Advantage

For OEMs and system integrators, getting the jump on the competition means leapfrogging to the most advanced technology available. Today, that means making the jump to 32-bit architecture. Now. When it can give you a decisive advantage.

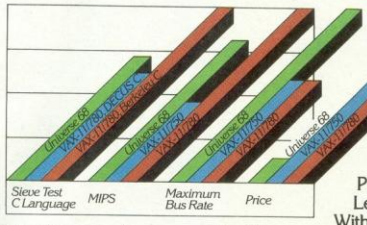
32-Bit Memory on a 32-Bit Bus

The Universe 68/05 is a true 32-bit system because it handles 32-bit data transfers in parallel on its 20Mb/sec VERSAbus, while most 68000-based machines are still limping along with 16-bit buses. With the next generation of processors (like the MC68020), a full 32-bit bus will be a requirement on *all* systems. VERSAbus is there now, and it's non-proprietary.



32-Bit Cache, 12.5MHz 68000

Our new Universe 68/05 is the first commercial product built *and delivered* using the new 12.5MHz 68000 microprocessor. Its 4Kb 32-bit cache memory virtually eliminates wait states, while a separate 68000 I/O processor offloads the main 68000. Its MIPS rate—1.25 million instructions per second—outstrips a VAX 11/750 that costs several times as much.



Universe 68 provides performance comparable to VAX, at a price far below VAX.

32/64-Bit Hardware Floating Point

Our new IEEE-format hardware floating point unit handles 32- and 64-bit operands fast. In fact, with floating point performance in the 40-50K flops range, it holds its own very nicely with VAX-level machines. Yet the Universe 68's price tag is only a fraction of a VAX's.

The First 32-Bit System Under $10,000

The Universe 68/05's under-$10,000 OEM-quantity-one price includes 32-bit central processor, 10Mb Winchester, 1.26Mb floppy, 256Kb RAM (expandable to 3Mb), and four serial I/O ports (expandable to 64). You can build multiterminal systems around a 68/05 at a cost-per-user that will embarrass workstation systems. For even more horsepower and expandability, you can hop over to the compatible Universe 68/37 or 47.

The 32-Bit, Real-Time, Bell UNIX

UNOS, our multi-user, multi-language operating system, brings real-time, transaction-oriented capabilities to the UNIX-compatible world. And UNOS now runs Bell-licensed UNIX System III tools for development. Plus Fortran, RM/COBOL, BASIC, Pascal, C, and DBMS.

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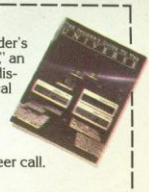
UNIX™ NOW RUNS ON UNOS™

☐ Send me "The Insider's Guide to the Universe," an informative 24-page discussion of the technical concepts behind the Universe 68 family of computers.



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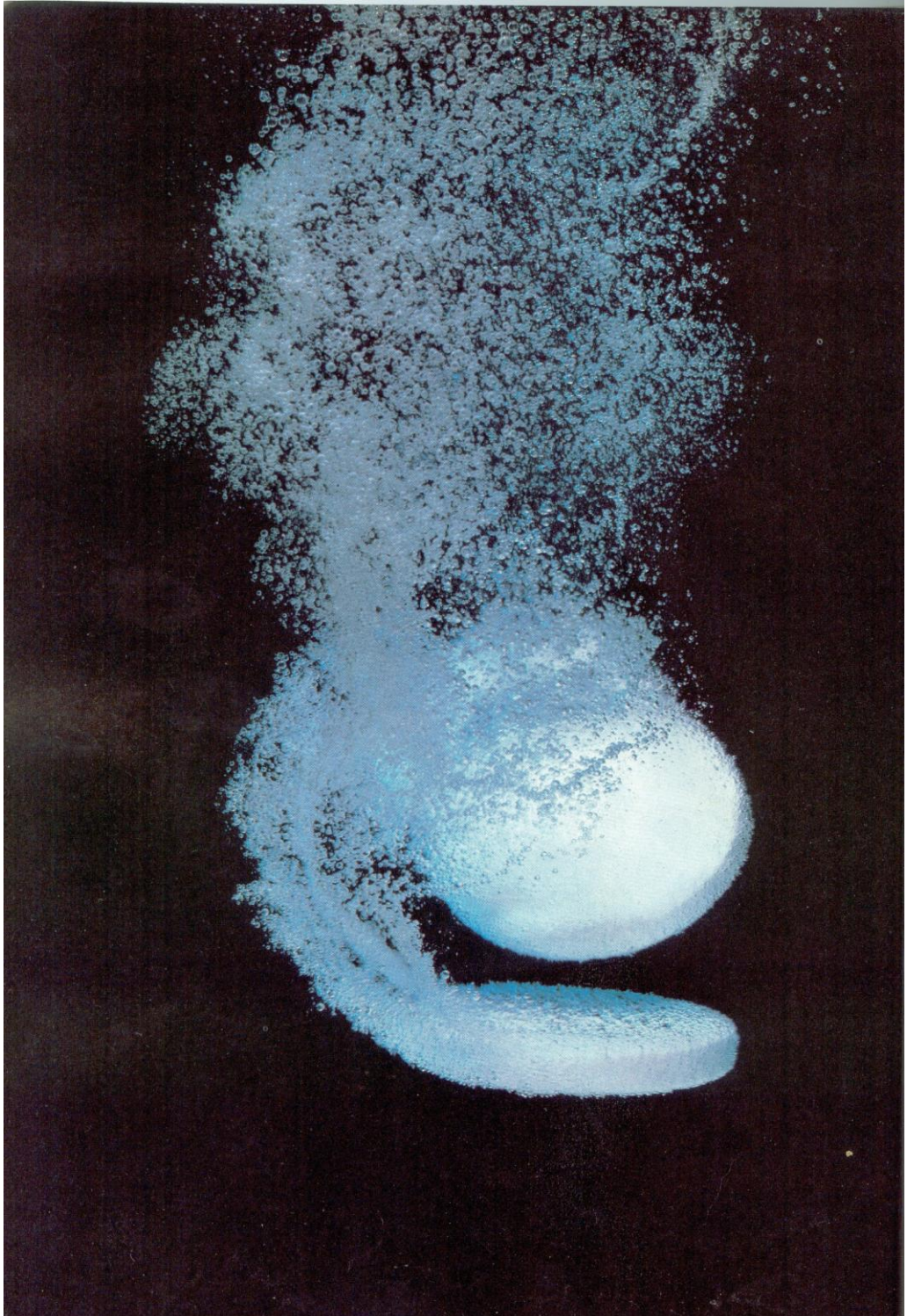
CHARLES RIVER DATA SYSTEMS

CIRCLE 28



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CIRCLE 29

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Midcon/83

Electronic Show and Convention

O'Hare Exposition Center
Rosemont, Illinois
September 13 to 15, 1983

This year Chicago will again play host to Midcon, the Midwest's largest and most comprehensive high technology convention. Over 25,000 OEMs engaged in the design, manufacture, and test of electronic components and systems are expected to cover nearly 550 exhibition booths representing leading U.S. electronics companies. In addition, for the first time Midcon attendees will converge at their own local version of the Mini/Micro convention. As a sister show, Mini/Micro-Midwest (see p 66) will run concurrent with—but separate from—Midcon.

The quest for high speed, low power, and cost efficiency will beckon many system integrators to Midcon, particularly those in the data communications field. Innovative ideas and new, workable hardware/software implementations in communications take up 8 out of 22 scheduled Professional Program sessions set for the Midcon convention.

Networking has become a pivotal point for the future of data communications. Now, projected traffic growth dictates the need for increasingly efficient, fast, and low cost architectural alternatives. Professional Program Session 3 will focus on available networking systems, including distributed processing LANs. The topic will be fine tuned with talks on performance analysis models and communications protocols for local and satellite networks.

Session 12, "Data Communications/Networking for Microprocessor Based Systems," will explain how, as more functions are integrated onto VLSI chips and microprocessor design is simplified, more complex LAN systems can be designed without losing application targets or user friendliness. Specific hardware to be analyzed includes the SC68562 dual-universal serial controller, the NEC 7201 LSI communications controller, and a processor friendly IEEE 802 CSMA/CD controller, along with communications applications for the MC68000 family.

LSI modem components that can be directly integrated into the host product save money and increase reliability. In fact, selecting the right modem is becoming crucial to effective communications today. Aimed at data communications specialist and nonmodem design engineer alike, Session 14 will give background information on LSI signal processing components, intelligent 212A-type modems, 1.2k-bps LSI modem ICs, and a Unit-A single-chip microprocessor with onboard telecommunications interface.

Enhanced telecommunications, the result of the integrated services digital networks (ISDNs), can be supported only by corresponding silicon capability—from bipolar through MOS VLSI circuits. Such a stipulation will be addressed during Session 18, when specialists take the floor to discuss advanced generation integrated SLIC, digital telecommunications systems implemented in silicon, CMOS LSI applications for voice and data networks, upgrading ISDNs through enhanced feature analog SET, and total silicon subscriber to subscriber networks.

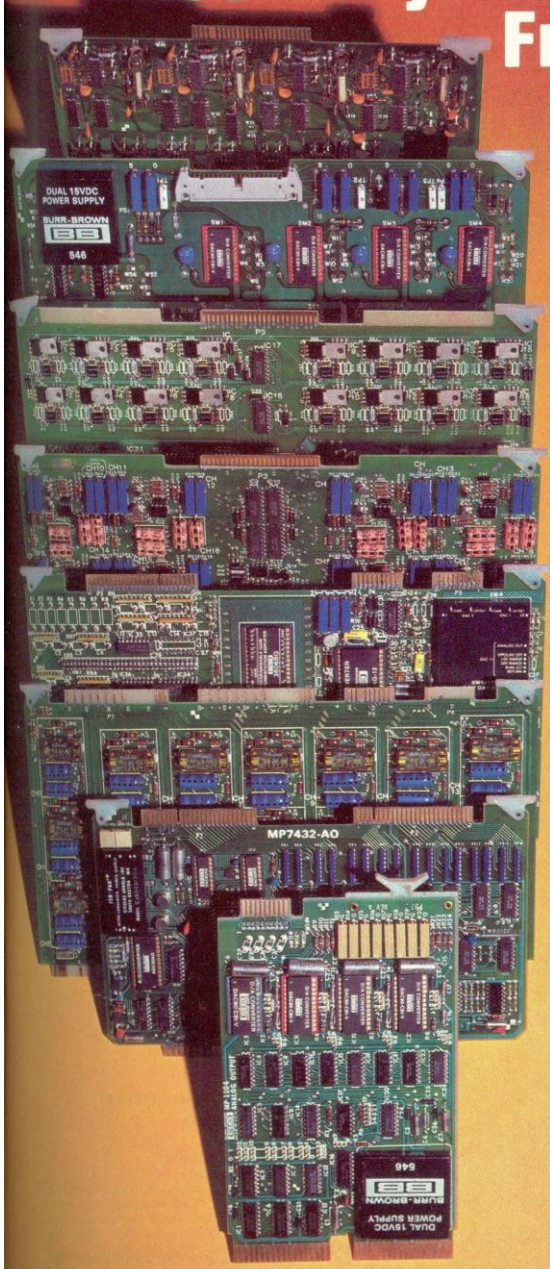
Session 6 will focus on silicon news, investigating the new processes that are changing semiconductor technology year by year. Microprocessor shrink methodology and its resulting process conversion benefits to the chip manufacturers and gains to the end product consumer will be explored. New inks and equipment, such as additive circuitry using polymer thick film and applications for infrared systems to both cermet and polymer thick films, will be analyzed for this growing market's trends and users.

Logic design is another technology driven by high speed, low power, and cost efficiency requirements. Logic circuitry, including the CMOS discrete family, will be compared to design concepts for the next generation logic systems. Recent advances in MOS technology will also be attributed to increased circuit complexity, higher levels of integration, lower costs, and decreased power consumption. Meeting these primary specs, new digital VLSI hardware can be developed to take over a variety of digital signal processing tasks. Session 16 cites the TMS32010 for speech processing and the 7720 (SPI), along with a 16-bit CMOS ALU slice and a digital signal microcomputer.

For registration information, contact Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965; 800/421-6816 (outside Calif)

(continued on page 56)

60+ Ways To Get I/O Data From Sensors to μC Bus... Easily



More than 60 different analog/digital I/O boards provide a variety of off-the-shelf, plug-in quick solutions for sensor-to-microcomputer bus compatibility. Designed - proven in Intel Multibus™, Motorola Micromodule, DEC LSI-11 and Zilog MCB/MCS (and others), these boards offer the important features that save you time and money.

ALL BOARDS FEATURE . . .
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- Simple operation - most boards can operate with one instruction - powered from standard system bus

ANALOG INPUTS WITH . . .
- 8 or 12 bit resolution - ±10 millivolt to ±10 volt range
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- Dedicated 16-channel RTD board with excitation and lead length compensation

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- 12 bit resolution and voltage or current output
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DIGITAL INPUTS AND OUTPUTS WITH . . .
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NEW TIMING FUNCTION BOARD has optical isolation and optional input debouncing . . . up to 15 channels, 16 bits per card . . . software programmable cascading of counters up to 80 bits. Use for clock, pulse counting, pulse frequency and pulse-width measurements. 60+ boards are described in a new Microcomputer I/O Board Brochure . . . ask for it!

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CIRCLE 30

(continued from page 54)

Professional Program Excerpts*

Session 1: Engineering Workstation Requirements for Systems, PC Board, and IC Design Engineers

Tues 9:30 to 11:30 am

Chair: D. Laughlin, CAE Systems, Inc

1/1 "Understanding the Problem"
D. Laughlin, CAE Systems, Inc

1/2 "Workstations for Professionals"
D. Nelson, Apollo Computer, Inc

1/3 "An OEM Workstation"
A. Wallack, Masscomp

1/4 "A Standalone VLSI Workstation"
T. Smith, Metheus Corp

1/5 "A CAD/CAM System for PC Boards"
J. Sliwkowski, Telesis Systems Corp

Session 2: Diagnostics

Tues 9:30 to 11:30 am

Chair: R. B. Silverman, SEI Information Technology

2/1 "Resident Diagnostics on Fault Tolerant Systems"
W. G. Bartels and R. W. Carlson, SEI Information Technology

2/2 "Resident Diagnostics on Coil Winding Equipment"
C. Goodin, Bachi, Inc

2/3 "Resident Diagnostics on Telecommunications Terminals"
A. Miotke, Extel Corp

Session 3: Trends in Communications Networking and Control Protocols Experience

Tues 9:30 to 11:30 am

Chair: S. Kota, Ford Aerospace & Communications Corp

3/1 "Distributed Processing Design Concept Based on LAN Technology"
P. Meng and W. Tan, Transaction Technology Inc

3/2 "Performance Analysis of Contention Techniques for 2-Hop Packet Networks"
R. Sherman, Ford Aerospace & Communications Corp

3/3 "Protocol Standards for Local and Internetworking"
Y. Jayachandra, Intel Corp

3/4 "Guaranteed Data Distribution Management over a Computer Network"
V. Bhave, Tandem Corp, Inc

3/5 "VLSI Based Distributed Control System Architecture for Digital Telecommunications"
B. Lusignan, A. S. Badawi, and S. Al-Wakeel, Stanford Univ

Session 4: Computer Aided Design of Integrated Circuits

Tues 1 to 3 pm

Chair: K. Housley, American Microsystems, Inc

4/1 "An Integrated CAD System for Gate Array Design"
J. M. Geyer, General Electric Microelectronics Center

4/2 "Tools for User Designed VLSI"
B. Duyn, VLSI Technology, Inc

4/3 "A Unified Approach to Custom and Semicustom VLSI Design"
J. C. Shovic, American Microsystems, Inc

4/4 "Applying CAD to the Engineering Design Cycle"
D. Laughlin, CAE Systems, Inc

4/5 "Automatic Implementation of Self-Timed State Machines in Integrated Circuits"
T. M. Carter, Univ of Utah

Session 6: Shrinking Microcomputers onto New Processes Yields New Benefits

Tues 1 to 3 pm

Chair: A. Toth, Intel Corp

6/1 "Microprocessor Shrink Methodology"
P. Secor, Advanced Micro Devices

6/2 "Process Shrinks and the Benefits from Them"
A. Toth, Intel Corp

6/3 "Process Technology Combines with Macro-Cell I/O to Benefit Both Customers and Manufacturers"
S. Groves, Motorola MOS Group

6/4 "Advancing Technologies Bring Increased Integration, Faster Execution, and Lower Cost"
E. Powell, Texas Instruments Inc

Session 7: Hybrid Thick Film Manufacturing

Tues 4 to 6 pm

Chair: M. Eeg, Research, Inc

7/1 "Developments in Additive Circuitry Using Polymer Thick Film Materials"
W. Green, Methode

7/2 "New Formulations for Cermet and Polymer Thick Films"
D. Olerg, ESL

7/3 "Infrared Systems for Cermet and Polymer Thick Films"
M. Eeg, Research, Inc

7/4 "Automatic, Inline Screen Printing"
C. Brown, American Microsystems, Inc

*Professional Program sessions are subject to last-minute changes.

(continued on page 58)

(continued from page 56)

Session 9: New Generation Logic Circuitry for High Performance Systems

Tues 4 to 6 pm

Chair: S. Dunn, Motorola, Inc

9/1 "Comparison of High Performance Logic Family"
B. Chao, Supertex, Inc

9/2 "Designing Tomorrow's Systems with High Speed Logic"
J. King, Motorola, Inc

9/3 "Design Concepts for Next Generation Logic Systems"
A. Gruszynski, GTE Microcircuits

9/4 "CMOS Discrete Logic Family"
D. Goodpaster, Texas Instruments Inc

Session 12: Data Communications/ Networking for Microprocessor Based Systems

Wed 9:30 to 11:30 am

Chair: C. M. Collins, Motorola, Inc

12/1 "SC68562 Dual Universal Serial Communications Controller—an Advanced Communications Circuit"
J. Magill, Signetics Corp

12/2 "Application for an LSI Data Communications Controller—NEC 7201"
R. Spears, NEC Electronics USA, Inc

12/3 "A Processor Friendly IEEE 802 CSMA/CD Controller with General Purpose Applications"
H. Logan and E. Lare, Rockwell Electronic Device Div

12/4 "Data Communication Solutions for the MC68000 Family"
J. Vaglica, Motorola, Inc

Session 13: Local Area Networks: Theory and Technologies

Wed 1 to 3 pm

Chair: A. Faro, Centro Di Calcolo, Ingegneria Catania

13/1 "Communication Architectures for Local Area Networks"
A. Faro, Centro Di Calcolo, Ingegneria Catania

13/2 "Management Architectures for Local Area Networks"
G. Messina, Instituto Di Informatica e Telecomunicazioni

13/3 "A Local Network for Industrial Automation"
A. Serra, A. Valenzano, C. DeMartini, and L. Vita, Politecnico Di Torino

13/4 "PABX and Local Networks"
M. Bozzetti, Italtel Telematica Milano

13/5 "Interconnections between Telematics Services and Local Networks"
G. De Luca, Olivetti Telecom

Session 14: Advances in LSI Modem Components

Wed 4 to 6 pm

Chair: S. J. Durham, Cermetek Microelectronics, Inc

14/1 "Implementation of LSI Signal Processing Components for Modems"
Y. Haque, American Microsystems, Inc

14/2 "Intelligent 212A Type Modem Components"
S. J. Durham, Cermetek Microelectronics, Inc

14/3 "New 1200-bps LSI Modem Integrated Circuits"
J. Lange, J. C. Sundell, EXAR Integrated Circuits, Inc

14/4 "The Communications Terminal Unit—a Single-Chip Microprocessor with Onboard Telecommunications Interface"
A. Gruszynski, GTE Microcircuits

14/5 "Data Communications Systems in Silicon"
D. Taylor, Advanced Micro Devices

Session 16: Hardware Implementation Alternatives in Digital Signal Processing

Thurs 9:30 to 11:30 am

Chair: V. R. Ranganath, Synertek

16/1 "Floating Point Processing Hardware"
J. Haight, TRW

16/2 "Low Cost Speech Processing with TMS32010"
L. Kaplan, Texas Instruments Inc

16/3 "A Digital Signal Microcomputer"
G. Ramachandran, Fujitsu Microelectronics

16/4 "A 16-Bit CMOS ALU Slice"
J. Larsen and V. Arat, Synertek

16/5 "DSP Applications Using 7720 (SPI)"
V. Jordan and W. Meshach, NEC Electronics

Session 17: Surface Mounted Devices

Thurs 9:30 to 11:30 am

Chair: J. J. Lightner, Lightner Assocs, Inc

17/1 "New Semiconductor Packages Facilitate Automated Surface Mount Assembly"
E. E. Baxter and A. Collins, Motorola, Inc

17/2 "Advantages of Chip Capacitors Relating to Surface Mounting Technology"
J. Sarvis, AVX Corp

17/3 "Latest Advances in Leadless Placement Technology"
N. McLean, Emhart Corp

17/4 "Automated SMD Printed Circuit Board Assembly"
L. Leicht and D. Derfiny, Motorola, Inc

(continued on page 60)

WINCHESTER BACKUP/ DATA BASE MANAGEMENT!

Model 451 — serpentine write
Model 450 — standard write

Back-up your Winchester with the new Model 450 or 451 cartridge tape drive. With the capability of a full tape peripheral, the new Qantex drive can be used to perform file search, update records, and edit/reformat data.

Designed for disk backup as well as archival storage or data logging applications, the 450/451 packs 17.2 megabytes on a single data cartridge, with a packing density of 6400 bpi and 192,000 bits per second transfer rate.

Both models incorporate a rugged transport mechanism with a precision servo motor. Model 450 offers a standard, and Model 451 a serpentine recording head. Read-after-write dual gap and selective erase are standard features of both models.

The serpentine tape drive features a special read-after-write recording head that provides bi-directional tape operation avoiding time-consuming rewind time.

The new Model 450/451 is available now! Contact us today for complete details!

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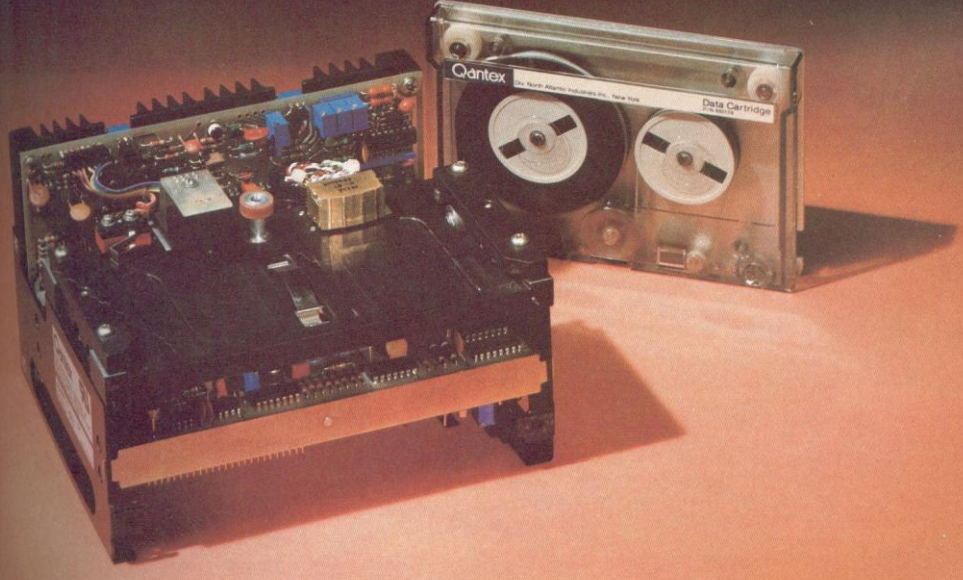


CIRCLE 32

(continued from page 58)

Session 18: Multiple Silicon Technologies Support Enhanced Telecommunications Services

Thurs 1 to 3 pm

Chair: B. Bowden, Intel Corp

18/1 "Advanced Generation Integrated SLIC"
P. J. Meza, Harris Corp

18/2 "Partitioning Digital Telecommunications Systems for Implementation in Silicon"
L. Thurlow, Mitel, Inc

18/3 "Total Silicon—Subscriber to Subscriber"
A. Ugge, SGE-ATES

18/4 "The Impact of CMOS LSI on Voice and Data Networks"
A. Mouton, Motorola, Inc

18/5 "Enhanced Feature Analog SET Supports ISDN Upgradability"
F. H. Cherrick, Intel Corp

Session 19: Process Control (I)—from Oil Field to the Modern Factory

Thurs 1 to 3 pm

Chair: B. Abernethy, Texas Instruments Inc

19/1 "Display Technology for Industrial Process Control—Current Status and Future Trends"
G. Ligler, Aydin Controls

19/2 "Using Local Area Networks for Industrial Process Control"
M. Webb, Intel Corp

19/3 "Applications of Artificial Intelligence to Industrial Process Control"
J. Dreussi, Texas Instruments Inc

19/4 "Sensor Technology for Industrial Process Control—Status and Future Trends"
W. Frost, Rosemount, Inc

Session 20: Videotex Systems—Low Cost Terminal to Information Providers

Thurs 1 to 3 pm

Chair: T. Vance, Quazon Corp

20/1 "Videotex Terminal Requirements Now and in the Future"
T. Vance, Quazon Corp

20/2 "The Shape of Videotex Systems Today and Tomorrow"
A. R. Haimes, SysDes, Inc

20/3 "Frontend Data Processing Requirements"
A. Cuesta, Telematics International

20/4 "The Network—Videotex Applications"
R. Raucci, Graphic Scanning Corp

Session 21: Signal Processing Technology for Digital Audio

Thurs 4 to 6 pm

Chair: R. R. Yamashita, TRW LSI Products

21/1 "Commanded Predictive Delta Modulation: a New Technique for Digital Recording"
R. W. Adams, dbx Inc

21/2 "PROM-Corrected DAC for Digital Audio"
S. Sockolov, Intersil

21/3 "Digital Recording Techniques for Magnetic Tape"
R. J. Youngquist, 3M Corp

21/4 "The Use of Floating Point Arithmetic in Digital Filters and Equalizers"
F. A. Williams, TRW LSI Products

Session 22: Process Control (II)—from Oil Field to the Modern Factory

Thurs 4 to 6 pm

Chair: J. Dreussi, Texas Instruments Inc

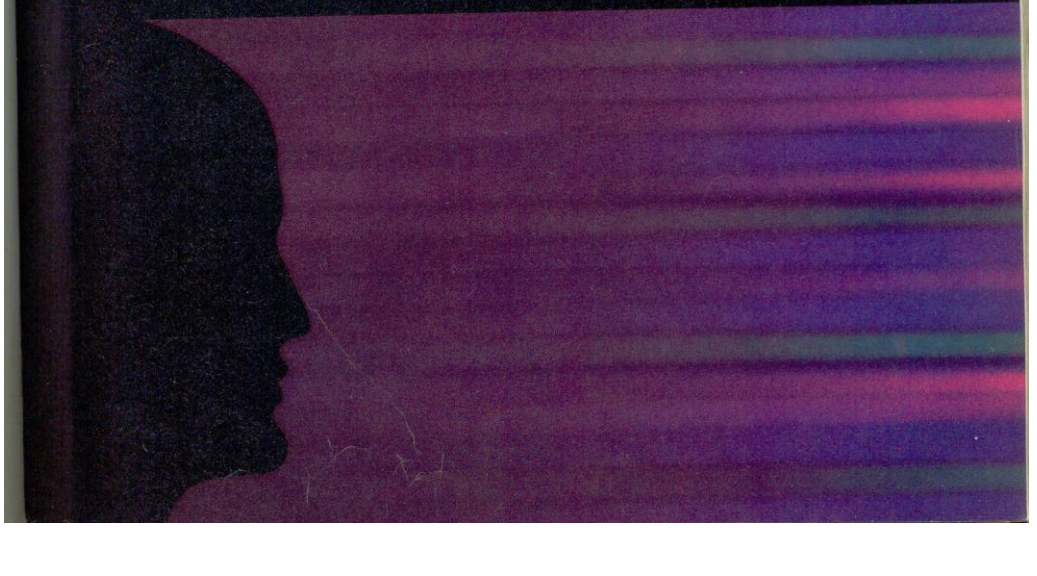
22/1 "Integration of Computer Aided Design with Computer Aided Manufacturing for Total Plant Automation"
D. Ameen, General Electric

22/2 "Present State and Future of Fault Tolerance Technology in Industrial Process Control"
J. Binder, August Systems

22/3 "Robotics and Process Control: Current Status and Future Trends"
J. Gage, Advanced Robotics

22/4 "Application of Process Control Technology to Oil Field Automation"
B. Abernethy, Texas Instruments Inc

Introducing the first array processor to break the $2,000/MFLOP barrier.



The FPS-5000 Series fro

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words are available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the FPS-5000 Series sets a new standard for cost-effective computing, breaking the $2,000 per MFLOP* barrier—the first time this has been achieved in any floating-point computing system.

*Based on U.S. Domestic Prices

Typical performance examples of geophysical, medical imaging an signal/image processing applications.

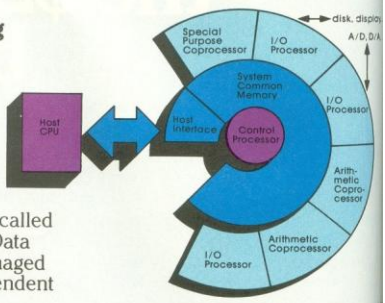
Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation/Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25.0 sec.	16 sec.	12 sec
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 se
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 mse

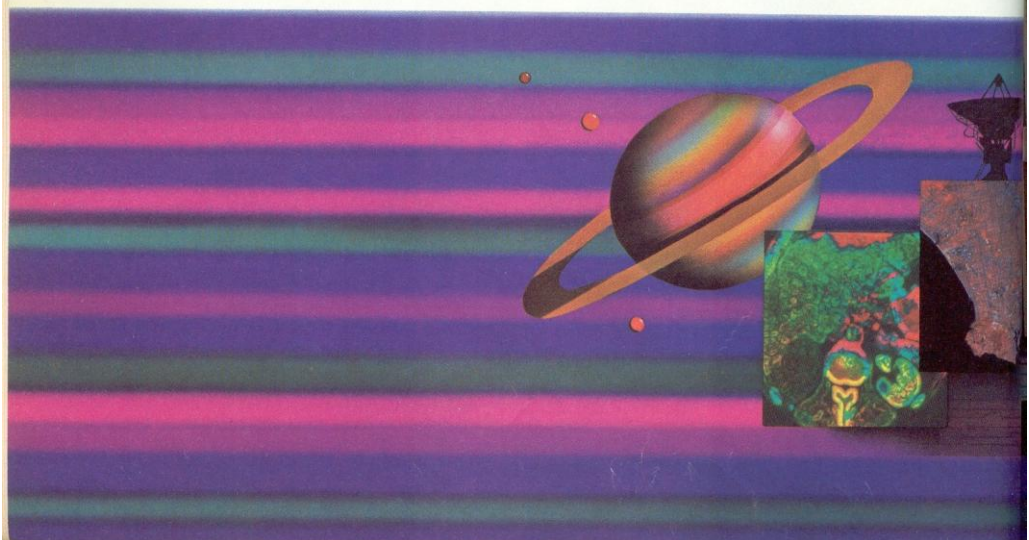
Based upon specifications subject to change.

Distributed processing architecture

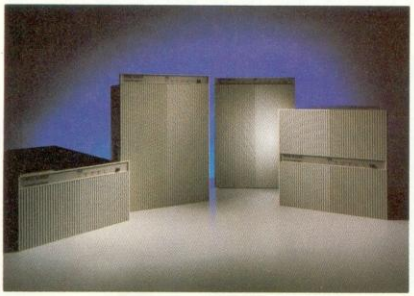
The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called Arithmetic Coprocessors. Data flow is simultaneously managed by a combination of independent I/O Processors and the central Control Processor.

FPS-5000 Series Architecture





Floating Point Systems.



Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

The new Multiple Array Processor Execution Language (MAXL), based upon FORTRAN 77, allows the user to construct an integrated system environment which can be tuned to application requirements.

Increased performance can be achieved by adding Arithmetic Coprocessors as a field-installable upgrade as the user's requirements evolve.

Compatibility

The FPS-5000 Series maintains software compatibility with previous FPS 38-bit processors and is supported on a range of host computers. Thus, the extensive software support developed for FPS-100 and AP-120B products is maintained and users are able to move existing applications onto the FPS-5000 Series with minimal effort.

Quality and Reliability

The FPS-5000 Series was designed and built with the same quality standards inherent in all of the previous Floating Point Systems products—standards that have earned those products a reputation for unprecedented reliability and one of the best meantime between failure (MTBF) rates in the industry.

The Series is backed by the same outstanding worldwide support services that distinguish Floating Point Systems from other manufacturers.

For more information about how the FPS-5000 can be used in your specific application, call (800) 547-1445 or your local sales office.

The world leader in array processors.

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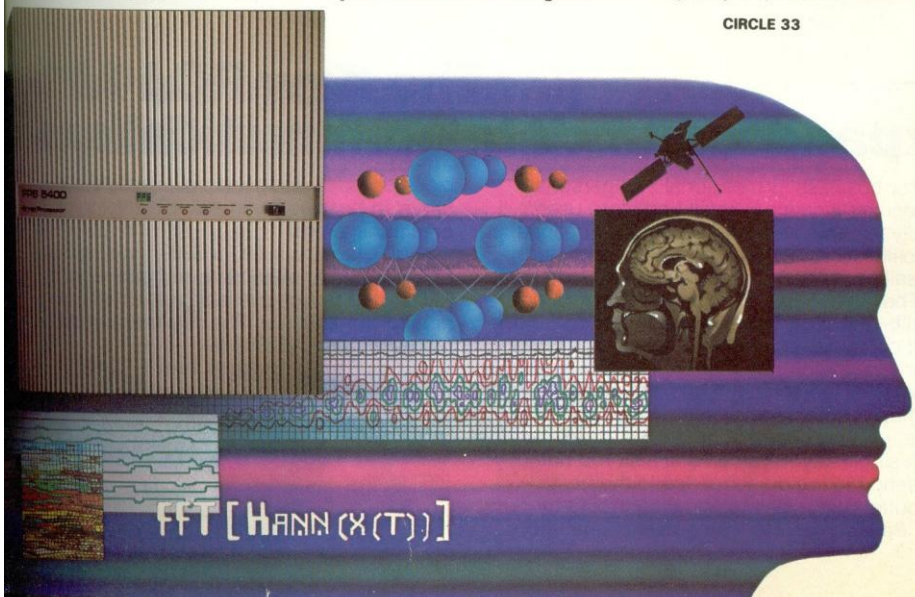
CIRCLE 33



Expensive.

The new RCA APT expands your data communications

For business, professional and personal data communications, you'll find more user-friendly features and greater communications capabilities in the RCA APT than in other terminals selling for up to three times the price.

The new APT terminals are ideally suited to multi-data base time sharing and dedicated, direct computer-connected applications. They feature menu-controlled operation and a programmable "personality" to match specific communications requirements for your data bases.

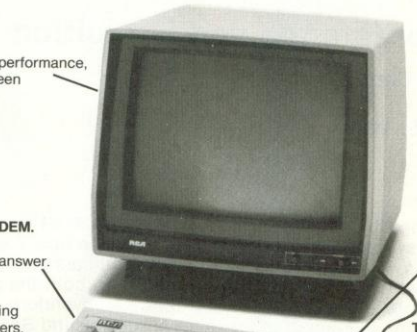
A single keypress can dial a stored number, send the log-on sequence to the host computer, and return terminal control to the user. Password protection prevents unauthorized access to designated numbers. APT can also be used as an auto-dialer for voice communications.

APT terminals list for $399, in your choice of full stroke or membrane keyboard versions. Either style is also available with a display monitor for $598 list. The data display monitor alone, VP3012D,$229 list.

OEM and dealer pricing available.

APT VP3801. Flexible membrane keyboard version designed for travel and hostile environments.

Expansive.



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CIRCLE 34

Mini/Micro Midwest

Computer Conference and Exhibition

O'Hare Exposition Center
Rosemont, Illinois
September 13 to 15, 1983

Mini/Micro-Midwest is set as the Chicago area's first forum specially geared to system design integrators, software specialists, and corporate management analysts. Being held in apposition to Midcon (see p 54), Mini/Micro-Midwest expects to unveil the most advanced computer related products and services before over 10,000 members of the electronics corps. Fourteen seminars, presented by over 60 authorities from business and industry, will be held as part of the show's Professional Program. These seminars are scheduled to eliminate overlap of similar interest areas within both Mini/Micro's and Midcon's Professional Program sessions.

Looking to the future is the behind-the-scenes impetus for each Mini/Micro Professional session. The next generation single-chip microcomputers will be shown as a by-product of recent innovations in semiconductor processing. During Session 1, specialists from five top electronics firms will spell out which unique microcomputer functions may lead to the most flexible, cost-effective systems. Timing and serial I/O for single chips will be analyzed for economic benefits. High density CPU migration via CMOS technology will be discussed, and HMOS and CMOS technologies cited for application excellence in high performance, chip-level microcomputers. Cost effectiveness and design-in capabilities for the single-chip micro will be explored via such avenues as the 8096 16-bit microcontroller and the low cost TMS 7000 microcomputer architecture during Session 3.

More designers are demanding 16/32-bit microprocessors with memory management and virtual memory capabilities for developing multi-user, multitasking systems. This year, microprocessor technology is allotted three sessions. Virtual memory systems using Motorola's MC68010, National Semiconductor's 16000, Zilog's Z8003, and Intel's iAPX 286 will be shown to provide memory schemes that rival those of more expensive microcomputers.

A survey of 16-bit microprocessor operating systems for the Intel 8086, Motorola 68000, and Zilog Z8000 will also cover software products available from both the processor manufacturers and third-party vendors. Future systems design is the thrust behind Session 12's discussions, which will anticipate hardware/software problems that can be solved by properly planning an upwardly compatible system.

Many development tools are currently available for the individual designer of 16-bit microprocessor based products. Session 13 evaluates low cost development tools for National Semiconductor's NS16000 and low end development tools for Zilog's Z8000. Speakers will also compare the benefits and uses of evaluation tools vs development tools. Then, of course, a microprocessor based system needs its peripherals. Session 14 will usher in new era LSI/VLSI technologies that are revising the catalog of advanced peripherals, including families of VLSI CRT and disk controllers.

Mini/Micro-Midwest also turns to a topic that has increasingly become of paramount importance to firms developing leading edge products. Software piracy and the resultant need for software security to protect investments is the topic of Session 11. Rounding out the Professional Program will be overviews of emerging graphics standards, database management systems, Pascal applications, and personal computers in the office environment.

For registration information, contact Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965; 800/421-6816 (outside Calif)

(continued on page 68)

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CIRCLE 35

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(continued from page 66)

Professional Program Excerpts*

Session 1: Advancing Technology Results in Unique Microcomputers

Tues 1 to 3 pm

Chair: M. Virts, Motorola, Inc

1/1 "Microcontrollers in Lab Environments"
S. Barton, Intel Corp

1/2 "New Timing and Serial I/O Techniques for Economic Single Chips"
B. Huston, Motorola, Inc

1/3 "High Density CPU Migration with CMOS Technology"
D. Zrebsky, National Semiconductor Corp

1/4 "Operating Systems for 16-Bit Microprocessors"
B. Williams, Zilog, Inc

1/5 "High Performance Single-Chip Microcomputers in HMOS and CMOS Technologies"
J. C. Campbell, NEC Corp

Session 2: Virtual Memory for 16/32-Bit Microprocessors

Tues 1 to 3 pm

Chair: M. A. Davidson, Motorola, Inc

2/1 "A Virtual Memory System Using the MC68010"
M. W. Moy, Motorola, Inc

2/2 "Virtual Memory with the 16000"
S. R. Mateosian, National Semiconductor Corp

2/3 "Virtual Memory with the Z8003"
S. Sandesara, Zilog, Inc

2/4 "Virtual Memory with the iAPX 286"
J. Crawford, Intel Corp

Session 3: Cost-Effective Design Solutions for Single-Chip Microcomputers

Tues 4 to 6 pm

Chair: M. Virts, Motorola, Inc

3/1 "8096 16-Bit Microcontrollers"
S. Barton, Intel Corp

3/2 "Advancements in Silicon Create Broad Applications Capabilities"
E. Peatrowsky, Motorola, Inc

3/3 "Developing Applications for Low Cost Microcomputer Architectures"
T. Harper, National Semiconductor Corp

3/4 "Cost-Effecitve Single-Chip Microcomputers from the TMS 7000 Product Family"
T. Schmidt, Texas Instruments Inc

3/5 "Advanced CMOS Microcomputer Family for Cost-Effective Design Solutions"
J. Fattal, NEC Corp

*Professional Program sessions are subject to last-minute changes.

Session 4: Operating Systems for 16-Bit Microprocessors

Tues 4 to 6 pm

Chair: D. Kusch, Zilog, Inc

4/1 "Operating System Features of the 16-Bit Z8000"
F. Zlotnick, Zilog, Inc

4/2 "Developing Silicon Standards for Realtime Operating Systems"
M. S. Ursino, Microsoft

4/3 "VRTX, a Standard Realtime Operating System Component for 16-Bit Microprocessors"
J. F. Ready, Hunter and Ready, Inc

4/4 "Modular Operating System Design with the RMS68K"
D. Leitch, Motorola, Inc

4/5 "Developing Silicon Standards for Realtime Operating Systems"
R. J. Slamp, Intel Corp

Session 5: Graphics for the '80s

Wed 9:30 to 11:30 am

Chair: M. Shapiro, NCR Corp

5/1 "A Unique VLSI Architecture for Graphics"
D. Henderson, NCR Corp

5/2 "TI's New VDP Family Offers Low Cost Graphics System"
B. Williamson, Texas Instruments Inc

5/3 "Applications of High Performance Instrumentation Graphics"
A. Smith, Hewlett-Packard Co

5/4 "Intel's 82730 Text Coprocessor"
B. May, Intel Corp

Session 6: Advances in Database Management Systems

Wed 9:30 to 11:30 am

Chair: A. K. Arora, Illinois Institute of Technology

6/1 "Design of Views in Relational Database Systems"
A. Pahwa, Bell Labs and A. K. Arora, Illinois Institute of Technology

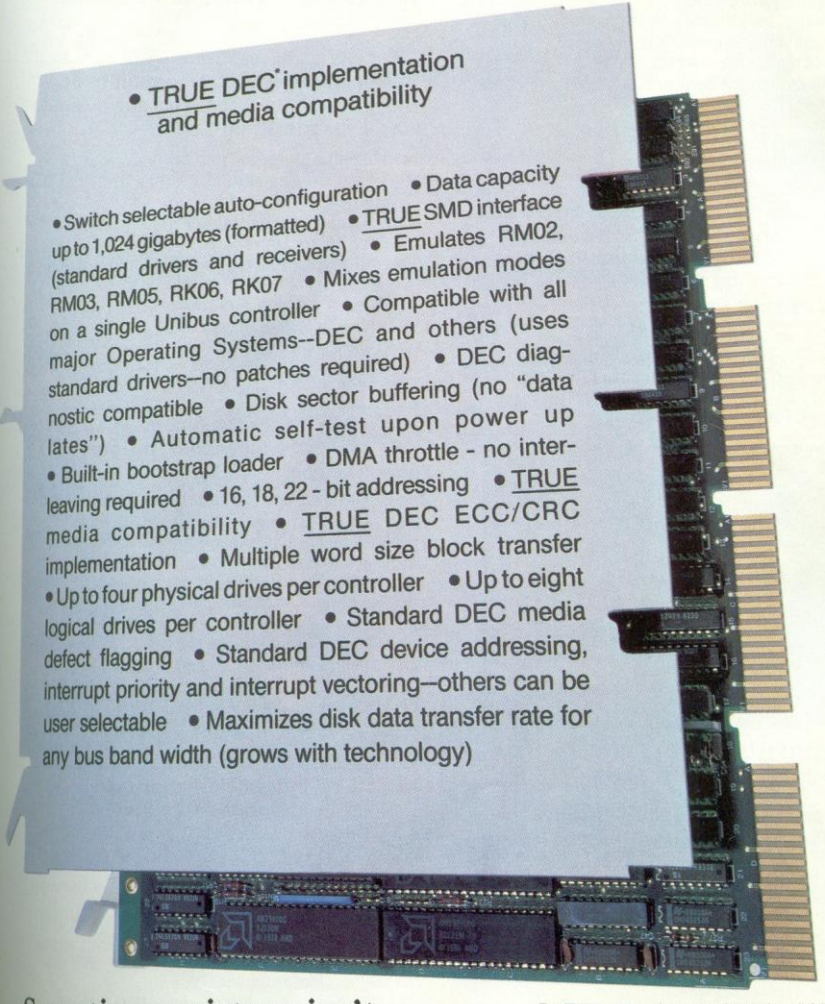
6/2 "Database Machines"
A. Pahwa, Bell Labs

6/3 "Trends in Database Management Systems"
M. M. Carlson, North Eastern Illinois Univ

6/4 "Comparison of Commercial Relational Data Bases"
A. Pahwa, Bell Labs and A. K. Arora, Illinois Institute of Technology

(continued on page 70)

20 major capabilities together for the first time on a single SMD controller!



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(continued from page 68)

Session 10: System Development Methodology and Environment

Wed 4 to 6 pm

Chair: R. B. Silverman, SEI Information Technology

10/1 "Establishing and Measuring a System Development Environment"
R. J. Weiland, SEI Information Technology

10/2 "Establishing System Functionality"
J. J. Rosecrans, Valtec Assocs, Inc

10/3 "Role of Management in a System Development Environment"
M. Kaplan, Western Electric

10/4 "A Project Case Study"
D. Pratt, Motorola, Inc

Session 11: Innovations in Software and Data Security—the Problems and the Solutions

Thurs 9:30 to 11:30 am

Chair: B. Huston, Motorola, Inc

11/1 "The Importance of Software Security in Entertainment Electronics (Electronic Arcade Games)"
D. L. Poole, Taito America Corp

11/2 Title to be announced
F. Thompson, Bell Labs

11/3 "Using Silicon to Prevent Software Theft"
W. W. Wyatt, Motorola, Inc

11/4 "Protection of Software and Firmware: Dispelling the Myths"
M. A. Lechter, Cushman, Darby & Cushman

Session 12: Upward Compatibility of Microprocessors is a Must

Thurs 9:30 to 11:30 am

Chair: J. Nutt, Motorola, Inc

12/1 "Upward Compatible MPU Family"
T. Starnes, Motorola, Inc

12/2 "Hardware Planning for the Future"
R. Bell, Sperry Univac

12/3 "8-, 16-, 32-Bit Requirements in Industrial Control"
B. Papp, Advanced Automation

12/4 "The Software Investment"
D. O'Dowd, Green Hills Software

Session 13: 16-Bit Development Tools for the Individual Designer

Thurs 1 to 3 pm

Chair: R. Mateosian, National Semiconductor Corp

13/1 "Low Cost NS16000 Development Tools"
R. Mateosian, National Semiconductor Corp

13/2 "168000 Educational Board Offers Low Cost Evaluation at Your Fingertips"
K. Roehrman, Motorola, Inc

13/3 "Low-End Development Tools for the Z8000"
S. Walters, Zilog, Inc

13/4 "Evaluation Tools vs Development Tools—Bridging the Gap"
D. Hopkins, Texas Instruments Inc

Session 14: Innovative Peripheral Integrated Circuits

Thurs 1 to 3 pm

Chair: W. W. Wyatt, Motorola, Inc

14/1 "Applying VLSI to CRT Controllers—a Complete Family of CRT Controllers"
J. Goodhart, Signetics Corp

14/2 "A Fusion of Different Memory Technologies Now Allows Flexible System Design"
C. Melear, Motorola, Inc

14/3 "An Innovative Approach for Data Integrity without Sacrificing Throughput"
M. Shapiro, Texas Instruments Inc

14/4 "CRT Controllers, Disk Controllers, New Cost-Effective Solutions"
J. Tweedy, Standard MicroSystems Corp

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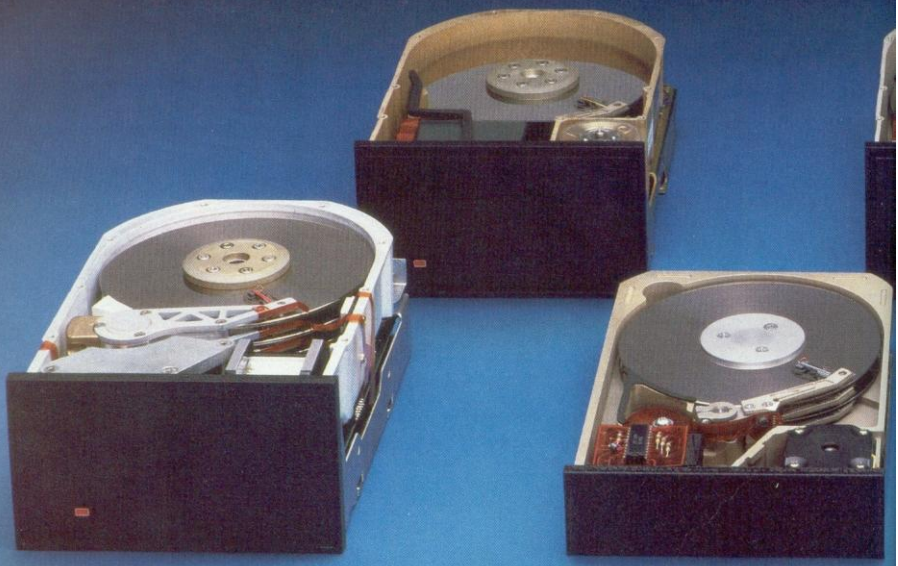

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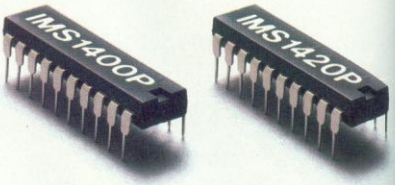

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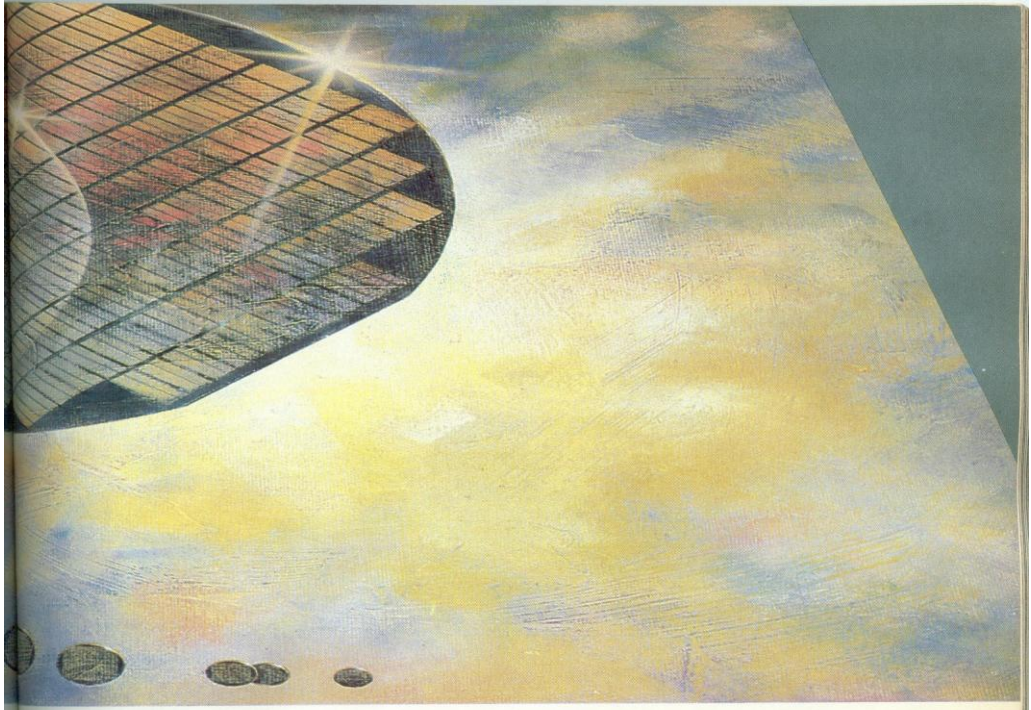
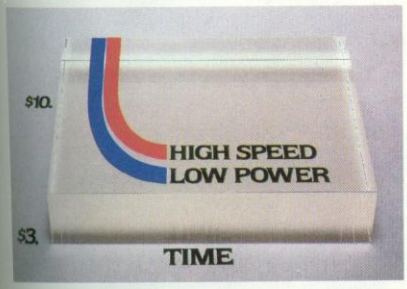
IMS1400P-55	16Kx1	55	660	110
IMS1420P-45	4Kx4	45	605	165
IMS1420P-55	4Kx4	55	605	165



New Low Power



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IMS1420P-70L	4Kx4	70	495	83
IMS1420P-10L	4Kx4	100	495	83

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CIRCLE 40

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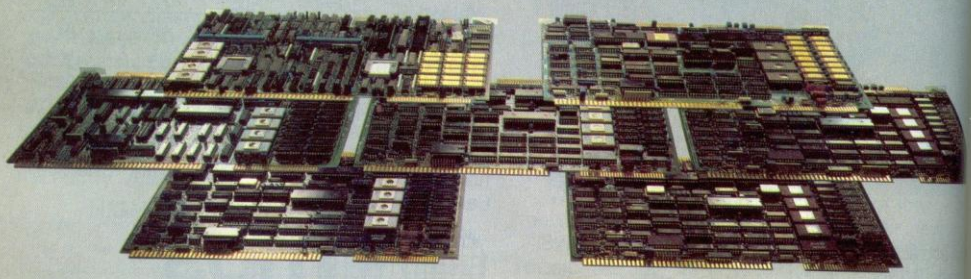

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Circle #41 for Multibus Products Plus Brochure

UNIQUE LAN INTERCONNECTS DIVERSE COMPUTERS

Mesh architecture proves ideal for a local area network linking many types of computers and peripherals.

by Richard Barnett and Richard C. Beckwith

How can 500 dumb terminals, 40 graphics terminals, and a number of small computers be connected with their workstations to a large mainframe and still provide adequate data rates at a reasonable price? As no commercial system satisfies all these requirements, customization is the only alternative.

To meet these needs, a local area network (LAN) was developed at Imperial College, London, to integrate an assortment of peripheral systems with a twin Control Data Corp (CDC) Cyber mainframe. A distributed, local area packet-switching network, CN-III offers a unique solution to the general system communications dilemma facing designers. In this design, diverse computer systems from many manufacturers are integrated into a single, common network. This is accomplished with an architecture considered rare for LANs—the versatile mesh configuration (Fig 1). Conventional LANs use either the broadcast—exemplified by Ethernet—or ring configuration. The mesh architecture of CN-III is a take-off on the well-known resource sharing network ARPANET (see Panel), with modifications adapted for microprocessor implementation.

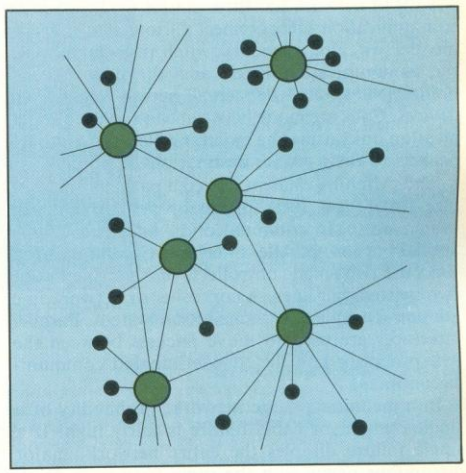

Fig 1 Switching and end-point nodes connected in an arbitrary arrangement of network links characterize a generalized mesh architecture. This is the foundation of ARPANET inspired CN-III.

The CN-III network has several major features: first, high performance results from up to 500k-bps link rates at distances to 1 km. Parallel or fiber optic links can be used for higher data rates. Second, mesh architecture permits distributed switching, similar to the Advanced Research Projects Agency

Richard Barnett is leader of the Microprocessor Group (communications, microprocessors, and graphics) at the Imperial College Computer Centre, Royal School of Mines, Prince Consort Rd, London, SW7 2BP. He is responsible for microprocessor system design and development.

Richard C. Beckwith is section chief of the Microprocessor Group at the Imperial College Computer Centre, where he is responsible for system planning and development in communications, microprocessors, and graphics. Mr Beckwith has a BS in electronic engineering from the University of Wales.

network (ARPANET), with a dynamic routing algorithm.[1] This mesh architecture keeps system faults isolated; maintenance stations permit easy fault location.

Also, simple incremental expansion is provided (new lines and switches can be added during normal network operations) and routing tables are automatically updated. Entry cost is low because each CN-III device is made up of a small set of Zilog Z80A based hardware elements. Finally, installation cost is low because links require just two twisted-pair lines.

Through a variety of network devices and basic communication link technology, CN-III provides a connection method that matches the computer system's capabilities. Where possible, CN-III network device software can be written as a set of general purpose modules. Thus, the modules can serve in many applications. This considerably reduces new network device-development time.

A 3-element architecture

A CN-III network has three classes of devices: the communication links connect various network elements; switching elements switch packets between the communication links; and the network end points (NEPs) are the actual network-connected devices. Calls are made between NEPs over communication links using the switching elements to route packets to their proper destinations.

The switching element, called a packet switch device (PSD), is a Z80A processor system that can switch up to 16 communication interfaces and 1 special-purpose parallel interface. Communication links use two small controllers, one at each end of two twisted-pair lines. A controller or network line adapter (NLA) is also a small Z80A system. Parallel interfaces are used to move packets between the PSD processor and the NLA-terminated communication links.

In a medium to large network, probability of a single-element or cable failure is fairly high. If a single failure disables the entire network, major disruptions occur with the same frequency. With mesh architecture, however, single-element failures are less severe. In the best case, a single NEP becomes unavailable. At worst, when a PSD or important link fails, the network can be split into disjointed subnetworks. In this case, a set of NEPs may not be able to use the network.

CN-III permits the use of redundant links. These links automatically become available when either the normal link fails or an element on the normal route fails, making the route unavailable. Judicious placement of redundant links can provide a highly fail-safe network configuration.

To improve communication among a group of computer systems and terminals located close to each other, a PSD should be placed near to the group. This allows the use of short, high speed links, with packet traffic localized outside the main network. In effect, this configuration becomes a private network. Traffic levels on the rest of the network have little effect on the localized PSD, but the grouped computer systems retain full access to the main network. This is accomplished via a link from the group's PSD to a PSD in another part of the network. In general, network performance can be optimized by locating PSDs wherever localized data transfers occur.

Using a parallel interface to communicate with a PSD or the device in which the PSD is installed, an NLA hides the actual type of link technology. That is, different links can use completely dissimilar technologies yet still be connected into a single CN-III network. Technologies include fiber optics and parallel data links. As long as the controller presents the

ARPANET—coast to coast communication

Created by the Advanced Research Projects Agency (ARPA) of the U.S. Department of Defense, the ARPA network (ARPANET) was designed in 1968 to permit large numbers of dissimilar computers—called hosts—to communicate with each other over a nationwide network. ARPANET is intended to achieve three goals: to allow computer resources (programs, data, special purpose hardware, etc) to be shared among a wide number of computers and users; to develop reliable and inexpensive digital communications; and, finally, to permit access to unique and powerful computer facilities that are economically feasible only when shared by many users.

Architecturally, each ARPANET host connects to the network through a small local computer, named an Interface Message Processor (IMP). Each IMP in the network connects to other IMPs over high speed communication lines. Terminal IMPs (TIPs) provide access for assorted terminals to enter the network.

Moreover, ARPANET's topology is multiconnected. This means that more than one path exists between any pair of nodes. High reliability and network growth at minimal cost are benefits of this multipath approach.

Message switching between nodes, rather than circuit switching, characterizes ARPANET. This is significant because, in a circuit-switched network, the source and destination are connected by a dedicated communications path. Message-switched systems, on the other hand, have no dedicated path. Instead, a source host or terminal passes its message, including a destination address, to a local IMP or TIP. The message travels from IMP to IMP until it arrives at its destination. Also, the path from source to destination is determined dynamically. That is, each IMP forwards the message on the path it deems best to ensure prompt delivery, taking into account network loading and failed paths.

Without a doubt, message-switched networks, based on ARPANET's operation, are well adapted to the interconnection of diverse computers and terminals. The network is not only operational, but growing. In time, it may shift from its defense-related role into more commercial areas.

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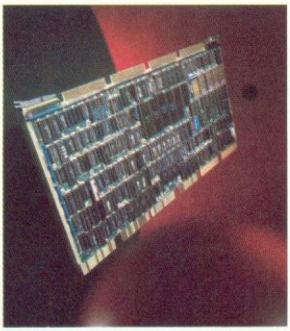

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same parallel interface as the NLA, any technology can be used. In fact, this entire network concept is in no way tied to the specific implementation currently in use.

For example, two MODCOMP II minicomputers at the Imperial College installation act as switching elements while providing a very high bandwidth link into the CDC mainframes. Switching elements and links need only provide performance sufficient to operate within the NEP's requirements. This concept not only considerably extends the network's lifetime, but since the network is not wedded to a specific hardware system, higher performance can be provided as required. Links and switches can be added or upgraded on a running network, with little or no disruption to the rest of the network. At worst, some packets may be lost as changes are made, but these are identified and corrected by higher level protocols.

Updating by dynamic routing

To fully utilize mesh architecture, it is important to use a dynamic routing system. If a conventional network uses hard-coded switching elements, these switching elements must be updated with any new connection. However, this means the elements are unavailable during the updating process. CN-III, on the other hand, updates automatically and has no hard-coded information regarding the network's configuration. Therefore, PSDs need not be customized for a particular network location.

This updating method is based on the ARPANET technique. As such, it requires that all network elements, including PSDs and NEPs, maintain a so-called configuration table. The table has an entry for each NEP on the network.

Among other data, the entry contains the NEP address and a "cost factor." Cost indicates the type of performance expected of a particular route to a specified NEP. The cost factor is weighted by the number of links involved in the route and their quality.

Network rules require that network elements broadcast their configuration tables—under certain conditions—to all elements to which they are directly connected (but not via a PSD). When a network element receives a configuration table in this way, it uses the table to construct a new one for itself. Each NEP entry is checked in turn, and three possible actions can be taken for each entry.

First, if the NEP specified is not in the element's table, a new entry is added. This records the fact that the new NEP is available via the link on which the configuration table was received. It also records the specified cost factor. Second, a NEP can already be specified in the element's table, but the new entry's cost factor may be greater than that currently in the table. In this case, the new entry is ignored and the old route retained.

And, finally, if the NEP is in the table and the newly received entry's cost factor is lower than the original's, the original is discarded. Only the lower cost route is used for future traffic. If a NEP was previously available via the link used to receive the configuration table, and now there is no entry for this NEP on the new table, that NEP is no longer available on the route and its entry must be deleted from the element's table.

Configuration-table broadcasts are event triggered (ie, they do not normally occur). A broadcast occurs if a new NEP becomes available, a new route is established for an existing NEP, a NEP becomes unavailable, or a PSD restart occurs. Usually, the rules governing configuration-table broadcasts make oscillations impossible while spreading news of the change as fast as possible. Updating occurs concurrently with normal packet routing and does not disrupt normal network operation.

In effect, CN-III has two protocol levels. The basic packet-delivery protocol is the Intra Network Protocol (INP). Above INP is the Trans-Network Communications Protocol (TNCP). TNCP corresponds to level 3 in the 7-layer International Standards Organization (ISO) model. Together with the American National Standards Institute, ISO has developed an Open Systems Interconnection model that serves as a reference for protocols within a network.

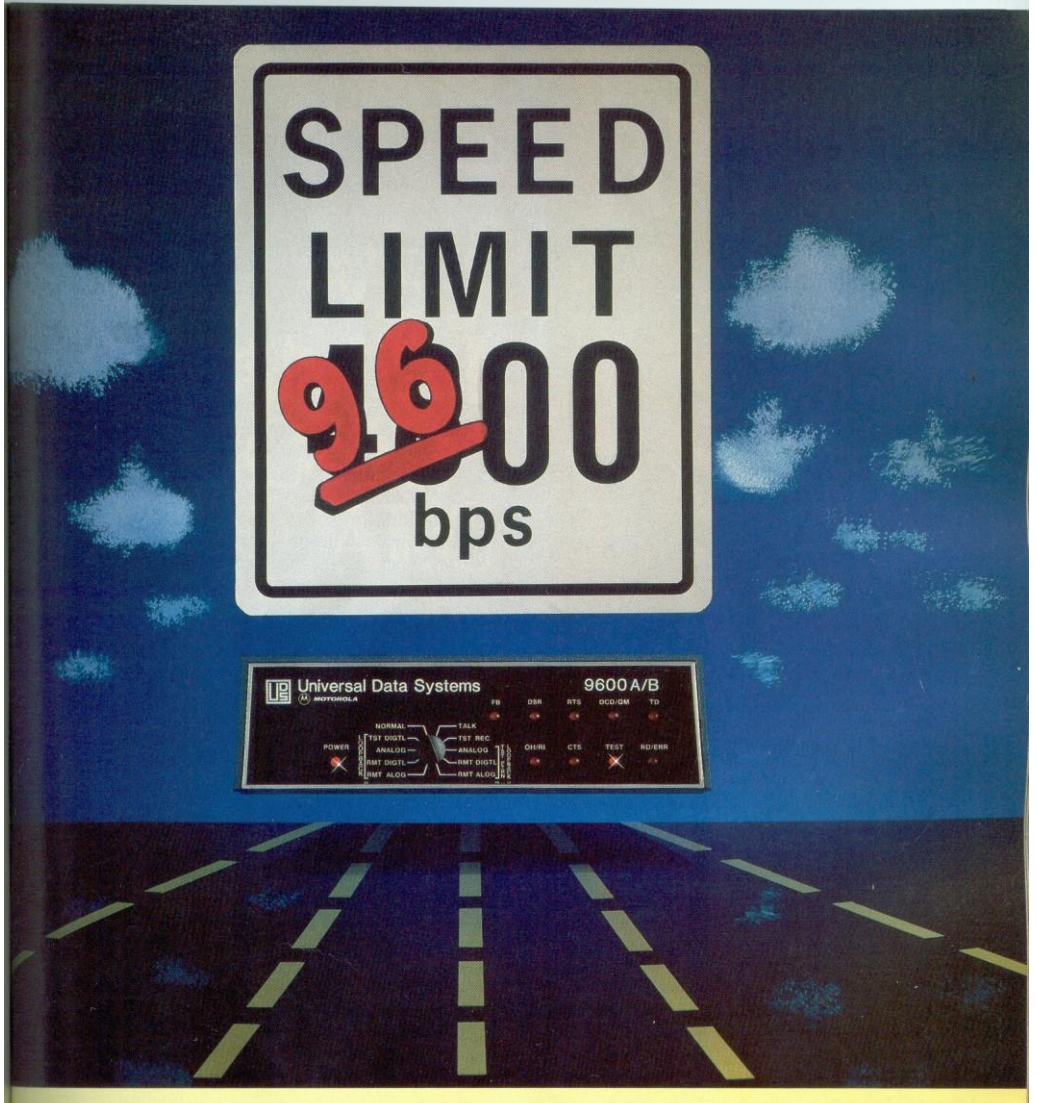
INP provides three functions. First, it links failure detection and recovery. Network elements at each end of a link use 2-byte link control packets to maintain the link state. The three possible states—and packet types—are down, resync, and up. Second, it permits two packet types for configuration-table broadcasts. Configuration-table broadcast rules dictate the specific type.

Third, INP defines trans-network data packets, which are used to transfer NEP-to-NEP packets and maintenance packets. In addition to INP-type code, such packets have two 16-bit fields. Each NEP on the network receives a unique 16-bit identifying code—its network name (usually restricted to binary coded decimal digits). The first field contains the name of the NEP that generated a packet, while the second contains the packet destination name. PSDs also use this second field for packet routing.

TNCP, the other protocol level, provides a virtual-call facility and implements flow-control strategy. It is a positive acknowledge protocol with a 1-packet acknowledge window. This technique helps keep TNCP software to a minimum. TNCP's structure (Fig 2) provides support for a so-called standard Transport Service (TS).

Collecting maintenance data

CN-III incorporates a maintenance facility through the INP protocol, which includes a special packet for this purpose. The packet permits information to be collected from any element in the network.



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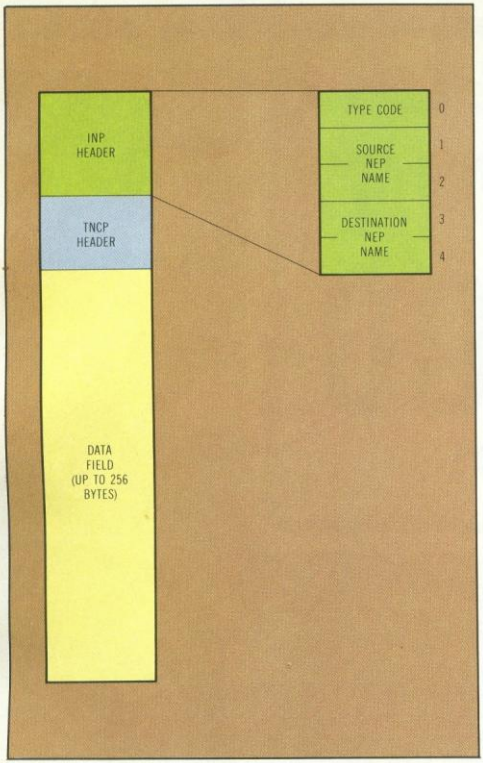

Fig 2 The TNCP consists of a 5-byte header containing source and destination NEP names, followed by a 4-byte TNCP header field with call and flow-control information. The data field following the header can be up to 256 bytes in length.

A special monitor station allows the use of this maintenance facility. The CN-III Maintenance Station (CMS) uses a high density text display of 52 lines of 136 characters each to display realtime network information. The screen is split into several areas, each dedicated to a particular display function. For instance, one area acts as a video display unit (VDU) emulator, which allows CMS to interact with remote systems.

A set of maintenance-collection functions can be selected by pressing the proper function key on the CMS keyboard. The four functions are general link status, standard mode status, configuration table, and link condition.

The general link status function requests device-dependent information about a link to a NEP or PSD. Device dependent means that the response format varies according to the type of device. CMS selects the appropriate display driver or the device type to process the contents for display. Target device requests are made about once per second. Thus, information displayed by the CMS is, a most, 1 s old. All maintenance functions are simi larly updated until an operator cancels the functio from the keyboard.

In addition, the standard node status functio requests device-independent information about network element, including the state of the links t which it is connected. And the function reques the configuration table from a target device, whic is useful for tracing routes between two NEPs.

Finally, in the link condition, NLAs maintai detailed data about the state of the link that the drive (number of cyclic redundancy check errors timeouts, etc). To access this information, the CM sends a request to the device in which the NL resides. Sending a command results in the devic receiving the special packet from the NLA. Th device then returns the packet to the CMS that mad the request.

In addition to these functions, any device tha maintains a realtime clock can synchronize with th CMS clock by using a maintenance function. Th CMS maintains a network-event log in the scrollin area of the cathode ray tube screen. Any device ca send a message to the log with the proper mainte nance function. The message is displayed alon with the sending NEP's address and the time it wa received. A hardcopy terminal can be connected i a permanent log is required. For example, most de vices send a message to the log on startup. PSD send a message every time a link failure is detected This allows network supervisors to be immediatel aware of a problem.

Several network utility services—sink, echo source, and call—are available to other networ devices. A network can have more than one CM and other devices can request maintenance infor mation. But a CMS is not a necessity for networ operation; any size network can operate without a CMS, but at the expense of increased time for faul location.

The Z80A hardware base

All the network elements are designed around th ubiquitous Z80A microprocessor and its associate system components. Other than application-depen dent peripheral interface boards, just four differ ent boards are used in various combinations.

One board contains the Z80A, direct memor access devices, and other support chips. The sec ond board is system memory and contains a mix o electrically programmable read only memory and complementary metal oxide semiconductor static random access memories. Sixteen RS-232 interface and their associated circuitry reside on the third board. The fourth board is an NLA with a self-con tained Z80A processor system for running the com munication link-level protocol. RS-422 drivers and receivers operate with twisted pairs to run at a data

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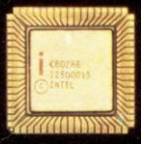

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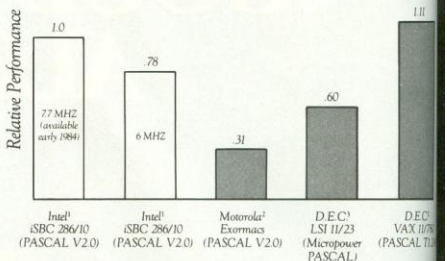

[1]*Based on Eratosthenes Sieve Benchmark in PASCAL. Details available from Intel's "Eratosthenes Sieve Prime Number Benchmark on the ISBC 286/10 Board," literature order number 210984.* [2]*"Eratosthenes Revisited," BYTE. Jan., 1983.*
[3]*"A System/Architecture Approach to Microcomputer Benchmarking." Digital Equipment Corporation. Sept., 1982.*

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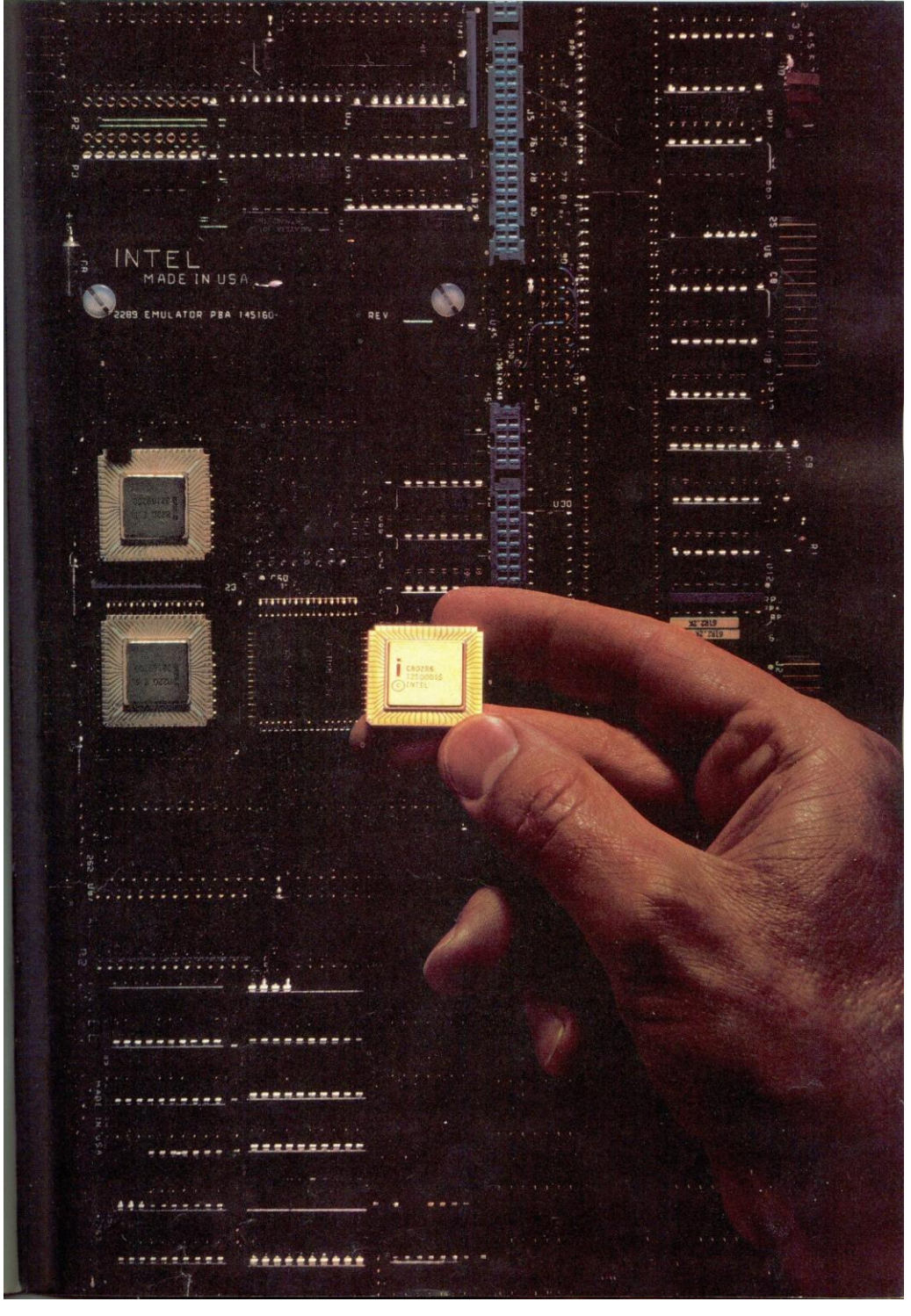
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rate of either 250k bps or 500k bps. A new version of the NLA, called the fast link adapter, is under development. This device will be able to run a fiber optic link at a 20M-bps data rate.

Hardware is constructed using double-sided boards in a double-Eurocard pattern. Boards are packaged within a standard slim-line "blue box." Some devices have a liquid crystal display on the front panel to continuously display important parameters.

Current CN-III network devices permit connection to a variety of computer systems and some application-oriented systems that can exploit LAN facilities. For example, the CN-III Packet Assembler/Disassembler (CNPAD) provides a connection for dumb terminals, personal computers, and other small computer systems (Fig 3). CNPAD has 17 RS-232 serial ports, each of which runs at various speeds. X-ON/X-OFF flow control is available in both directions, permitting high speed data transfers in and out of the CNPAD port.

A number of parameters define a port's specific operating mode (eg, flow control enable, echo mode, and data forward on timeout). To guide a user through the selection process, a comprehensive menu system eliminates referring to a manual for the correct command. Calls to other network devices, or another port on the same CNPAD, also use the menu system. Thus, a user need not remember long, complex address strings. Rather, CNPAD offers a choice of devices on the network (obtained from the configuration table). Thus, the user only has to type a single character into the keyboard to select a device or type of service.

One CNPAD can serve as a simple LAN since calls can be set up between any two of its ports without any form of network connection. An optional expansion increases the number of ports from 17 to 31. A variation of CNPAD is called Anti Pad (APD). This device connects up to 16 RS-232 ports from a service-providing host onto the CN-III system.

The Transport Service Adapter (TSA) provides a high performance, high level CN-III connection method.[2] An 8-bit bidirectional data port, together with 10 control lines that handle the data flow across the interface, is the interface between a TSA and its host. The interface from the TSA uses a 40-ribbon cable—20 signal lines and 20 ground lines—and can run at up to 250k bytes/s. It is designed to permit the host to use just a Z80-type programmable input/output chip, plus buffering, for connection to the TSA.

Communication between TSA and host is via messages passed across the parallel interface. The message-passing protocol is a master-slave relationship; the host is the master, TSA is the slave. At the logical level, the interface takes the form of a TS-level interface. This TSA TS supports the primitives specified in the "yellow book" recommendations.[3]

One benefit of a standard TS-level interface is that nonstandard aspects of the underlying LAN architecture have little effect on the network that the host device sees.

In addition, this interface can support multiple streams (ie, the TSA can support several simultaneous active calls up to a configured limit). Service providers—file servers, for example—can be TSA connected. A service makes itself known by sending its service name to the TSA. Any connect that the TSA receives, specifying the service name in the TS address string, will be passed through to the service provider.

Additional network elements

An X25 Inter-Network Adapter (INA) serves two very important purposes. First, it connects X25 speaking host devices into the CN-III network. Second, it can be used as a gateway into external X25 wide-area networks.[4]

X25-INA supports multiple, simultaneous calls across itself; each call has an X25 call and an associated TNCP call. Packets on the X25 side of the X25-INA are mapped into their equivalent packets on the TNCP side, and vice versa. In fact, the TNCP design simplifies this process.

The X25-INA is somewhat of a misnomer—it not only supports X25 but also X29 and TS29. This permits CNPAD-connected devices to run interactive sessions with hosts available on the wide-area network through the X25-INA. All addressing, aside from the NEP name of the X25 used, is carried in the connect's TS parameters. This allows uniform addressing of both devices on the local CN-III network and devices connected to other, external networks.

A local intelligent terminal system called Advanced Campus Terminal (ACT) offloads highly interactive operations from remote computer systems. ACT, developed from the Community File Station, connects directly to the network via its own NLA. Thus, it has access to full network facilities and NLA link bandwidth.

ACT supports two types of network calls. An interactive call allows a user to connect to an interactive computing service in the network. A file transfer call is used to transfer files to and from the filing system, or color graphics display, across the network. Calls can be initiated either by the ACT user or by another device on the network (eg, another ACT).

An example of this operating mode is the use of the ACT as the file server. Files on the ACT's disk can be created and accessed by other network-connected devices. A set of parameters controls the ACT's operating mode, and a setup function allows a user to alter the operating mode with a question and answer system.

Another useful network device is the Line Printer Station (LPS), designed to interface a

Centronics-compatible printer to the CN-III network. This device can operate without supervision in an end-user environment. Files are sent to the LPS for printing under one of two file-transfer protocols (FTPs): the Network Independent File Transfer Protocol, which is becoming standard in the United Kingdom;[6] and the Mini File Transfer Protocol (MFTP), used in the ACT and other CN-III devices.[7] MFTP is a much simpler protocol and is easy to implement on small computers. The actual protocol used is selected by specifying either FTP or MFTP on the connect TS parameters.

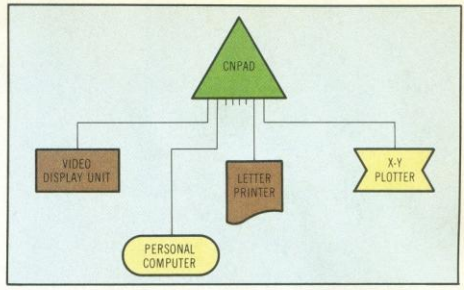

Fig 3 Just a single CN-III Packet Assembler/Disassembler (CNPAD) can connect up to 17 dumb terminals, personal computers, and other small computer systems through RS-232 serial ports. Each port can run at baud rates from 300 to 19.2k.

A CN-III hierarchy

The single CNPAD of Fig 3 is the smallest useful CN-III network. Without its NLA communication link, it can serve as a LAN for up to 17 terminals or computer systems through its RS-232 ports. Calls can be set up between any pair of ports, and flow-controlled data can be transferred at rates up to 19.2k baud. This type of system is useful for a very isolated group of terminals that need not access the network on an extended basis.

By adding a single PSD, as shown in Fig 4(a), the range of systems that can be connected to the network is expanded considerably. NLA pairs can operate at distances up to 1 km. Therefore, a single-switch CN-III configuration can cover a considerable geographical area. Several CNPADs can operate in such a configuration. Also, since any CNPAD port can call another as long as the called port accepts the call, CNPAD-connected devices can communicate with any others on the network.

A higher step is the dual PSD configuration in Fig 4(b). The PSDs are connected by two links. Thus, if one fails, the other can provide an interswitch link, preventing network disruption. An APD is shown in its role as a front end to an interactive host. This network permits a wider range of connected devices, including some TSA-connected types.

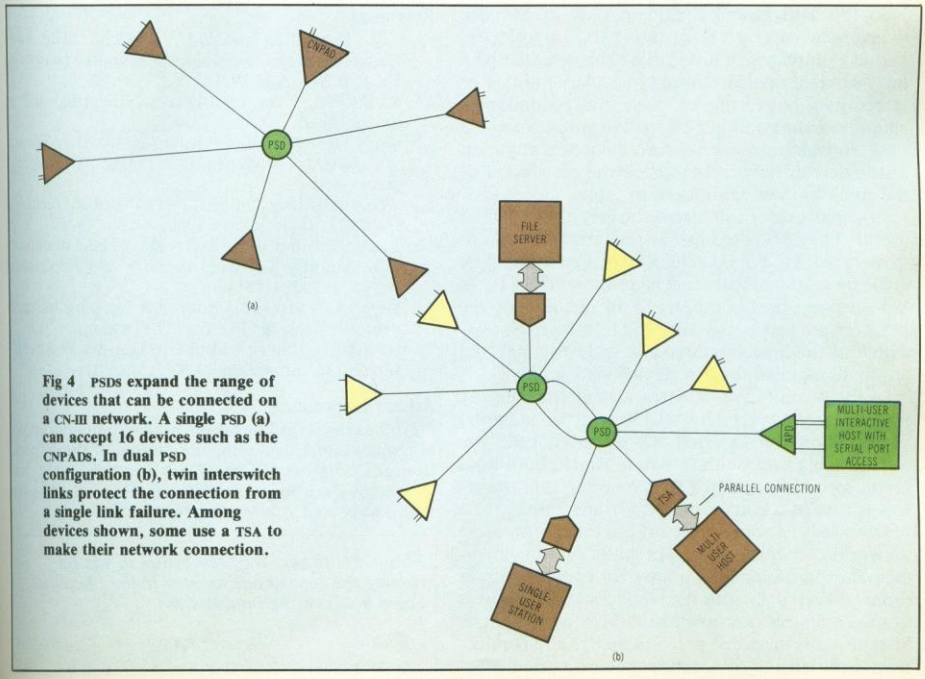

Fig 4 PSDs expand the range of devices that can be connected on a CN-III network. A single PSD (a) can accept 16 devices such as the CNPADs. In dual PSD configuration (b), twin interswitch links protect the connection from a single link failure. Among devices shown, some use a TSA to make their network connection.

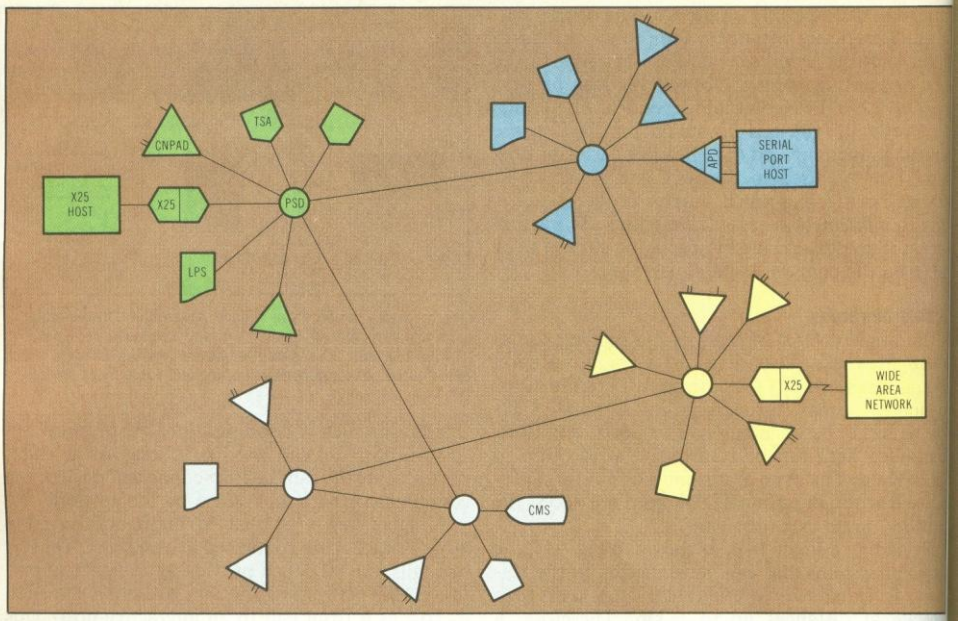

Fig 5 The multiswitch network demonstrates the highest form of CN-III architecture. An external network connects to CN-III via an X25-INA. Another X25-INA acts as the host interface while a CMS provides the maintenance capability.

CN-III's real power is evident only in a multiswitch network (Fig 5). Various PSDs are interconnected by interswitch links; these can be either NLA links or higher performance types. Any number of interswitch links can be used for redundancy, should one link fail. The fact that more than one PSD can be on a route between devices is apparent to the devices only if they check the cost factor of the route in their configuration tables.

In a network of this size or larger, a CMS can be useful. The CMS needs just a standard NLA link into any PSD. Fig 5 shows the X25-INA performing its dual roles. In one case, it acts as an interface to an X25-speaking host computer. Full facilities of the X25 host are retained across the interface. For example, if the host supports X29, CNPAD-connected terminals can call the X29 service via the INA.

In the second case, X25-INA acts as the gateway into an external X25 network. When, for example, a device on the external X25 network calls the X25-speaking host on the CN-III network, both INAs are in use. Although two INAs map the call, the effect is that of a continuous X25 connection.

Obviously, CN-III is versatile enough for most networking requirements. In addition, its incremental expansion ability allows for easy buildup in order to keep pace with demands for more connections. Designers can now install high performance links to tailor network performance to the connection requirements of a wide range of equipment.

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The World's Most Elegant Microprocessor Family

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Be advised: the NS16000 family is establishing all new benchmarks for 8-, 16-, and 32-bit microprocessors.

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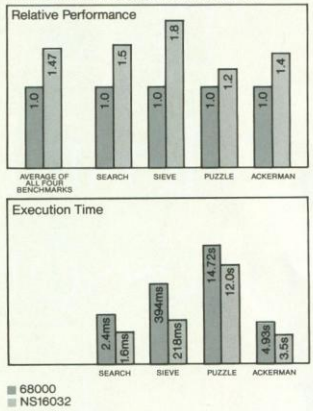
Of course, comparing the NS16000 family and the microprocessors your competition is banking on is difficult—perhaps even irrelevant—because the NS16000 family is, fundamentally, much more advanced.

No other commercial processor (micro, mini *or* mainframe) is designed to fully support the use of high-level languages. All members of the NS16000 family of CPUs;[1] however, feature not only 32-bit internal architecture, but also a high degree of regularity in the arrangement and use of their 32-bit registers. Data can be read or written 1, 8, 16, or 32 bits at a time, as sophisticated programs require, and transfers from one register to another are not restricted.

Moreover, the symmetrical instruction set of the NS16000 CPUs includes over 100 genuine two-operand instruction types, but avoids special-case instructions that compilers cannot use. All instructions can be used with the addressing modes common to most microprocessors (register, immediate, absolute, and register relative), as well as with powerful HLL-oriented modes that only the NS16000 offers: top-of-stack, scaled indexing, memory relative, and external. And any operand length and any general-purpose register may be used with any mode.

The combination of these virtues makes it possible to write especially lean high-level language programs on NS16000-based systems. The simplicity with which a programmer can implement a compiler, for instance, is matched only by the compiler's increased speed of execution. In effect, the dream of being able to pack the enviable working environment and performance of a large computer into a microprocessor has become reality.

HIGH-LEVEL LANGUAGE COMPARISONS[2]



Putting large-computer performance into a microprocessor is further advanced through the implementation of the NS16000's Demand Paged Virtual Memory—a strategy equivalent to that used in such systems as the VAX-11 series and all present IBM mainframes.

With an architecture that supports uniform addressing, the NS16000 is the first commercial microprocessor able to feature Demand Paged Virtual Memory as a means of solving large-memory-management problems. As a result, an NS16000-based system, blessed with this completely flexible memory configuration, can maximize the use of its physical and virtual memory resources and achieve a level of performance heretofore unrealized.

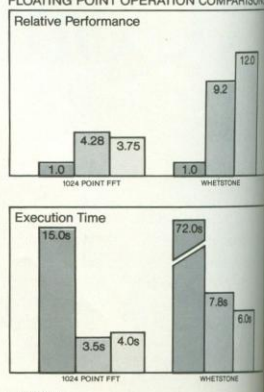
With the NS16082 Memory Management Unit (MMU), only the information most recently used is kept in RAM: other information is swapped in and out from mass storage, as needed. Consequently, each programmer, each program, each task has access to a uniform addressing space of 16 Mbytes simultaneously and independently, without reservation or special exception. (And more efficiently than on any other commercial processor—micro, mini, or mainframe.)

Among the reasons for the MMU's prowess is its support of a *two-level* page table translation, whose process is speeded up by an associative on-chip cache. Utilizing a very fast Least-Recently-Used (LRU) algorithm and a powerful "referenced bit," the NS16082 MMU achieves a translation cache hit rate of over 98 percent.

The NS16081 Floating Point Unit (FPU) extends the NS16000 instruction set with very high-speed floating-point operations for both single- and double-precision IEEE operands.

Designing the FPU into a system allows programmers to treat floating-point numbers as they would any other data types, and to use any of the addressing modes to reference them. For example, the scaled index mode permits an array of floating-point data elements to be addressed by its logical index, rather than its physical address. The power this can add to a system makes it especially applicable for graphics and engineering work-stations.

FLOATING POINT OPERATION COMPARISONS[3]

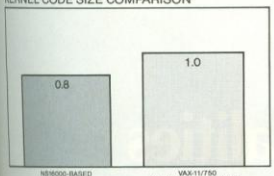


With the introduction of National's proprietary GENIX™ operating system, even the advantages of using UNIX® on a large computer have been ported to the NS16000 microprocessor family.

GENIX is an elegant implementation of the proven Berkeley 4.1 bsd version of UNIX. Created in-house, to facilitate the development of software for NS16000-based applications, it is the first UNIX operating system to support Demand Paged Virtual Memory in a microprocessor.

Here, then, is a demonstration not only of the pure functionality of the NS16000 family architecture, but of the large-computer-like results now possible on a microprocessor-based system using GENIX.

KERNEL CODE SIZE COMPARISON



When you consider applications for the NS16000 microprocessor family—from elegant personal and business computers, to graphics work-stations, to industrial control systems—keep in mind that:

1. The NS16032 CPU and the NS16201 TCU are in production now.
2. The NS16082 MMU, the NS16081 FPU, and the NS16202 ICU are being sampled now.
3. Evaluation tools are available now.
4. Development tools are available now.
5. Training classes are in progress now.
6. Third-party software for the family is available now and increasing daily.
7. The software you write now will work *without modification* if you move your product line from one NS16000 CPU to another in the future.

   Similarly, the optional use of the NS16000's MMU and FPU slave processors—integral parts of the NS16000 architecture—will allow you to determine price/performance trade-offs while preserving your initial software investment.
8. Only the NS16000 family can make it possible for you to put a large-computer-like product on the market today—at microprocessor prices.

Footnotes:

1. The NS16032 CPU, the first of the NS16000 CPUs, has a 16-bit-wide data path to memory and 32-bit internal architecture. Before the end of this year, CPUs implementing the same 32-bit internal architecture, but with 8- and 32-bit-wide data paths to memory will also be available, to allow maximum price/performance flexibility within your product line.

2. Results for the 68000 were taken from *Computer Architecture News*, Vol. 10, No. 4, June 1982, pp. 17-28. The 68000 was run at 10MHz, with no Wait States. Source programs in Pascal.

   Results for the NS16032 were obtained on a DB16000 at 10MHz, with no Wait States. Source programs in Pascal. All variable sizes are 32-bit.

3. Results for the 68000 were obtained on a SUN System at 10MHz, with no Wait States, using Motorola's ROM-based floating point subroutine package.

   Results for the NS16032, utilizing the NS16081 FPU, were obtained on a DB16000 at 10MHz, with no Wait States. IEEE floating point, variable sizes.

   Results for the VAX-11/750 were obtained without using floating point accelerator.

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NS16000: Demand Paged Virtual Memory

NS16000: Benchmarks

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RELIABLE DESIGNS BEGIN WITH THE BASICS

Even veteran engineers, slugging it out in the design trenches, can benefit from review of reliability basics. So, here are some hints and kinks for harried engineers.

by Carl P. Oppenheimer

Although the proliferation of microprocessor based systems has been startling in the last 10 years, there is still no universal way to predict their reliability. Typical reliability prediction methods that are based on the assumed reliability of individual components are not applicable, since subtle design flaws can cause erratic operation. For instance, a solenoid putting spikes on the power supply output, or a memory device with marginal access time, may cause intermittent errors. Software can also cause errors that are nearly impossible to diagnose.

With the potential pitfalls of these flaws, designers often wonder how reliable a system can or should be. A good guideline states that a system's reliability should be directly proportional to the cost, user aggravation, and safety risks of a worst-case failure.

While the cost of failure is initially paid by the user, penalties will ultimately be passed to the system manufacturer through lost sales and/or legal proceedings. For instance, computerized bank tellers that give away money, industrial machines that destroy parts and halt production, as well as machinery that kills or maims are chilling examples of system failures where manufacturers may incur liability. To avoid these problems, systems must be planned with care and attention to detail. And, working engineers, long out of school, would do well to periodically review the basics of reliable system design.

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Back to basics

Power supply problems are a major cause of system failure and transient errors. These become an even greater difficulty when power distribution noise and ground loops are considered.[1] Major power supply problems include long term power supply failure (eg, loss of ac mains), and temporary loss or drops (eg, brownouts) in ac power input.

Power-failure circuitry can signal the system that V_{CC} will only be available for a few more milliseconds. This allows the system to go into a power-down routine that protects vital data in open files and prevents drive heads from crashing into disk surfaces. Power-failure circuitry is available for some power supplies. Where it is not available, it should be added.[2]

Other methods used to protect data and peripherals in case of power failure include the use of battery backup and/or a redundant power supply. Battery backup is useful for temporary system

operation, since a system with battery backup has time for a graceful shutdown. The addition of a redundant power supply to a battery backup unit ensures that the time required to switch in and stabilize a new power supply is available. Note that this will not work in the case of an ac input power failure.

Temporary losses or drops in ac power input account for a great many system failures. Currently, the instability of ac power in many areas is becoming worse. In microprocessor based systems, a momentary drop in ac power is often enough to cause a drop in V_{CC} (supply voltage). A spike in V_{CC} can, and does, affect microprocessors. Unfortunately, such failures do not always result in a reset, and thus often go unnoticed. Using power-failure circuitry that detects a momentary drop in ac power is one way to ensure that a power-on reset occurs. A watchdog reset circuit or timer also guarantees reset when appropriate.

Watchdog timers expect to receive pulses from the microprocessor at a predetermined rate. Pulses are generated from decoding the address of an input/output (I/O) or a memory location that is repeatedly accessed during normal operation. If the pulses are not received at the predetermined rate, the watchdog timer resets the processor or causes a nonmaskable interrupt. This provides alarms and/or system restart. Adding a watchdog timer is an inexpensive way to ensure system performance.

Noise presents the designer with additional problems.[1,3] These problems are often very difficult to detect because they are either intermittent or random. Noise problems can take the form of electrostatic discharge, spikes, or noisy peripherals. To avoid noise problems, normal high speed digital design practices, such as protecting inputs with transient suppressors and proper shielding, should be used. Well-filtered and regulated power supplies, and the shielding of interconnect wiring can also reduce noise.

Other design considerations involve the use of separate power supplies for noisy peripherals. Remember that peripherals, solenoids, and motors all add noise to a power supply distribution network. The high speed sequential waveforms in many systems also make circuit board design critical. Properly positioned bypass capacitors and ground planes help the designer avoid noise problems in the system.

I/O not GIGO

I/O peripherals present the designer with additional challenges. Output peripherals such as digital to analogs (D-As), voice output systems, and display devices convert system data into a different form. This is, of course, their function, but the conversion makes direct testing of peripherals difficult. Short circuit and overload protection alarms, as well as error correction codes (ECCs), help keep the system working.

Analog outputs should include short circuit and overload protection alarms. The microprocessor monitoring these alarms can disconnect the faulty output, signal the operator, or switch in a backup system to prevent system damage when necessary.

ECCs, parity check bits, and elaborate protocols, are ordinarily used for serial I/O data transmission, such as RS-232 and MIL-STD-1553B. Checking output peripherals with an input peripheral has its drawbacks, however. For example, if an analog to digital (A-D) checks a D-A, a lot of overhead is required. Worse still, the test does not show which peripheral is failing.

Unlike output peripherals, input peripherals provide many opportunities for self-testing.

I/O peripheral tests as well as system tests can be performed in a closed loop control system. An automotive engine controller that monitors the revolutions per minute and controls the carburetor, for example, can be self-testing. Redundant I/O peripherals and a transfer function of the system can localize the error. Other output peripherals, such as cathode ray tubes and printers, are almost impossible to test directly. Operator verification is possible with test patterns, however.

Unlike output peripherals, input peripherals provide many opportunities for self-testing. Many inputs can be connected to known signal sources, such as voltage or frequency, and then tested. Although this assumes a reliable signal source, faults can be localized if more than one source or input is available. This type of test requires little overhead since there is usually an extra channel available on a multiplexed input system. Tests can be done quickly and performed whenever the input is used. This method allows easy checking of important parameters, such as power supplies and clocks. In addition to the already mentioned tests, designers should debounce switch inputs with hardware and/or software. To avoid system damage from overvoltage inputs, it is good practice to isolate inputs with optocouplers.

System software should be able to handle any combination of inputs or range levels without problems. Many A-D converters, for example, require a START CONVERT command and will respond after a nominal time with an END OF CONVERSION message. This is often done via a software polling routine. Note that all polling routines must have a software fallout so the system does not wait forever

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for a response if the END OF CONVERSION message fails to occur. An example of a polling routine with software fallout follows:

```
T=0 (Initialize timer)

Output=Start Convert Command

Do While (No End of Conversion)
   and T<100

T=T+1

END

If T=>100 A-D is not responding
```

Software techniques can improve reliability

Software can also be used in data smoothing to debounce switches and remove noise from analog inputs. An average of two samples of the same quantity is the simplest method of data smoothing. A complex digital filter algorithm can also be used.

A still more complex system of sampling for noisy signals assumes that two consecutive samples are similar. The samples must be taken one after another with negligible time delay. For instance,

```
Start:  Input 2 Samples S0,S1

        X=Preset Value (maximum allowable
          difference between samples)

If [S0-S1] <=X then finish.
```

If not, try again. After a set number of tries, an error condition can be assumed.

Another way to smooth data assumes that two consecutive samples are similar. This method can be used if data are input at regular intervals, or if time information is available to correlate samples. Data from sample to sample should not change more than a set maximum amount to preserve low overhead.

Averaging data from multiple or redundant sensors presents two potential problems. Multiple sensors can be used to measure a parameter that is consistent from sensor to sensor. Although the data can be averaged, and the sensor with the largest mean deviation ignored, the sensor with the largest mean deviation may be the only correct one. Another difficulty with this kind of measurement can result if the system has only two transducers. If one fails, averaging the two yields bad data.

If synchro inputs or outputs are used, checking for reference power is easy. The synchro will not operate if all reference power is unavailable. Synchro to digital converter input data should be ignored in the case of digital to synchro converter outputs, and an alarm condition should be set.

Microprocessor design books, manufacturers' data books, and design handbooks from some of the major semiconductor companies provide useful information on the multitude of available memory devices.[4,5] Static random access memory (SRAM) is one such device.

The increasing popularity and lowered cost of complementary metal oxide semiconductor (CMOS) SRAM has allowed many manufacturers to make CMOS SRAM memory boards with battery backup for various bus structures. Since the RAM maintains the data in case of a power loss, this permits more reliable system operation.

To increase the reliability of some larger systems, error correction and detection is employed.[5,6,7] Single error correction (SEC) and double error detection (DED) are now used extensively. This system corrects 1-bit errors, but only detects 2-bit errors.

SEC and DED use several parity bits stored within each data word. A common configuration for 16-bit words is 5 parity bits.[5] The 5 parity bits associated with a data word read from memory are compared with 5 parity bits generated using the data word. The difference between the two, called a syndrome word, contains the error information that allows the SEC, DED functions to operate.

Any actual gain in reliability from using SEC DED depends on the memory's reliability and configuration, as well as the circuitry's reliability.[5,8,9] If the RAMs used are 1-bit wide, as in the Harris 2164 or 2147 chips, the memory can be configured with one chip per bit of the parallel data word. In this configuration, one chip can fail, and the system still operates error free.

RAMs can also be checked by the microprocessor during normal operation. Writing known data to a memory location, then reading it back and checking for equality is a straightforward operation. However, a wide range of interactions and combinations must be considered for thorough testing.[10,11]

One thorough test, GALPLAT 1, takes about 12 h for a 64K-byte memory. If a medium-performance microprocessor drives the memory, each read, write, and verify takes approximately 10 μs. Simpler tests performed by reading and writing a few words to each chip can be done in under 1 ms, however. Obviously, compromises between thorough testing and available time must be made. Checking every possible combination in a large RAM is time consuming and often impossible.

Since magnetic media include a wide range of products from a small cassette recorder to large hard disk systems, choosing the right system for intended use is important. A cyclic redundancy check (CRC) is often used for testing tape drives. A CRC character is appended to each data block as it is written. If an error exists between the appended

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character and another one that is generated when the data block is read, the read/write operation is repeated. CRC code is particularly useful in correcting burst errors (several closely spaced errors) that result from common mechanical problems in tape drives, as well as tape imperfections.

Tracking down soft errors

Software, like hardware, does not offer the designer a way to ensure a reliable system. Instead, a number of interdependent checks and tests help the designer find and remove bugs. Unique to software problems is the fact that they are almost always due to design flaws.

Reliable software begins with an error-free program. This kind of programming has been discussed in a number of books.[12, 13, 14] The first step to a reliable system is obtaining a correct definition of system requirements. This can often be difficult in the early stages of a project.

To avoid inappropriate designs, a written description and/or flowchart of the solution that everyone agrees on is critical. The project suffers when there is a lack of communication.

After a program's flow and functionality are documented, design tasks should be broken into functional modules. A good way to accomplish this is to give each module a name that reflects its function, such as ADIN, and RS-232. Interaction between modules must be simple.

Initially, all coding should be done on paper. Programming aids are important, such as comments that document program functions, and descriptive variable names. Spaces, indentations, and line feeds help the programmer produce readable code. Other critical points include initializing all variables and avoiding undocumented features. A variable should never be assumed to be within any range unless it is assigned. Undocumented features may not be available in later parts or versions of assemblers or compilers.

After each module is written, it should be checked for errors before it is entered into the computer. Entry, compilation, or assembly should be followed by another careful reading of the program by at least two programmers. The time used in this stage can be made up later on.

The next stage of development, debugging, often results in long project delays. Many programmers during this phase are anxious to see results instead of thinking about solutions to problems. Others are always ready to point an accusing finger if something goes wrong. An open mind and careful planning can decrease debugging time.

In addition to keeping up to date program listings and a log of what has occurred, a bug book may help uncover bad programming habits.[13] Stubs (dummy modules with a set response) are also useful for unfinished hardware, software, or program simplification.

Establishing test organization

Deciding when to do various tests and what to do in case of a failure is another important part of system design. Dedicated diagnostic (offline) tests are performed when the system is totally dedicated to testing itself. They can be done automatically on startup or power on, or under user or service control. In some cases, special connections or switch selections must be made, or special hardware must be installed.

Common diagnostic tests include RAM checking with various patterns at all locations, read only memory checksum tests, and an exercise of disk and tape drive systems.[10,11] I/O can be checked with known inputs, and known test patterns can be output. Some systems even allow for wraparound tests, connecting the output to the input. A good method of finding intermittent problems in a suspect part of the system is to test repeatedly.

When performed during normal system operation, online testing does not interfere with normal operation. The amount of online testing performed is proportional to the amount of time available, as well as the testing required to meet the system's reliability goals. Typical online tests include having an I/O port check input data. Out of range variance should be searched for from sample to sample. Power supply voltages can be checked with A-D's. Other tests include checking calculations for out of range results, and checking several RAM locations from each memory chip for correct operation. During testing, it is dangerous to wait forever in polling places. Thus, programs should always fall out and set the appropriate error flags upon encountering a failure.

An open mind and careful planning can decrease debugging time.

Error output should be audible and/or visual. Specific error messages inform the user as to what type of problem has occurred. These messages also aid in repair. A common method uses a 2-digit number for each problem. However, a full text display of errors is more desirable.

Errors that occur for a short time can be ignored as noise in some applications. In these applications, the system should have several error inputs before setting an error condition. When a single error input sets an error condition, hysteresis should be added to avoid transients.

When an error occurs, systems should switch in a backup or redundant system, go into a default condition, and set all outputs to a predetermined state.

When an input peripheral fails, using the last good data or a predetermined set value allows the system to continue to operate and to execute a more detailed self-diagnostic test.

Until one complete method can replace the many interdependent checks and tests discussed in this article, the designer will have to rely on painstaking care in design, and accurate communication with all development team members. To create good, reliable, microprocessor based systems, good, reliable, design procedures are a must.

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Acknowledgments

This article was done under the direction of Dr John L. Pokoski, Dept of Electrical Engineering, University of New Hampshire.

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High 704 *Average 705* *Low 706*

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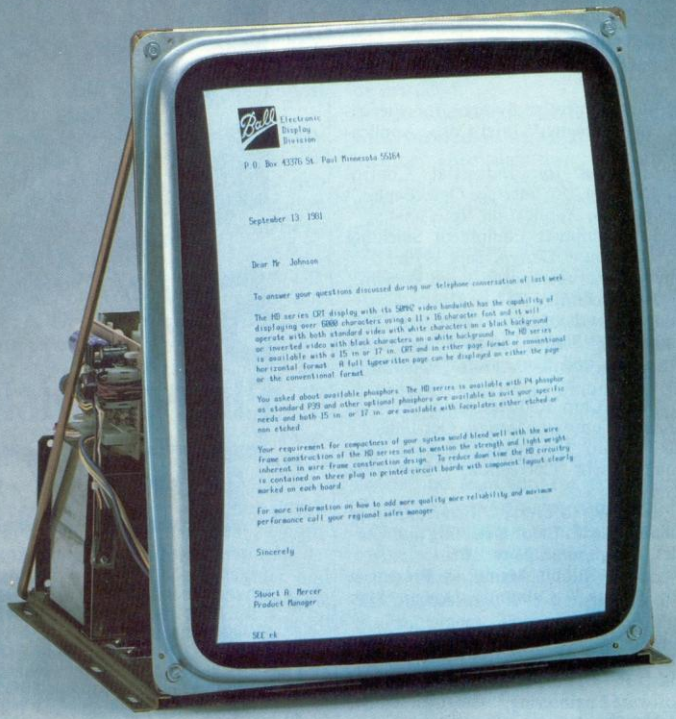

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DESIGN DATA BASES AND DESKTOP MICROS

Using the humble PC to extract database information from schematics lets designers focus on creativity instead of paperwork.

by Bruce E. Gladstone and Paul D. Page

Using computers as drafting tools is a step toward increased designer productivity. If the process stops at merely creating drawings, however, a large part of the computer's potential is being ignored.

All engineering drawings can be viewed as processes that are used to create manufacturing data bases. For example, the process of drawing a schematic diagram creates a design data base that contains all of the electronic engineer's thoughts on such subjects as part types, connections, values, and component tolerances. However, creating a data base from a schematic diagram is a much less controlled process than most people think.

To illustrate, consider the relatively simple process of creating a mailing list. Each item (ie, name, address, and phone number) is entered in a specific field on a specifically designed form. Contrast this

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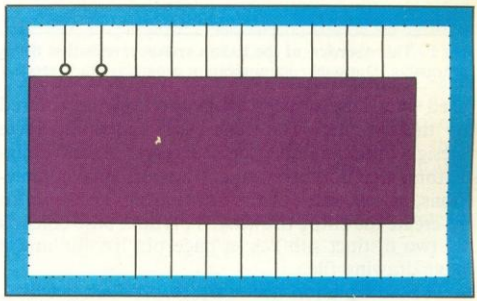
Paul D. Page is vice president of research and development at FutureNet, where he is responsible for all design and development. Previously, he was president of Futuredata Corp. Mr Page holds a BS in physics plus an MS in computer science from the University of California, Los Angeles.



ordered process with that of creating a schematic diagram. The parts may be located anywhere on the drawing; the part numbers may be above, below, to the left, or to the right of the part symbol; and connections can be directly drawn or derived via signal names. This list could go on and on.

The key problem in the design of a usable schematic entry system is to provide a way for the system to find and properly associate the data items without imposing undue restrictions on the designer. In addition, the entry system design must allow for future extensions without requiring complete software revisions.

One approach, taken by FutureNet, allows the designer to use familiar standard symbols, drawing conventions, and formats to enter and edit a schematic drawing in graphic form. Called the DASH-1 schematic designer, the software system operates on either the IBM PC floppy based or the IBM XT Winchester based personal computers. The DASH-1 package automatically creates an easily

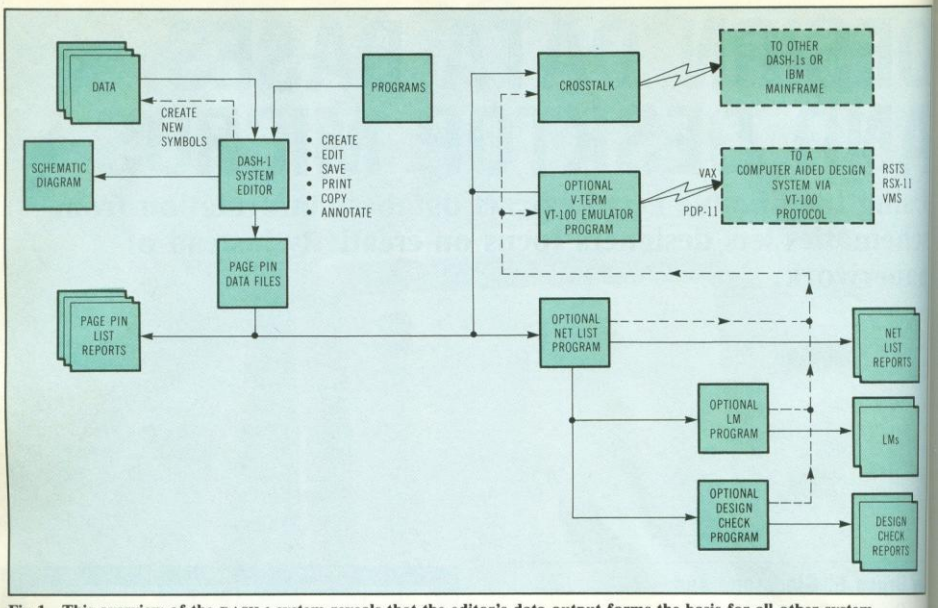


Fig 1 This overview of the DASH-1 system reveals that the editor's data output forms the basis for all other system processing. Optional communication programs allow access to mainframe resources.

used data base directly from the drawing entered by the designer. The data base, called the Page Design File, contains part numbers, circuit designators, pin numbers, signal names, and connections, as well as all of the information necessary to re-create the entire drawing. This data base consists of two distinct subfiles: a page pin list file and a page drawing file.

The information necessary to produce net lists, lists of material (LM), design check reports, wire lists, and simulation program input is provided by the page pin list file. A page drawing file provides the additional data necessary to re-create the actual schematic drawing in another system.

Fig 1 shows the interrelationship of the data files involved in the design process. Pictorial part libraries contain the parts' diagrams, part numbers, pin descriptions, pin numbers, and a location field for the circuit designator. Descriptive part libraries contain the full part numbers (eg, 74LS04 might yield a complete part number SN74LS04), part description, vendor, cost, and other items. Schematic drawings exist as a compacted drawing file used within the DASH-1 system. These files have been optimized for speedy in-system processing but are unsuitable for transfer to other systems. On the other hand, the page design files contain the same information but in a readily usable form. These ASCII "source files" are easily read and modified for all the previously mentioned applications.

So far, only a single page of a schematic has been considered, but most designs consist of more than one page of schematic drawings. In general, the contents of these multiple pages must be combined into a single design file. Two types of information exist on multiple pages. One type occurs when signal names are used to connect from one page to another. Another type comes into play when packages have multiple elements that may not all be located on the same page (eg, a 74LS00 consists of four separate 2-input gates). In the DASH-1 system, the net list processor's task is to handle both of these situations. Nets labeled with the same signal name are combined into a single net and the page references are noted. Parts labeled with the same designator are combined into a single part reference.

Capturing and extracting data

The Table illustrates how the DASH-1 schematic designer extracts the various types of information. Each alphanumeric field is tagged with an "attribute." The pin list and drawing file processors search the schematic's data base and recognize each alphanumeric field's class.

Fig 2 shows a schematic segment and illustrates the types of data included there. Clearly, an LM can be created from the part number, part value, and circuit designator data fields. Similarly, a net or wire list can be created from the data on pin

System Attributes	
Attribute Value	Description
0	Pin description
1	Pin number
2	Circuit designator
3	Part number
4	Part value
5	Signal name
50	Drawing title
51	Drawing number
52	Drawing revision
53	Date
54	Drawing page number
100	Ground (power)
101	5 Volts (V_{CC})
102	Nonprinting pin number

numbers, circuit designators, signal names, and interconnections. Other schematic information includes data titling, part location, and notes.

Fig 2 also illustrates other DASH-1 database characteristics. Dotted lines enclosing the 74S138 block indicate the alphanumeric fields that belong to that part. The dotted lines create a "cell" within which the part number and circuit designator fields can conveniently reside. The numeral 2 in the cell's upper left corner is an example of a sequential reference number that the DASH-1 software generates for each new symbol entered. Consider the usual design process in which the electronic engineer creates the logic design and the drafting department creates the printed circuit (PC) design. In the Fig 2 sample, the circuit designators are assigned during the PC board's creation. The reference number allows the two processes to associate the engineer's logic functions with the PC board designer's circuit designators.

In the right hand corners of the 74S138 symbol cell, the 16 in the upper corner is the 5-V pin connection to the chip while the 8 in the lower corner is the ground pin connection. Fig 3 shows the attributes of each field within the cell. Note that 5 V and ground have attributes of 101 and 100, respectively. This allows the page pin list processor to tag these pins with the signal names 5 V and ground. To avoid cluttering drawings, the DASH-1 software also features a default print suppression of all fields with attributes greater than 100.

The software allows up to 128 separate attributes (0 to 127). So far, only 13 attributes have been assigned. The attributes 80 to 99 and 120 to 127 have been left free for the user to allocate as needed. Since the pin list processor will associate the attribute with the field, special classes of information can be extracted from the schematic as necessary. If the special fields are within the chip cell, they will be associated with the chips; if they are outside the cells, they will be general notes.

Multiline buses present another special case. Here, a single line is used to represent many lines. Fig 4 shows the bus labeling conventions used by the DASH-1 schematic designer. The signal designation DATA<07:00> represents an 8-line bus. Each of the signal lines "tapped off" the bus is given a number. The pin list processor associates these numbers with DATA00 through DATA07 and gives the signal lines the proper names.

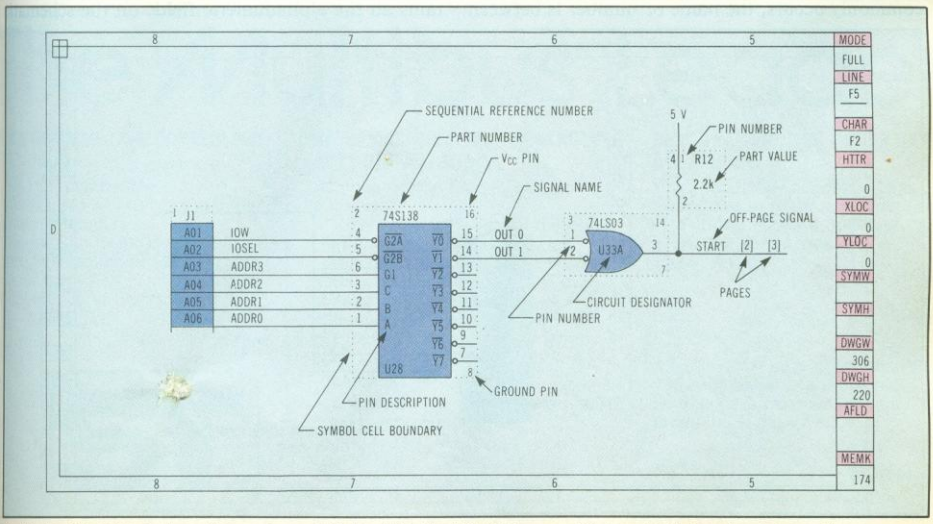


Fig 2 In this DASH-1 schematic sample, each field within the dotted lines constitutes cells that are treated as units. Signal names appear above or adjacent to the line they refer to.

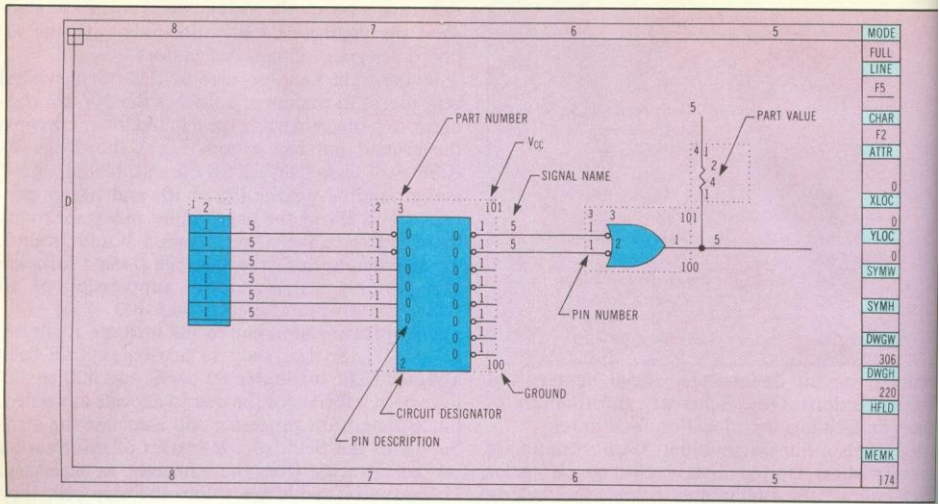


Fig 3 Attributes in the DASH-1 display allow the pin list and drawing file processors to search the data base for the specific kinds of inputs they require. Provision is made for user defined attributes and, by extension, user created processing programs.

Attaching pin numbers and signal names to lines in the schematic illustrates the need for certain conventions. The DASH-1 package attempts to make these conventions as unrestrictive as possible, but it must be clear that a signal name floating between two lines cannot be reliably associated with either. For that reason, the signal name or pin number field must abut the associated signal line. If, as commonly occurs, the name or number is between two lines and is touching both of them, then the name or number is associated with the line below or to the left of it.

Postprocessing of schematic diagrams

A page pin list file is the primary mechanism for passing information from the schematic design to the other postprocessing functions. This file contains all the alphanumeric fields on the schematic

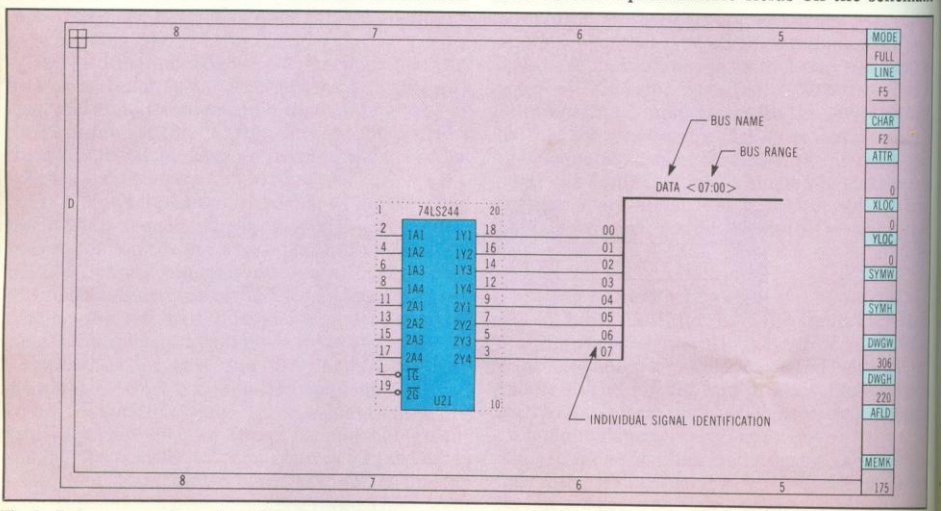
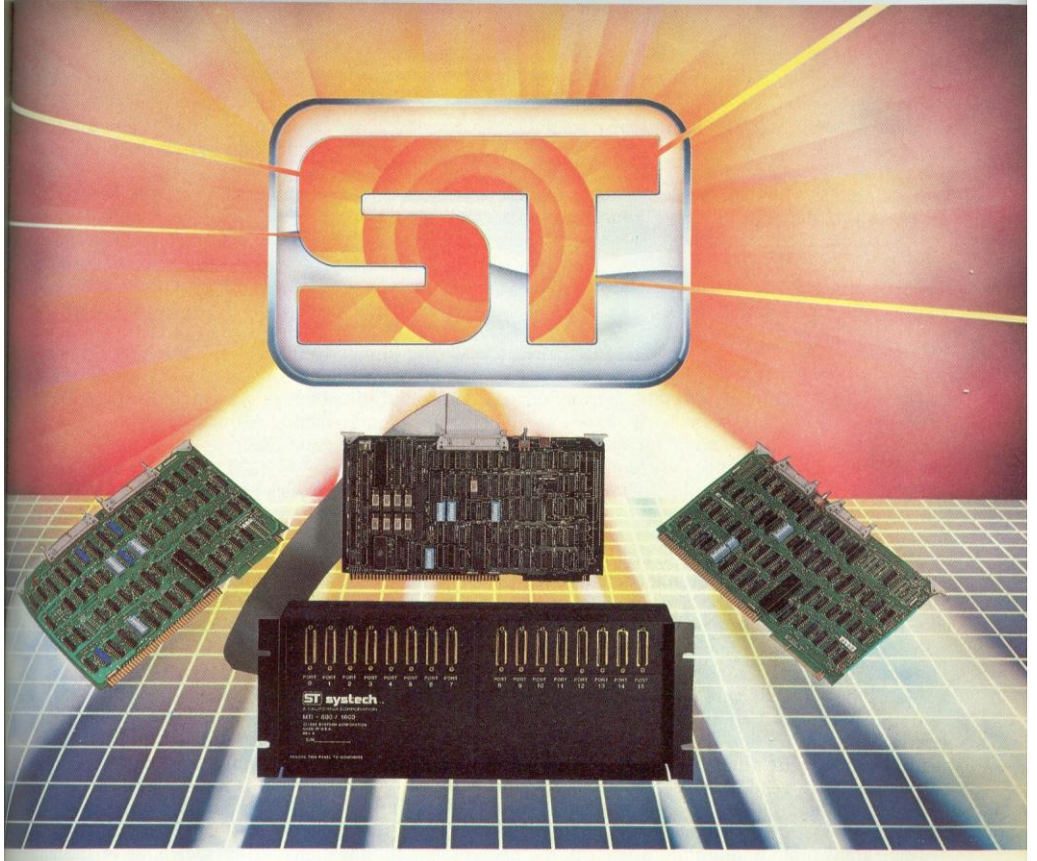


Fig 4 In bus conventions, signal lines attached to a bus (with name and range designators) can be run around the drawing as a single line. Signals can then be broken out of the bus line at their various destinations.



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drawing, except pin descriptions. Thus, it contains all the "intelligence" of the schematic diagram—an engineer could conceivably read the page pin list and discern the design.

As mentioned, the net list processor combines its data with the page pin list files to create a complete design. All of the page pin list file information is preserved, including that related to part numbers and values.

Using a micro such as the IBM PC as a design aid has many advantages.

The net list processor reorders the data contained in the page pin list files, where the connection data are in the order of reference and pin number. In the net list output, the connectivity data are in the order of signal name, pin number, pin number, . . ., pin number. This is the normal net list or string list format used by most circuit board layout systems and wire list processors. Because both connectivity and part information have been included in the net list output, these data are also suitable as input data for circuit simulation programs.

Producing an LM is the next step in the process. The net list processor's output forms the LM processor's input. In this case, the part number and part value data are used as the keys to access the descriptive part files and produce an LM. The LM has full vendor part numbers, user part numbers, part descriptions, vendors, costs, quantities, circuit designations, and other information that individual companies might require.

There are two more important aspects to the LM process. First, each company may have its own standards for part numbers and material list layout. To answer these needs, a part file editor is included that allows user defined fields and field sizes. Also, the LM processor is written in BASIC for easy user modification.

Second, creating part numbers and descriptions such as resistors and capacitors could present a problem. For example, the part value 10k for a resistor will create the part number "RC07GF103J" and the description "10k Ω, 1/8 W, 10% Carbon Composition Resistor." Clearly, one should not enter every possible resistor and capacitor value in the part description file. The DASH-1 LM processor includes three procedures for deriving part numbers and descriptions of this class. One produces data for RC07 resistors, the second for tantalum capacitors, and the third for ceramic capacitors. These are the default results for resistors and for polarized and nonpolarized capacitors. The user can easily edit the resulting LM file to modify the entries for any nondefault-type parts. Users can also modify the BASIC program itself to include other default part types.

The design check program uses the net list processor output. This program produces a series of reports to help the engineer verify the correctness of the design's connectivity information. The first report lists all unconnected pins by their reference number or circuit designator, and the second lists all missing page references. While these lists may not represent errors *per se*, they certainly indicate suspect areas. All signals that connect to single pins, which are definite errors, compose the third report. The fourth report lists all signal names that appear on only one page, and the fifth report lists all the circuit elements sorted by part number. Often the fifth list indicates areas where resistor and capacitor values can be combined to reduce inventory requirements. A final report shows all 5-V and ground connections.

Uploading and downloading data

Finally, there is a need to upload and download data from a central system. Options to the DASH-1 system include two data communication packages. The first (VTERM) is tailored for communication with VAX and PDP-11 based systems. It turns the IBM PC into a VT-100 look-alike. Communication can be at rates up to 500 characters/s. Since a typical design of 100 chips is represented by a net list file of about 120k characters, a design file can be transmitted in approximately 4 min (assuming the host system can accept data at a full 500 characters/s). A second communications package, Crosstalk by Microstuf, Inc, is a more general package not tailored to any specific host computers.

Using a microcomputer such as the IBM PC as a design aid has many advantages. One of the most important is gained access to more general data bases in any type of design environment. Another benefit is the possibility of integrating the system into larger corporate design environments. In the near future, most host systems can be expected to support Ethernet. At that point, design files can be uploaded and downloaded at much higher rates. Indeed, it should be possible to use all host system facilities to aid in the design process.

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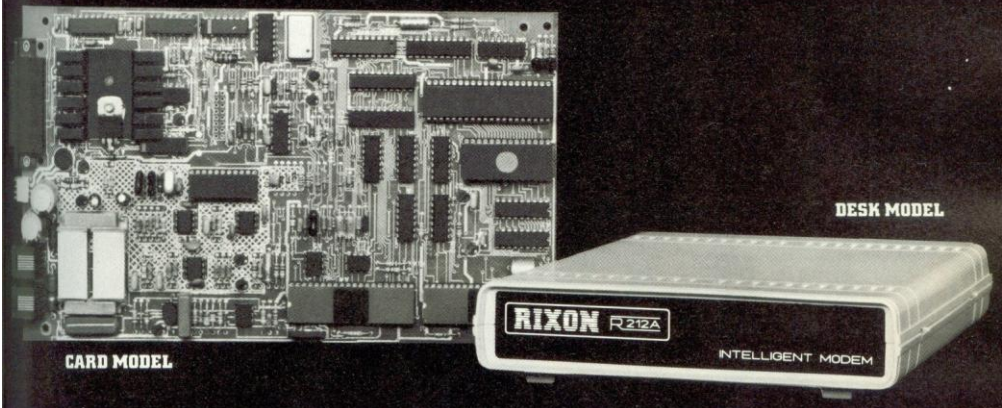

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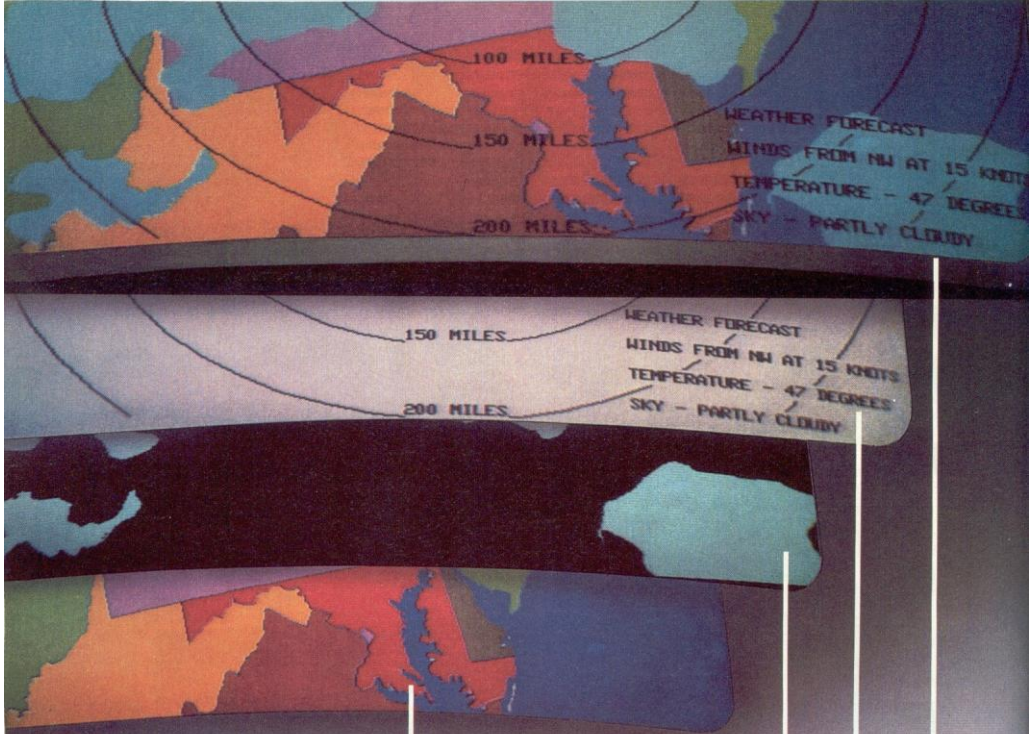

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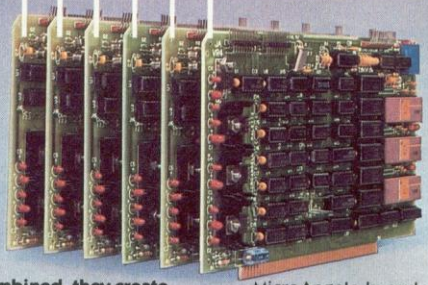

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SPECIAL REPORT ON

MICROSYSTEMS SOFTWARE

This month's Special Report encompasses two of the most exciting and volatile elements in today's computer industry: 16-bit microcomputers and their associated software. Thanks to these two factors, the face of modern computing is changing, for better or worse, at a pace that leaves designer's heads spinning. The net result is that solutions that were technically plausible a year ago are no longer valid.

The people who are paid to look at our computer present and deduce our computer future are fond of citing a familiar marketing analogy. Razors and blades are equated with hardware and software, and dubbed the commodity aspect of the computer industry. The theory is that soon microcomputer hardware will be practically given away as a vehicle with which to sell software. Maybe.

In any case, as software issues represent an increasing part of the microcomputer system design exercise, software suppliers—large and small—are gaining credibility. While trying to adjust to the radical dislocations caused by the intrusion of corporate giants like AT&T and IBM into their provincial world, software companies are also being forced to keep an eye on technology. Issues of portability, performance, applications support, and the user interface must be addressed quickly. The problems inherent in these issues, unfortunately, are not so speedily solved.

In this Special Report, one of the largest system software suppliers copes with the portability problem via the C programming language. Another boosts the performance of a popular 16-bit operating system by fine tuning its I/O mechanism. A third, traditionally viewed as a hardware supplier, calls into question our fundamental notion of an operating system and provides a rationale for an alternative. Purportedly, the alternative is easier to use, more logically structured, and friendlier than any method devised to date to control the activities of 16-bit computers.

For designers and users, OEMs and integrators, it is an exciting and confusing time. And, while no manufacturer has yet given away hardware scot-free, the razor/blade analogy lingers. For the time being, the hardware segment of the industry is likely to continue in its smaller-cheaper spiral. The software industry, however, is proving to be much less predictable.

That old axiom about the capriciousness of the weather applies equally well to the present microcomputer software scene: "If you don't like it, wait a minute. It's sure to change." The long range forecasters guiding tomorrow's software winners are under pressure to guess right technologically today. We hope that the trends exemplified by this Special Report help keep the rain off their parade.

Chris Brown
Technical Editor

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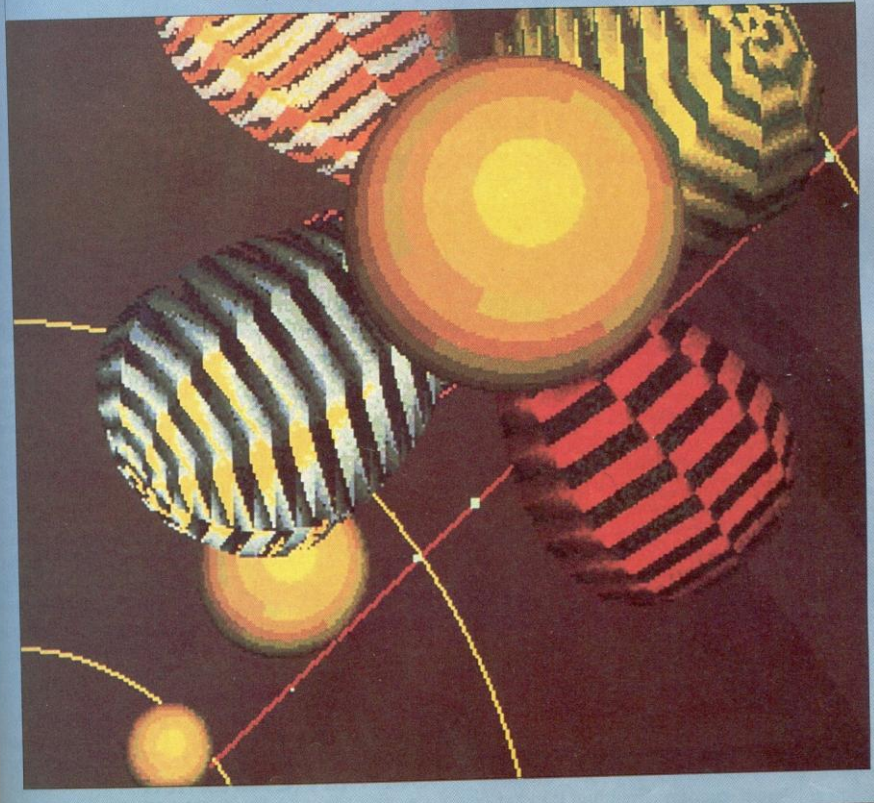

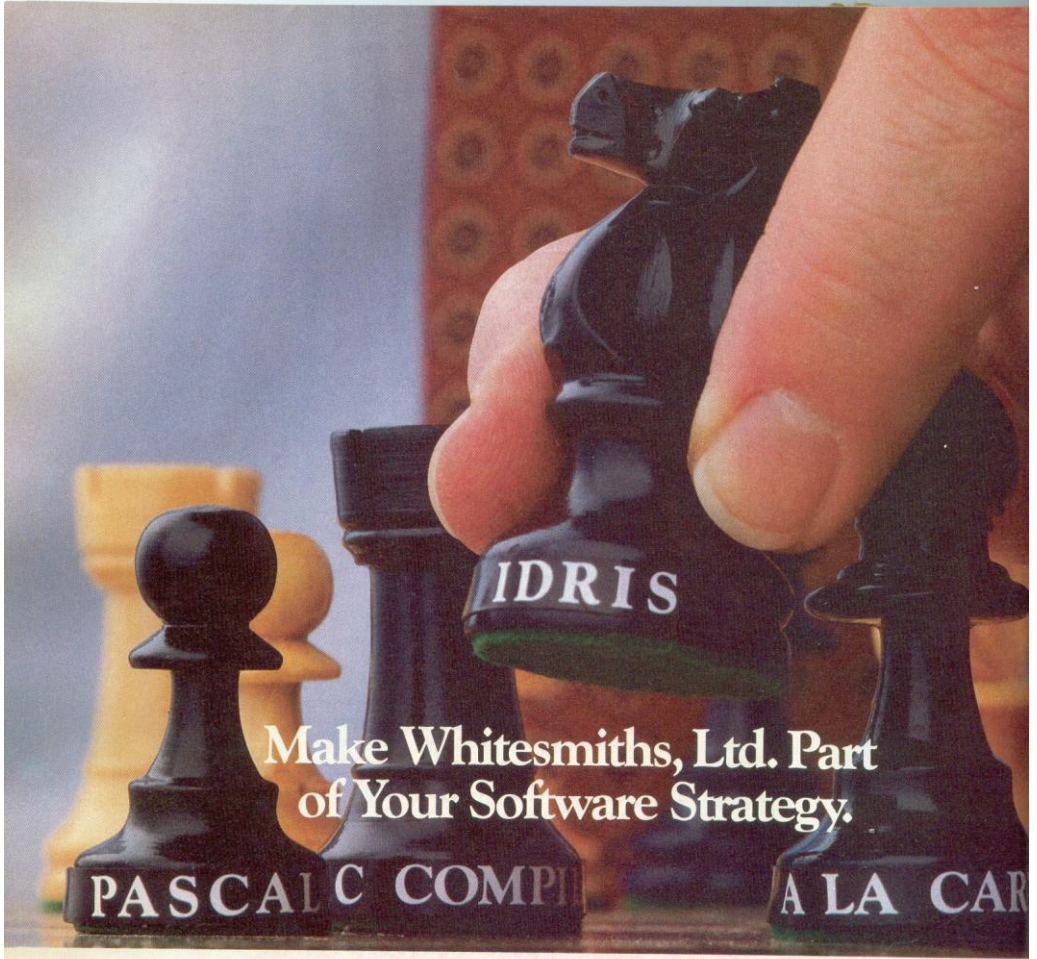

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OPTIONS ABOUND IN 16-BIT OPERATING SOFTWARE

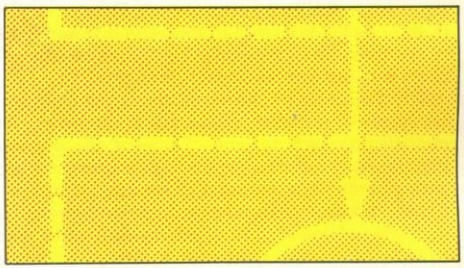
As trends are established amid the confusing proliferation of products and philosophies on the 16-bit operating system scene, strange alliances are forming between hardware and software manufacturers.

by Chris Brown,
Technical Editor

The quest for an appropriate operating system that meets the broad range of 16-bit microcomputer users' needs is resulting in an agonizingly familiar situation. Both hardware and software manufacturers, having cast about for some time in search of the ideal set of instructions to control 16-bit microcomputers, are grudgingly conceding that no clear-cut ideal exists. These seekers of software are now adopting the next best alternative: force-fitting existing, often inadequate large and small operating systems to 16-bit hardware. Consequently, mutated derivatives of Unix proliferate, while souped-up CP/M versions are assigned suffixes and prefixes.

For users, many of whom traversed an identical development curve with their first, 8-bit microcomputer operating system, the situation is frustratingly familiar. Once again, resiliency is proving to be a virtue as users are forced to adapt to awkward command syntax, serpentine directory and menu structures, and voluminous documentation sets. Compounding the situation is the confusion resulting from the more sophisticated nature of the 16-bit machine.

A valid question arises, especially in high performance, multi-user settings, concerning who has the main responsibility for manipulating an operating system. Is the primary interface with a multi-user system really at the user level? Or, by their very nature, do such systems demand the ministrations



of a sysop (system operator) to be effectively exploited? If the latter is true, is it fair (or realistic) to expect friendly, as well as functional, operating systems? Probably not.

In addition to friendliness and functionality, portability must also be considered. Assuming most users want hardware that performs a wide range of applications (text preparation, business operations, periodic bouts with programming), the operating system's ability to accept a broad range of applications is crucial. In fact, as the amassed software base continues to swell, the issue of portability is becoming preeminent. Thus, multifaceted languages like C, which foster portability while supporting operating system functions, are coming increasingly to the fore.

Beyond the immediate issues raised by the ongoing debate over existing operating software options lies a more fundamental question. Is the traditional concept of a multilevel, resource managing operating system actually a thing of the past? Will, in fact,

TABLE 1

A Sampling of 16-Bit Operating Systems

Company	OS	Processors Supported	No of Users	No of Tasks	Price ($)
Charles River Data	UNOS	68000	64	256	1200
Digital Research	CP/M-86	8086/8088	1	1	250
Digital Research	MP/M-86	8086/8088	16	255	650
Digital Research	Concurrent CP/M	8086/8088	1	4	350
Digital Research	CP/M-68K	68000	1	1	–
Industrial Programming	MTOS	8086/8088	255	4096	9500
Infosoft Systems	Multi/OS	68000, 8086/8088	16	1	250
Mark Williams	Coherent	68000, Z8000, 8088	–	–	–
Microsoft	MS-DOS 2.0	8086/8088	1	2	60
Microsoft	Xenix 3.0	8086, 68000, Z8000	hardware dependent		
Phase One Systems	Oasis-16	8086/8088, 16000, 68000	32	32	1500
Pick Systems	Pick System	8088, Z8000, 68000	hardware dependent		
Softech Microsystems	p-System	8086, 68000	1	1	350
Western Electric	Unix System V	68000, iAPX 286, 16032	–	–	43,000
Whitesmiths Ltd	Idris	68000	–	–	1300

future computers offer users "environments" in which to write text, analyze numerical relationships, and store and retrieve data? Are present-day manifestations of such environments as Visicorp's (San Jose, Calif) VisiOn, Lotus Development's (Cambridge, Mass) 1-2-3, and Apple Computer's (Cupertino, Calif) Lisa pointing the way to tomorrow's human/computer relationship?

The vagueness of the word "environment" certainly gives software producers great leeway in constructing such systems. Some of the systems mentioned are nothing more than a user interface sitting atop conventional operating software. Others, however, like Apple's Lisa, do represent a new way of looking at operating software. (See "Lisa's Alternative Operating System," by Bruce Daniels, *Computer Design*, Aug 1983, p 159.) Present popularity of such alternative approaches does seem to indicate that the time is ripe for a new definition of operating software.

For users, many of whom may be well served by bundled versions of the "big three" applications (word processing, spreadsheeting, database managing), a simple and limited environment could actually be a blessing. The drawback of such an approach is the inevitable reduction in variety resulting from bundled environments. Allowing systems and users to grow together in sophistication is imperative.

The scramble for software acceptance has resulted in a confusing array of options for the operating system user. A company like Digital Research Inc (Pacific Grove, Calif), which offers an extended family of 16-bit operating systems based upon CP/M, is one case in point. Companies such as Pick Systems (Irvine, Calif), Mark Williams (Chicago, Ill), and Phase One Systems (Oakland, Calif), also bring specialized operating software targeted at specific applications to market.

As if this weren't enough, the situation is exacerbated by the number and variety of systems falling under the flag of Unix. Unix look-alikes, derivatives, subsets, supersets, and even generic versions, present a challenging exercise in subtlety detection. Adding to this panoply of functions are realtime systems destined for use in data acquisition, automation, and control applications. Here, performance-tuned, full-featured systems stand in stark contrast to stripped-down executives that often reside in read only memory (ROM).

It is a fascinating and rich store of 16-bit operating software that confronts both designers and users (Table 1). However, sorting it all out can present a problem. A good place to begin such an activity is with one of the largest suppliers of operating software in the business, Microsoft Inc (Bellevue, Wash).

Consistency in system design

To its credit, Microsoft has taken a pervasive approach to the operating system dilemma. From the simplest to the most complex levels of system sophistication, Microsoft is attempting to make all of its operating systems compatible, and similar in appearance. This effort is particularly evident in the company's recent release, MS-DOS 2.0.

Designed for single-user, 8088 based microcomputers like the IBM Personal Computer, MS-DOS 2.0 is intended to bridge the gap between simple, single-user systems and more complex, multiuser/multitasking machines. Microsoft's product offering in this latter arena is Xenix, a Unix derivative. By using the same screen formats and graphics

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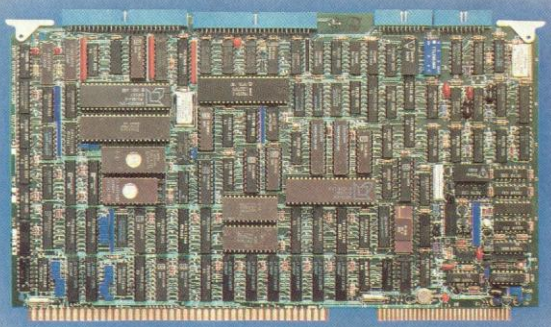

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drivers for both Xenix and MS-DOS, Microsoft eases the user transition from one system to the other. In addition, common system calls and directory structures foster a sense of familiarity between the two systems. And, in a partial concession to the mass of CP/M based software in existence, MS-DOS 2.0 emulates CP/M-80 system calls.

In general, the differences between MS-DOS 2.0 and its earlier versions take two forms. Some additional features have been added, and enhancements that allow the operating system to interface with its more sophisticated sibling, Xenix, were constructed. In the area of additional features, several are noteworthy.

First, an American National Standards Institute (ANSI) terminal driver is supplied. Of interest mainly to original equipment manufacturers (OEMs), this feature allows standard interface emulation between the terminal and programs running under the disk operating system. The X3.64-1979 standard supported may help foster an industry norm and promote software transportability for graphics.

Another new feature in MS-DOS 2.0 is installable device drivers. Now, when a new peripheral is to be connected to the system—such as an international keyboard, tape drive, or plotter—a device driver can be incorporated at boot time to configure the system accordingly. If users are incapable of writing their own driver, however, the manufacturer of the device must supply it. Microsoft will not have a library of drivers available. In the long run, this feature will result in a greater diversity of hardware capable of being used with MS-DOS 2.0 based systems.

Input/output (I/O) redirection, filtering, and piping are also supported by MS-DOS 2.0. These suspiciously Unix-sounding features provide users with great flexibility. Feeding the output of one program to the input of another, or redirecting files around the system, are abilities that have not been used to a great extent by previous 16-bit operating systems. Their inclusion in the MS-DOS command repertoire bodes well for the sophistication of applications running under this operating system.

Another feature of the disk operating system (DOS) is dynamic sector caching. Disk sectors can be buffered according to a least recently used (LRU) algorithm. This speeds disk operations and is particularly apt for database manipulation.

One of the most notable features of MS-DOS 2.0 is its hierarchical file structure based upon Xenix system calls. Here Microsoft's intention to provide compatibility between low and high level operating systems is most obvious. In this tree-structured filing system directories, subdirectories, and subsubdirectories proliferate (Fig 1). This potentially confusing situation is addressed by the TREE command, displaying the entire system file structure. By specifying paths to directories, users can navigate this maze of optional file locations.

MS-DOS 2.0 also has the ability to run background tasks. While not true multitasking, this feature is useful to single users. By allowing background processing to take place during processor interrupt time, specially configured tasks like electronic mail and printer spooling can be accommodated while the system performs a foreground application. Batch files of commands can also be created and, by using conditional identifiers such as FOR, GOTO, and IF, strings of commands and subcommands can be logically chained together. When operating in the batch (BAT) mode, command execution is serial and automatic.

Unfortunately, there are negative aspects to Microsoft's latest DOS. For one, advanced features like I/O redirection, batch mode operations, and piping are not particularly easy to use. The primary reason for this is the elaborate and often illogical command syntax required to activate these functions. For example, in a system that has several subdirectories, the following command is required to copy a file from one directory to another:

```
COPY C: MP\PRJOE.MP.C:\ BOS WKR\JOE\SLRY
```

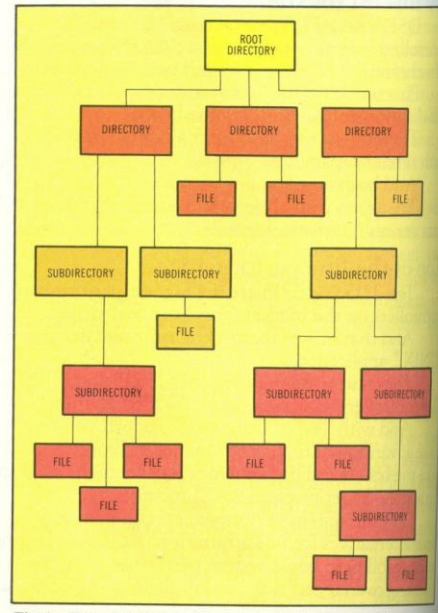

Fig 1 Tree-structured, hierarchical directory and file systems of MS-DOS 2.0 provide great flexibility but foster user confusion. The operating system includes commands (TREE, PATH) to help users navigate through the maze to the desired file.

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Here, a copy of Joe's multiplan salary records are transferred to a new directory. A backslash character denotes separate directories, and the sequence of commands beginning with \ BOS describes a path through the tree-structured filing system. The necessity for users to specify these paths to the copy command adds complexity to their interactions with the operating system.

It might be argued that only advanced users will avail themselves of the operating system's advanced features. Therefore, the complexity of the command sequences is of little matter. It can also be argued, however, that by placing many of its most desirable and convenient features beyond the ken of casual users, the benefits of this powerful DOS may be lost on the majority.

In all, features inherent to MS-DOS 2.0 provide savvy users with a rich command library. In addition, it seems logical to assume that as Microsoft slants its lower level operating system toward its Unix-derived Xenix, a migration path will be established. Thus, the transition to Unix-like systems will aid Microsoft customers looking for the power and features of multi-user/multitasking settings.

The single-user/multitasking area between MS-DOS 2.0 and Xenix, presently vacant, may eventually be served by a multitasking version of MS-DOS. If this is the case, Microsoft's commitment to Unix-like operating systems can be expected to shape any entry. By familiarizing users with the structures and concepts of Unix early on, their conversion to evermore Unix-like systems is eased, if not assured.

At the high end of Microsoft's product line reigns Xenix. Of all the Unix-derived operating systems that abound, Xenix certainly enjoys the highest visibility and the greatest momentum. Its most recent incarnation, Xenix Version 3.0, offers a tamed Unix-like operating system that combines the benefits of a rich development environment with the good manners of a practical multi-user business system. Version 3.0 is derived from Unix System III and Unix Version 7. It also contains some Berkeley Unix routines.

The system is supplied in three parts: the timesharing portion, the development system, and the text processing system. The timesharing portion contains the Xenix kernel plus many utilities. By itself, this segment of Xenix is capable of administering multi-user hardware. Both the development system and the text processing system can be acquired as needed.

Version 3.0 of Xenix also offers features not available earlier. Shared data areas can be accessed by many users via a new system call. A mouse interface allows this new version to be used with systems like Apple's Lisa. A fixed stack analysis utility eases program development in the C

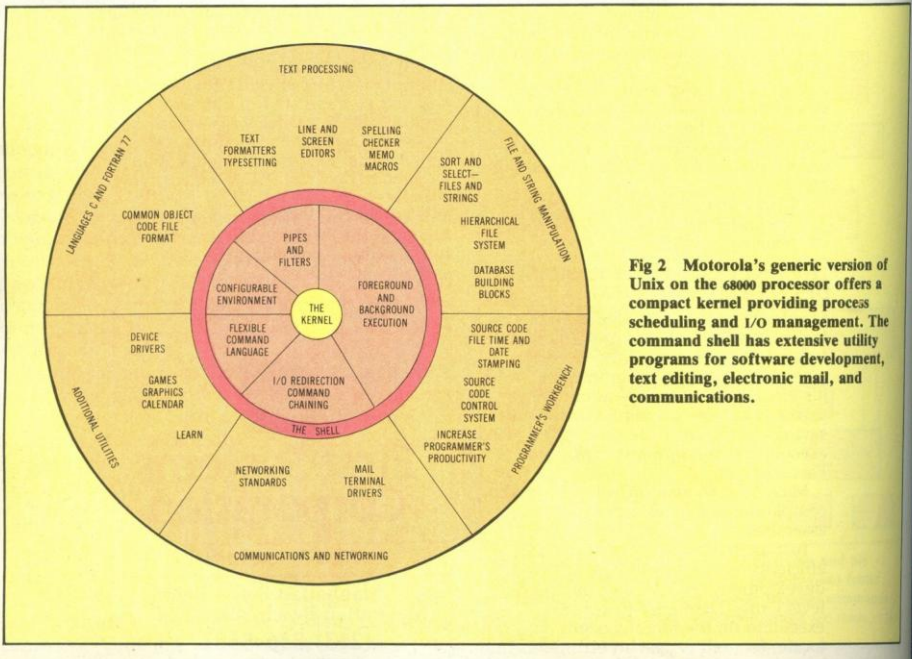

Fig 2 Motorola's generic version of Unix on the 68000 processor offers a compact kernel providing process scheduling and I/O management. The command shell has extensive utility programs for software development, text editing, electronic mail, and communications.

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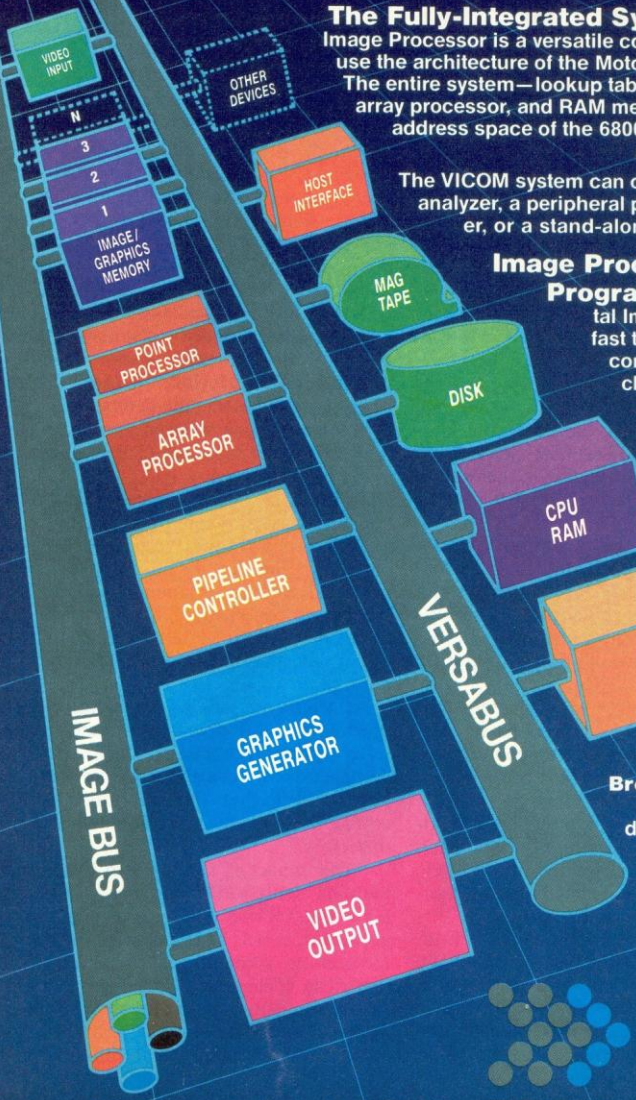

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TABLE 2

Revised Unix Licensing Fees

Commercial Licensing Fees ($)	
Initial CPU	43,000
Each additional CPU	16,000
Upgrade from System III	1,000
Upgrade from 32V	6,000
Upgrade from Version 7	18,000
Upgrade from Version 6	26,000
Upgrade from PWB	16,000

Academic Licensing Fees ($)	
Initial request for all CPUs	800
Each additional CPU	400
Upgrade from System III	0
Upgrade from other Unix	800

Administrative Fees ($)	
Initial request for all CPUs	16,000
Each additional CPU	400
Upgrade from System III	0

language where target processors with limited memory resources are involved. Also, read/write compatibility with MS-DOS 2.0 files is provided.

The refinements evident in this latest version of Xenix are extensive and indicative of Microsoft's commitment to Unix-like solutions. In addition, the effort at compatibility and standardization within the system family is an attractive aspect for upwardly mobile users and OEMs moving into the multi-user world.

All's not quiet on the Western front

Presently, multi-user, 16-bit operating system devotees are divided into two vocal, if not militant, camps. In the near corner, one finds those backing Unix, along with its look-alikes and derivatives. From the far corner glare those allying themselves with non-Unix solutions. Each group attempts to make a convincing case.

Unix fanciers boast of the operating system's richness, development support, and high performance in multi-user settings. Unix detractors rail against the hostile nature of this software development system, its lack of realtime features, and its proclivity for doing unspeakable things to its files in times of crisis.

In addition, Unix detractors will point out that no Unix standard exists. Many third-party software and hardware vendors have whipped up their own flavors of Unix to suit the needs of their one-of-a-kind settings. As a result, complete software transportability across the variegated Unix landscape is an impossibility. Recent developments, however, involving Unix licenser Western Electric (New York, NY) and several semiconductor companies, may alter this situation drastically.

At a heavily attended National Computer Conference press briefing last May, Western Electric, in union with Motorola, Intel, and National Semiconductor, announced plans to develop a generic version of the Unix System V operating system. This generic version will carry Western Electric's blessing, and its certification. Initially, generic System V versions of Unix will be available for use on Motorola's MC68000 (Fig 2), Intel's iAPX 286, and National Semiconductor's 16032 processors. Versions are described by Western Electric as being "functionally complete," and are expected to be released later this year.

According to Western Electric Vice President Jack Scanlon, "These arrangements will increase the availability of application software written for Unix systems." Scanlon adds, "This [the announced collaboration] is a logical follow-up to our January announcements of active support of Unix System V." To bolster enthusiasm for its generic implementation of Unix, Western Electric claims to be going the extra mile in terms of customer support. New training programs and packages, as well as a revised fee structure (Table 2), are being provided by the company.

Third-party marketers of Unix-like operating systems, most of whom provide some value added, are concerned by the Western Electric announcement. For the time being, however, neither large nor small admits to running scared. Predictably, there is no consensus as to whom will be most affected by Western's latest move. In public anyway, each thinks that the other will bear the brunt of the damage.

At Microsoft, one of the industry's largest and most formidable operating system suppliers, cautious optimism prevails. Mark Ursino, product manager of Microsoft's Unix-like operating system Xenix, feels that the immediate threat to his company is being overstated by many industry observers.

"The impact of the Western Electric announcement on Xenix will be minimal," he claims. Ursino adds that, "Once we educate people as to what it all means, it will be business as usual for Xenix." He sees no great import in the collaboration of American Telephone & Telegraph (AT&T) with several semiconductor companies. To him, all this agreement indicates is that "AT&T has added a few more microprocessors to its hit parade." Ursino adds, "It's a hacker's delight. Now you can get real Unix on a microprocessor. Big deal."

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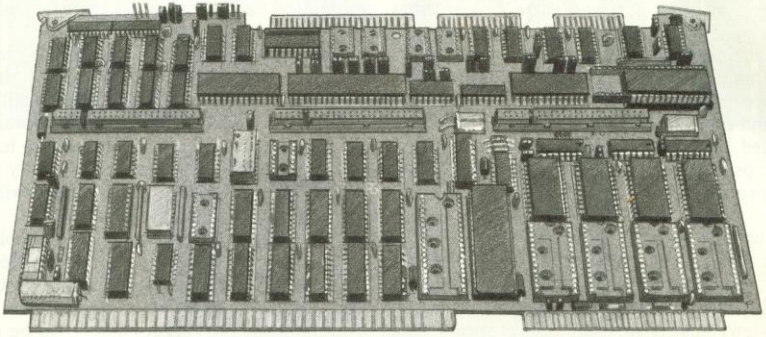

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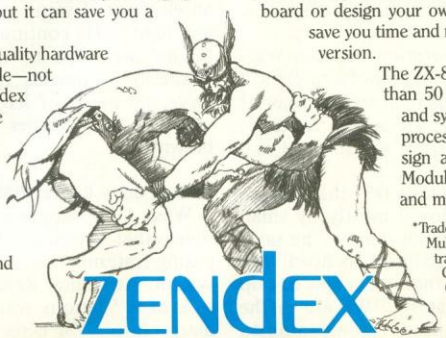

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For Ursino and the folks at Microsoft, that is certainly no bargain. "Unix is a far cry from Xenix," he claims. And he proudly adds that as far as sophistication and functionality are concerned, Unix System V is at least two years behind Xenix in development maturity. Thus, in public anyway, Microsoft is not displaying any emotion over Western Electric's moves in the Unix marketplace. In addition, Microsoft does not expect any measurable erosion of its customer base due to OEMs opting for generic Unix on MC68000 based systems.

"In reality," says Ursino, "there is still no generic Unix. Three semiconductor companies are doing three separate ports for three separate processors, and each company is angling for their own value added." Ursino may have an inside line here since Microsoft is doing the Unix port for Intel's iAPX 286 processor.

Who will be hurt most?

Who is going to be most affected by Western Electric's intention to offer generic versions of Unix to the microcomputer marketplace? In Mark Ursino's view, smaller software houses specializing in Unix-related products will be affected most. Displaying a bit of big corporation chauvinism, he crows, "A lot of these smaller companies don't have a real Unix product with any value added to offer in the first place." Thus, no technical response will be forthcoming from Microsoft. Instead, a promotional campaign designed to educate the masses to the differences between Unix and the well-mannered Xenix is planned.

Small companies in the Unix marketplace tend to disagree with Microsoft's interpretation of the recent collaboration between the semiconductor companies and Western Electric. At Whitesmiths Ltd (Concord, Mass), manufacturers of a Unix-like operating system called Idris, president Bill Plauger feels that Microsoft is facing a serious, possibly life-threatening, situation.

"The effect of the collaboration between Western Electric and semiconductor manufacturers will be much less traumatic for us than for the likes of Microsoft," asserts Plauger. He adds, "AT&T is going right into their [Microsoft's] backyard and that's got to hurt eventually."

In the long term, Plauger feels that the benefits of this situation will be enjoyed mostly by small companies like his. "We are not dumb," he says. "It is not our business to go head to head with AT&T and Unix. If we tried that, we might dry up and blow away." Plauger adds, "We are in the business of making an inexpensive companion to Unix. One that runs nicely on machines in the $4000 to $10,000 range and on which full Unix will not fit."

Plauger feels that the availability of a generic Unix will reduce the number of Unix dialects, as well as legitimize Unix on 16-bit hardware. He also feels that the existence of a generic Unix will spur hardware developers to build better, more capable machines. Such systems will exhibit increased mass storage (at least 20M bytes) and larger random access memory (RAM) areas (1M byte) as standard equipment. These changes are necessary for microcomputers to take advantage of the Unix development library.

When considering Unix in the long term, an inevitable question arises: What are the ultimate intentions of AT&T/Western Electric with regard to the Unix software market? The appraisals of industry analysts differ, but they seem to have reached a consensus on one point: This is only the first of many steps another corporate giant will take into the world of microcomputers.

At Microsoft, the wariness is tangible. "I have no doubt that this is the first of a series of moves designed to do something," cautions Ursino. He adds, "AT&T has made a statement to the microcomputer industry. They intend to be involved." Ursino concludes by saying, "We can all be assured that they will not do something arbitrary now to destroy the microcomputer market for Unix."

At Whitesmiths, Bell Labs veteran Bill Plauger is also convinced that AT&T is in the game for keeps. His assessment of Western Electric's motives is less vague than Ursino's, however. "This is a very aggressive step," he warns. Plauger adds, with the insight of a Bell insider, "Despite all their pious pronouncements to the contrary, Western Electric hopes to tie up the Unix market. They would be foolish not to exploit Unix to the hilt. They are never foolish for very long."

Plauger summarizes his reaction to the situation by saying, "It is not comfortable sleeping next to an elephant. I won't pretend that all is sweetness and light." He continues, with a survivalist tinge, "What we hope to do is coexist with Unix." Whitesmiths intends to do so by continuing to serve the needs of its self-defined market niche: small 16-bit machines incapable of running full-blown Unix.

Putting more C into CP/M

What Unix supporters often find incomprehensible is that a substantial segment of the microcomputing fraternity heartily dislikes AT&T's operating system. At Digital Research Inc, for instance, the lack of a "serious software base" is just one of many reasons for Unix ridicule.

Allen Bebee, Digital Research's director of language development, hopes that recent Western Electric moves on the Unix front will further

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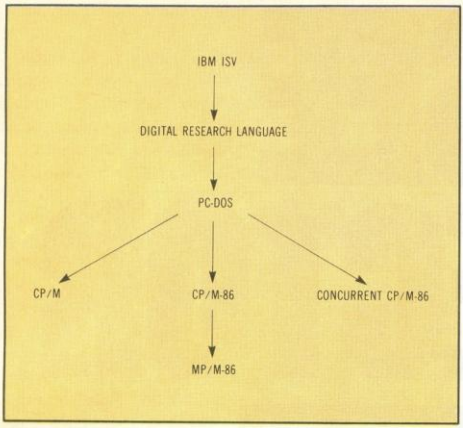


Fig 3 IBM's popular PC-DOS plays a central role in the strategy of CP/M supplier Digital Research. By building bridges to this widely supported disk operating system, the fathers of CP/M hope to bolster their own product acceptance while supporting independent software vendors developing IBM applications.

fragment the Unix community. Eventually, in Bebee's view, this will result in a well-deserved loss of popularity for the operating system. More significantly, Bebee and Digital Research conceive the nature of the 16-bit marketplace in very different terms than the backers of Unix.

Bebee feels that true multi-user/multitasking microcomputer systems will be in the minority in the foreseeable future. He pegs their number at roughly 800,000 installed bases by the end of the decade. The mainstream of 16-bit computing for Bebee is represented by single-user/multitasking systems, of which he expects 5,000,000 to be in use by 1990. Thus, the ability of an operating system to run foreground applications, as well as background tasks like electronic mail, is the wave of the future at Digital Research.

The progenitors of CP/M, that most veteran of operating systems, are not disinterested observers of the 16-bit operating system struggle. In fact, Digital Research is stirring from its lethargy and initiating several technical moves to gain a piece of the multitasking 16-bit operating system pie.

The first of these moves has resulted in what at first glance appears to be a paradox. Digital Research has recently announced that all of its language products and software development tools are available for use under PC-DOS on the IBM Personal Computer. PC-DOS, a product of Microsoft, is extremely similar to that company's MS-DOS. Thus, Digital Research seems to actively support the operating system of the enemy. According to a company spokesman, the game plan at Digital Research goes deeper than that.

Initially, Digital Research hopes to take advantage of the vast base of software support that the IBM Personal Computer has engendered. The strategy is that if Digital Research languages and tools like CBASIC, PL/1, Pascal/MT, Display Manager, and Access Manager are used for development on the Personal Computer, the resulting software will form a bridge from IBM systems to systems running Concurrent CP/M-86. (See Fig 3.) In the short term, Digital Research gains more applications packages. In the long term, it gains a foothold in the IBM marketplace.

According to Carmen Governale, Digital Research's marketing manager in the language division, "By supporting PC-DOS we provide IBM Personal Computer users with a large number of CP/M-86 based applications that will run under PC-DOS." The effect of this strategy on Digital Research's operating system division is less clear.

So, Digital Research is not abandoning the 16-bit operating system market. In fact, its family of 16-bit operating systems is an extended one. CP/M-86, a single-user/single-tasking operating system, is designed for the 8086/8088 family of microprocessors. MP/M-86 is a multi-user/multitasking version of CP/M-86. Concurrent CP/M, a single-user operating system, allows IBM Personal Computer owners to run one foreground and four background tasks concurrently. Thus, it offers a degree of multitasking. The newest family member is CP/M-68K. This C language version of CP/M, designed for use on Motorola's MC68000 processor, offers a full C compiler and runtime library.

Strategies for the future

The philosophy behind offering a high performance operating system for the IBM Personal Computer is well thought out. Digital Research hopes that Concurrent CP/M will prove attractive to IBM users wanting more performance from their hardware, as well as access to the existing CP/M software base. This low cost version of CP/M-86 ($60) includes GSX graphic extensions and a library of graphic device drivers. The GSX extensions allow users to take advantage of many CP/M based graphic routines. In addition, an expanded device driver library supports many graphic peripherals presently unavailable to Personal Computer users. Support is included for Hewlett-Packard color plotters and a variety of foreign and domestic printers.

In addition to this assortment of operating systems, Digital Research is planning new offerings in the 16-bit marketplace. The first step along these lines is its support of the C language. This month, the company will release its version of C and, in addition, will be shipping its rewritten version of CP/M in C. (See article on page 143 of this issue.) Digital Research also intends to have a version of

The operating systems market, circa 1986

by Jean Yates

In the next three years, the most common type of personal computer will be capable of multiprocessing. The number of networked, multi-user systems will also grow dramatically. Major hardware vendors are now working with software houses to standardize operating systems so that microcomputers and mainframes can communicate at the program, file, and message levels.

As operating systems become standardized, applications software will follow similar guidelines. Several significant standards will probably evolve through the coordination of major data processing vendors and microcomputer operating system manufacturers. In particular, the alliance between IBM and Microsoft, which has successfully promoted PC-DOS, will influence the other hardware makers. IBM's adoption and *de facto* endorsement of a standard operating system has triggered the development of an unprecedented volume of applications software. This software boom has in turn strengthened the IBM Personal Computer's position in the market. Could American Telephone & Telegraph (AT&T) or Digital Equipment Corp (DEC) do something similar with Microsoft or Digital Research Inc? Quite possibly.

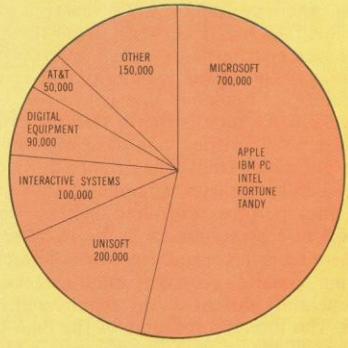
As micro to mainframe communication influences the development of future generations of operating systems, hardware vendors will align themselves with operating system developers. This will be done to ensure the standardization of communications between large mini and mainframe computers, and the vast installed base of micros. If the IBM/Microsoft connection addresses the IBM installed base, then the logical choice for Digital Research is DEC. Thus, a micro VMS operating system could be forthcoming from Digital Research and DEC.

AT&T, due to deregulation, may try to make it on its own. Although the company has one of the finest research and development organizations in the world, its programming resources are limited. At present, it can probably use each high level programmer three times over. In the attempt to retake control of the Unix market (see Figure), the agreement between Western Electric and the major semiconductor manufacturers enlists outside programming resources to develop generic versions of microcomputer based Unix. As for application offerings, it is widely known that American Bell is actively pursuing the acquisition of products from independent software developers.

With the foregoing premise in mind, Yates sees four major families of operating systems at the fore in 1986: Microsoft's MS-DOS family, Digital Research's CP/M and potential micro VMS product, AT&T's Unix family, and IBM's PC/OS family.

In single-user, multitasking environments, Concurrent CP/M and MS-DOS will diffuse into, and dominate, all major microprocessor families. IBM's relationship with Microsoft may be more tenuous than it seems. We project that IBM's extensive line of micro and small business systems will eventually require an IBM controlled product, perhaps to lengthen the life of the Datamaster 5200 line of small business systems.

Through 1985, the success of Microsoft's line of operating systems will depend on the progress of the IBM-Microsoft phenomenon. Although CP/M will still exist in the multi-user market, Microsoft's MS-DOS/Xenix will steamroll through the low end to mid-range, 16-bit market. However, if IBM adopts Pick, or introduces its own operating system, Microsoft may lose market share to AT&T micro-Unix. The recent Western Electric joint development agreement with the microprocessor vendors could significantly influence system developers to



adopt AT&T Unix as supplied by the microprocessor vendors, rather than go to Microsoft for Xenix. Of course, it is possible that Intel could convince Microsoft to become a second source to its AT&T Unix offering, and this then, would become the product that MS-DOS is bridged to.

Microcomputers will serve as intelligent workstations for multi-user, networked environments. This means that microcomputers will be able to communicate with mini and mainframe systems. Since IBM and DEC's installed base of large systems is extensive, networking will begin between these computers and micros running standard operating systems.

Following this theory, the network operating system world will be split into the IBM/Microsoft and DEC/Digital Research camps. IBM/Microsoft will develop MS-DOS to MVS/VM software for communications ability.

Meanwhile, DEC/Digital Research must provide micro to minicomputer communications. This is complicated by CP/M's networking deficiencies. Nonetheless, operating system development is currently under way at Digital Research, and micro VMS operating system may yet surface.

Concurrent CP/M running on Intel Corp's (Santa Clara, Calif) iAPX 286 processor very soon.

With the expansion of its own 16-bit operating system offerings, the company is rumored to be in the midst of negotiations with Digital Equipment Corp (Maynard, Mass). The result of such a collaboration could be a micro VMS-type operating system. Company spokesmen are particularly reticent on this subject but the advantages provided by such an operating system are many. For one, a wide variety of microcomputers could be connected to Digital Equipment's VAX hardware.

Real timeliness for Unix

When the issue of realtime operation is raised by designers of 16-bit operating systems, consternation usually ensues. Generally, an operating system that fosters a rich development environment and a non-hostile user interface is assumed to be a poor performer where realtime responsiveness is concerned. This fact results primarily from the laid-back way such systems manage their interrupts, as well as from the increased complexity that several layers of software functions impose.

The demands of multipurpose, realtime operation are less easily satisfied than those of low level control applications. Unlike the stripped down executives and task managers common in embedded systems, multipurpose operating systems must meet a host of contrary needs. In the 16-bit arena (Fig 4) these needs are usually met by customizing an existing general purpose, multi-user/multitasking operating system to the requirements of real time. The foremost example of the high performance available by such an approach is Masscomp Inc's (Littleton, Mass) optimization of Unix.

Masscomp offers an extremely high performance, 68000 based, dual-processor system designed for use in high speed data acquisition applications. The Unix System III operating system has been performance tuned by Masscomp through some added functions and rewritten segments of code. Most modifications have been made in the I/O and task-scheduling areas of the operating system.

A set of priorities, higher than Unix's normal time sharing priorities, has been added to the processor's scheduling mechanism. These fixed priorities result in a predictable response from the operating system under interrupt conditions. As a result, processes can be guaranteed time to run by declaring themselves unswappable. Normal Unix reserves the right to reschedule any process it sees fit.

Masscomp also provides for contiguous disk file allocation under its Unix version. These files allow full disk speed and throughput to be maintained by minimizing the number of disk head seeks required during I/O operations. Also, this performance-tuned version of Unix features modifications in the context switching mechanism. A 2:1 performance improvement over conventional Unix has been realized through more efficient coding in this section of the operating software. Similar improvements in Unix pipe operations have been achieved by compact code.

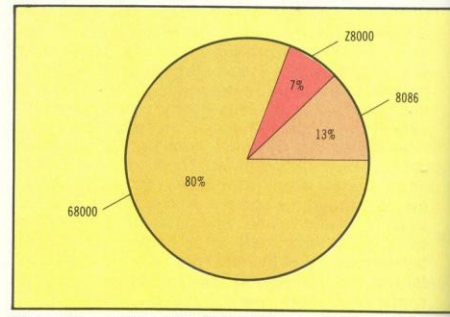


Fig 4 The distribution of microprocessors used in present Unix, or Unix-derived systems, reveals the momentum of the 68000 processor that is visible in software as well as hardware.

Finally, the use of asynchronous traps in the operating kernel has yielded significant performance improvements. Full, asynchronous I/O can now occur and, as a result, disk operations and data acquisition or program activity are not mutually exclusive. By supplying a signal to a running program that indicates a completed data acquisition task, program operation and data acquisition occur simultaneously. Data are buffered on the fly and do not need to interrupt processor operation.

Masscomp's customization of Unix provides a superset of user functions. Several new system services are available, and their presence does not detract from the normal functionality of Unix. Operating system response time in the 1- to 4-ms range is possible and, if microsecond response is required, a high speed, frontend I/O processor is available to meet the challenge. This direct memory access-like device will buffer high speed data or generate a host interrupt when further processing is possible.

Another performance-tuned version of Unix is available from Venturcom Inc (Cambridge, Mass). Venix-86 is derived from Unix and includes most of the functions of the mother operating system. A sped-up I/O processor has been added to facilitate the overlapping I/O transfers common in data acquisition settings. Also, Venix-86 provides for multiple accesses of common memory regions. Thus, a series of program routines can use common data almost simultaneously.

Binary semaphores are used to coordinate interprocessor communication and also to lock out certain processes from critical regions of memory or program code. A special, fast response priority

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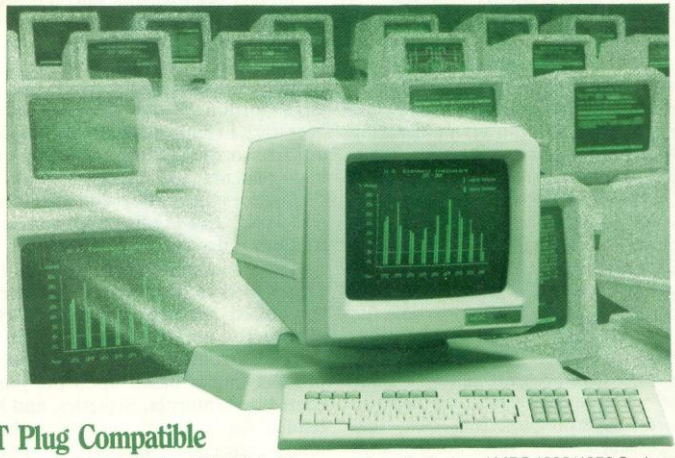

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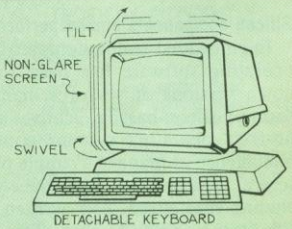

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level is supplied for processes that need instant access to the processor. The Venix-86 system supports several high level languages. Included are FORTRAN 77, C, Pascal, BASIC, and Rational FORTRAN. A full-screen editor, text editor, and graphics package are also included.

Alycon Corp's (San Diego, Calif) Regulus is another Unix-derived operating system specializing in realtime features. Regulus supports the entire Unix kernel and provides full multi-user/multitasking functions for Motorola's MC68000 processor. Standard Unix I/O subroutines, system calls, pipes, and filters are also supported.

Regulus has 32 user defined priority signals available to schedule processor response to realtime events. These priority signals can also be used for the supervision of intertask communication. Regulus provides for locking of part or whole file sections. Its file structure incorporates multikeyed, B-tree, and indexed sequential access method (ISAM) schemes. The ISAM feature allows any of four keys to serve as a data locater.

From the foregoing examples, it is clear that Unix-like systems can, and do, meet the demands of realtime operation. By optimizing I/O, modifying the Unix task scheduler, and improving various sections of code, the Unix operating system can be forged into a responsive software vehicle that will keep tabs on realtime events. An additional benefit of performance-tuned versions of Unix is the commonality that most versions maintain with stock Unix. For system designers, that spells convenience, software support, and functionality.

Silicon components embed performance

In embedded realtime applications, the trend in operating software has been to supply stripped down versions of resource managers, taking the form of silicon-based executives and kernels. These no-frills operating systems contain just enough intelligence to manage a simple process or monitor several data points. Often, the entire executive, including specialized, user written routines, can reside in a single ROM chip. This greatly simplifies design and improves reliability. The following examples of ROM-based executives, and the subtle differences between them, serve to illustrate the various approaches available to designers of realtime process control systems.

Intel's 80130 chip contains a collection of software components intended to function in conjunction with their iRMX-86 operating system. By using the 80130 chip as a source of lower level operating system instructions, designers can improve interrupt handling and realtime responsiveness. In addition, by combining the 80130 chip with recent Intel silicon software releases like the 82586 local area network coprocessor, improved realtime system performance is gained without sacrificing full functionality.

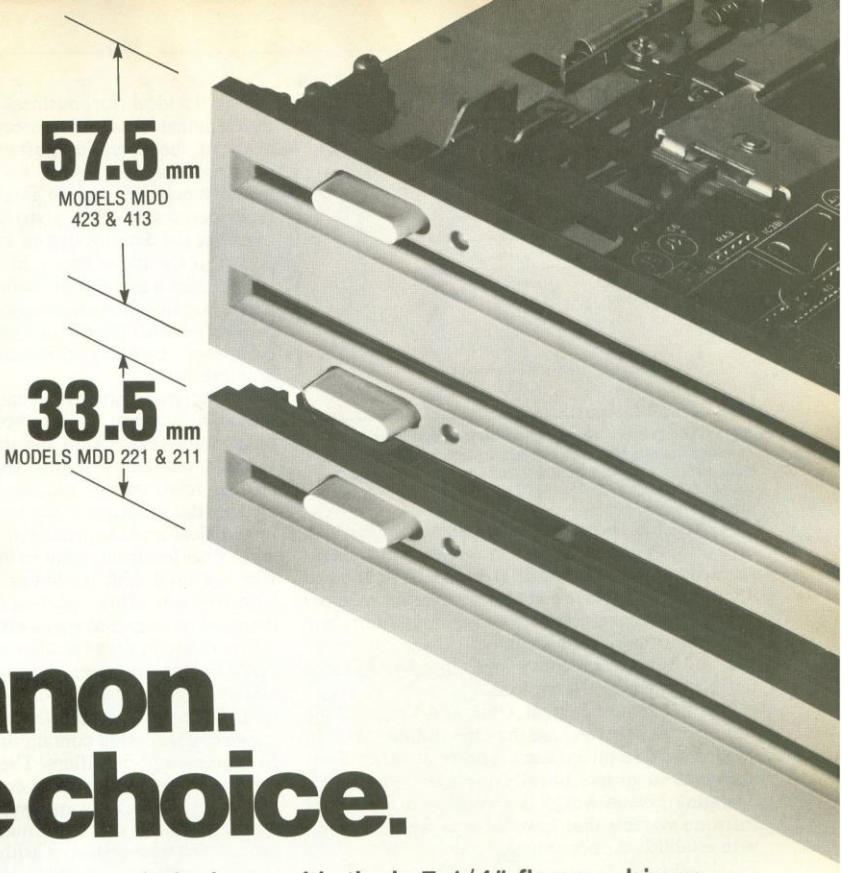
Another example of a silicon based executive approach to realtime operating systems is Hunter & Ready's (Palo Alto, Calif) well-known versatile realtime executive (VRTX). VRTX is a set of multitasking software components that can supply a large portion of the operating system primitives necessary in embedded control applications. Users are free to choose from a variety of control, task management, and communication routines and semaphores that provide an interface with the outside world. In addition, users can author their own routines if desired.

A set of internal pointers within the VRTX kernel allows users to direct operating system functions to specialized runtime routines. VRTX was recently chosen for use on VMEbus products by Mostek Corp (Carrollton, Tex). The VMEbus and board product line is based upon the joint design concocted by Motorola, Signetics, and Mostek and intended for international use in data, word, and image processing. Versions of VRTX are available for the 68000, 8086/8088, and iAPX 186 processors.

Hemenway Corp's (Cambridge, Mass) approach to the problem of realtime control is a hybrid one. Its well-known, silicon based MSP operating kernel is finding increasing application in laboratory, data acquisition, and industrial automation settings. By combining this popular realtime executive with a version of the Forth control language, a high performance, multitasking operating system results. (See "Adapting Forth to a Multi-User World," by Bruce Sweet, *Computer Design*, Apr 5, 1983, p 111.)

The MSP/Forth marriage allows users to take advantage of the comprehensive interrupt handling features of MSP while, at the same time, exploiting the strengths of Forth's threaded code and expandable vocabulary in control applications. Within the MSP system, a monitor is used to keep track of executing tasks. It also prohibits intertask interference and works in conjunction with a task queuing mechanism. The integrity of each task is thus ensured, while performance is optimized in multitasking settings.

JMI Software Consultants Inc (Roslyn, Pa) is another supplier of realtime software solutions. The company's recently released C executive is a case in point. This realtime monitor supports 8086/8088, 16032, and 68000 processors, and is suited for use with board-level products used in data acquisition or process control. This executive allows multiple C or Pascal tasks to run concurrently, and provides for the management of intertask communications. (See Fig 5.)



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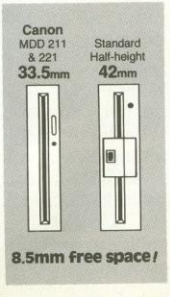

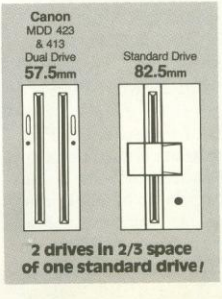

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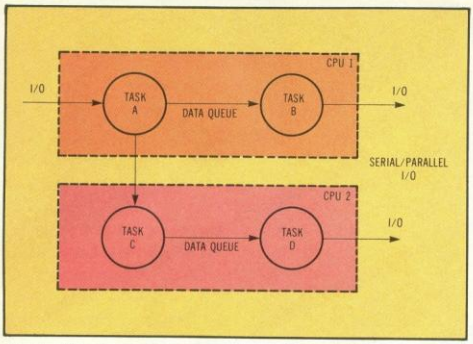

Fig 5 The C executive supports intertask and inter-CPU communication. Intertask communication uses byte-stream data queues; inter-CPU communications occur through I/O ports.

A realtime, preemptive scheduler, sensitive to task priority and other system events, is also incorporated into this C language executive. A ROM based library of 50 software routines covering memory management, character string manipulations, and I/O operations is also supplied. Users can easily link and run the executive and library routines in flexible system configurations.

Lest it be thought that Unix and CP/M, along with their derivatives, are the only options open to designers of 16-bit systems, a look at other alternatives is in order. Luckily for users, the 16-bit operating system world is served by a variety of software systems that have little or nothing to do with established operating systems.

Pick, an operating system

The Pick operating system is a Unix competitor with a long and varied history. Originally developed by Richard Pick in 1972 for use on 16-bit minicomputers, today's Pick system may represent operating software whose time has come. At present, the Pick operating system suffers from limited visibility. It is used primarily on hardware destined for use in business settings. Systems running Pick operating software include those of Altos Computers (San Jose, Calif), Datamedia Corp (Pennsauken, NJ), IBM Corp (Armonk, NY), Honeywell Corp (Minneapolis, Minn), and Hewlett-Packard Co (Palo Alto, Calif).

By most conventional units of measure, the Pick system is much easier to use than either Unix or Xenix, but lacks the rich and varied software development support. However, its lack of tools and utilities serving this function has not been a hindrance to its primarily business oriented users. In fact, the simplicity of the Pick system, stemming from its streamlined nature, is one of the reasons for its popularity.

Pick is ideal for business related application development. And, it is no coincidence that at the heart of the operating software lies an effective database manager. Also featured are a virtual memory manager and an English language query/report generator. Pick's virtual memory manager manages the data located in main memory storage and also on disk. Pages of 512 bytes each are swapped into and out of main memory as needed. Thus, applications developers need not concern themselves with the constraints imposed by microcomputer memory limitations when writing applications.

A relational database manager is also provided and allows several users to access a common data base. Data files within the data base are related through dictionary terms. Users may specify or change relationships quickly and easily without altering the structure of the central data base. Four hierarchical levels are available to dictionary entries and higher levels can point to lower. Variable length files are used with maximum file size set at 32K bytes/record. This space-saving file format is designed to extract as much efficiency from limited microcomputer disk facilities as possible.

An English language-like query/report generator allows selective or conditional retrieval of information. Inquiries can take the form of English language sentences that contain the appropriate verbs, file names, and modifiers. The vocabulary used to compose these sentences is contained in a system dictionary that is always available to users. The report generator can be formatted by the user and generalized with logical or arithmetic relationships. Output sorting is possible, even down to a subvalue level within multiple unit records.

Both the commonsense English language command structure and the inclusion of the BASIC language as the core programming dialect have contributed to the Pick System's popularity with users. Hindering the operating system's general acceptance, however, is a woeful lack of high level language support. With the exception of Pick BASIC, no high level languages are available. As a result, the attractiveness of the operating system is limited to users and application authors content to work in BASIC. Granted, there are thousands of these people in the microcomputer arena. Unfortunately, this situation places the Pick operating system out of the running in most non-business settings.

Another hindrance to the universality of Pick is its lack of communications function support. In the distributed world of office computing, the ability to link diverse desktop computers together, as well as to a central data base, is crucial. An operating system that inhibits this interconnection must be viewed with some skepticism.

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CIRCLE 66

Changes are in the offing for the Pick operating system, however. Recently Richard Pick announced Release 84 of the Pick system. This update is, in Pick's words, "a major rewrite and enhancement that will provide an optimized application generation tool." If nothing else, this update is likely to embody the solid, predictable performance that characterizes earlier versions of the operating system. A few more bells and whistles will be supplied to users, and expanded database functions are planned. Unfortunately, the issue of poor to nonexistent high level language support goes unaddressed.

With approximately 10,000 installed bases at present, Pick operating software should be as visible as other major multi-user operating systems. Such is not the case. One factor promoting its proliferation, though, is its well-established, debugged, and reliable base of business software. Unix-based business applications have not exactly inundated the market, and Pick's strength in this important segment of the 16-bit software scene gives it a leg up on the competition. Also, the ever present rumors that Pick is about to ink a pact with Tandy/Radio Shack (Fort Worth, Tex), IBM, or Apple keep it poised on the verge of prominence.

In the 16-bit, multi-user microcomputer arena, there is certainly a place for a user friendly operating system. If that operating system also provides effective database management and serves as a powerful application development tool, so much the better. The Pick system seems to satisfy most of the criteria for operating system success. And, as business applications multiply, a simple, effective operating system that fosters development and database management at the user level will be increasingly in demand. The Pick system may indeed be software whose time has come.

An operating system, Oasis

Phase One Systems is no recent arrival on the 16-bit operating system scene. In fact, its Oasis operating software has been seen around business settings since 1977. Recent versions of the operating system designed for modern 16-bit hardware include Multi-User Oasis (Tandy) and Oasis-16 (IBM Personal Computer).

The IBM Personal Computer version supports several advanced features that are essential in business computing environments. Three users can share a single machine equipped with hard disk; the operating system supports automatic record locking and optional file locking. As a result, the integrity of files is retained during multiple accesses. In addition, access to an entire file can be locked at the user level to prevent unauthorized data alteration.

Other data protection features include optional passwords and privilege levels. Thus, the status of user accounts can be set with access controls. The system also maintains records of user accounts and program execution histories to aid in system record keeping in commercial, timesharing installations.

One of the most desirable features of the Oasis system, from a business user's point of view, is its support of true ISAM files. Here, data files result in the creation of auxiliary files providing keys that can be quickly searched by the operating system. Thus, speedy random access to all data is possible. In addition to ISAM files, Oasis also supports direct and sequential file structures.

The high level language support offered by the Oasis operating system includes RM/Cobol, C, and interpreted or compiled BASIC or macro assembler. BASIC programmers have several advanced functions available to them. These include SELECT-CASE-CSEND, WHILE-WEND, and IF-IFEND statements. Also, the BASIC supplied provides multiline functions, calling of assembly language subroutines, and chaining of commands.

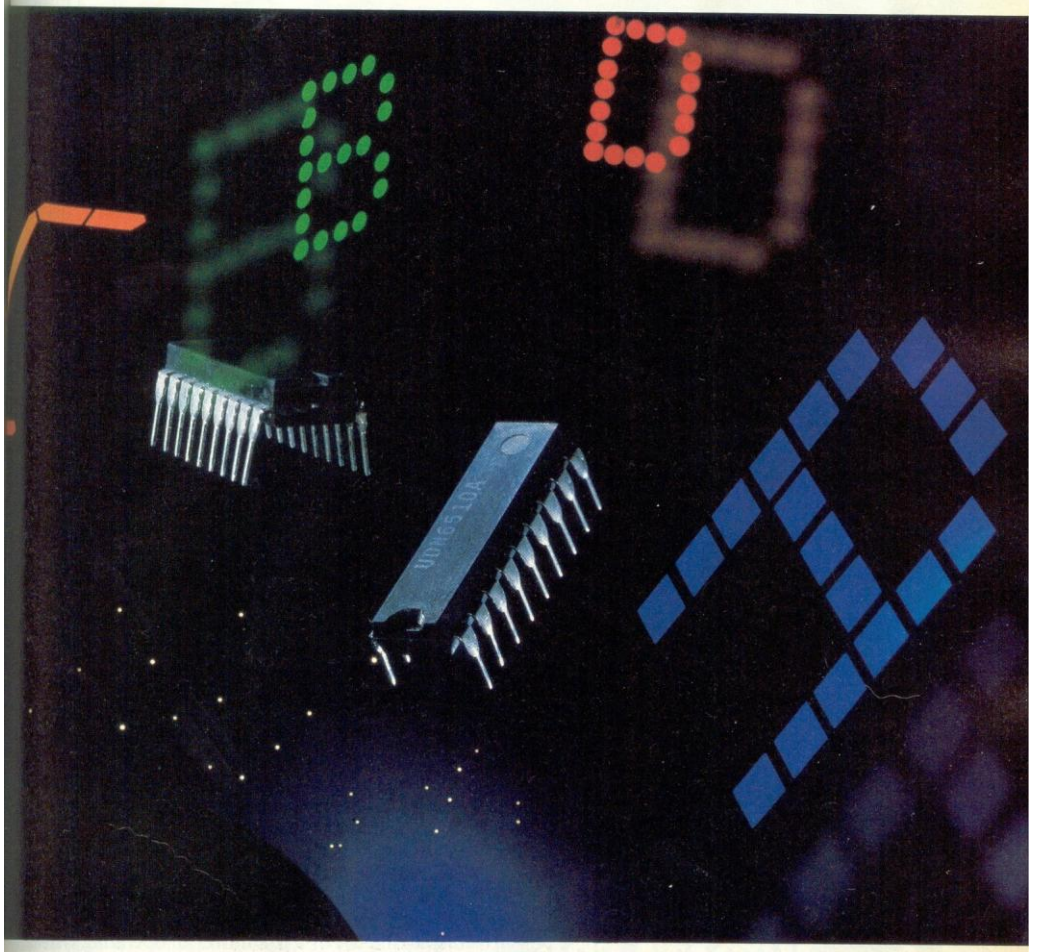
In the spirit of user friendliness, Oasis supplies a job control language (JCL) that allows users to be isolated from the system command shell. Users not adverse to hacking it up, however, can take full advantage of the relocatable macro assembler, the debugger, and the linker/editor. Diagnostic utilities, communication drivers, and electronic mail facilities are also supplied.

Central to any business application is a data base. Oasis operating system offers such a feature in the form of its Control database system. Control is a relational data base featuring an interactive screen generator. Users may design screens, provide prompts, and prohibit the entry of incorrect information with the Control screen editor. A HELP function is also available. An English-like query language allows users to generate reports from data bases by using simple, easily understood commands. In addition, a file sort utility that runs in conjunction with the Control data base provides fast, record level sorting.

Big system compatibility is available, to an extent, with the Oasis operating system. A bisynchronous communication package allows communications to take place between Oasis systems and 2780/3780 mainframes. A disk formatting utility provides IBM 3740 data file compatibility as well.

With its focus on the multi-user business market, the Oasis operating system is well-targeted for success. Its support of friendly, as well as advanced, features makes it attractive to users and programmers alike. Finally, its availability on a wide range of hardware, particularly the IBM Personal Computer, may result in the increased application support necessary for it to become a mainstream, 16-bit operating system. Hardware support, application availability, and time will eventually tell.

VISION.



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CIRCLE 67

A Unix imitator gaining increasing attention is Coherent, from Mark Williams software. A 16-bit Unix-like system available for use on several popular microprocessors, it supports Intel's 8086/8088, Motorola's 68000, and Zilog's Z8002. In addition, versions of Coherent are supplied for use on Digital Equipment's PDP-11 family of small computers.

Coherent qualities in operating software

Written in C language, Coherent features many general purpose software development tools designed to ease program creation and management. It is also compatible with Unix at both the source code (C) and user command (shell) levels. Coherent features full multi-user/multitasking, as well as the ability to run both foreground and background tasks for a single user. A tree-structured, hierarchical file system, in which I/O piping and memory sharing are possible, is used. Realtime performance is made possible by process locking in memory, and minimal interrupt lockout times. Coherent is also able to gracefully recover from power failures without destroying files.

Coherent provides high level language support for C, International Standard's Organization Pascal, and a compiled version of BASIC called XYBASIC. This version of the popular BASIC language displays interactive, interpreter-like features to ease program debugging. Mark Williams claims that by using a generalized code generator, the Coherent operating system also enhances the portability of applications running under it and speeds their development. The entire operating system, including all of the language processors, can be transported to a new machine with ease.

It is obvious that operating system alternatives abound for the users of 16-bit microcomputers. Deciding which system to use is often based equally upon instinct and information. Paramount in any choice, however, is application software. Choosing a mainstream operating system like CP/M or MS-DOS 2.0 ensures that lots of applications will be instantly available. However, having a specific application in mind, such as business calculations, realtime control, or networked processing, may dictate the use of a less universal operating system.

In general though, choosing an operating system is similar to selecting hardware. In an effort to answer the question, "What can it do?" users increasingly look to available applications for clues to the most functional operating-level software.

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CIRCLE 70

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CIRCLE 71


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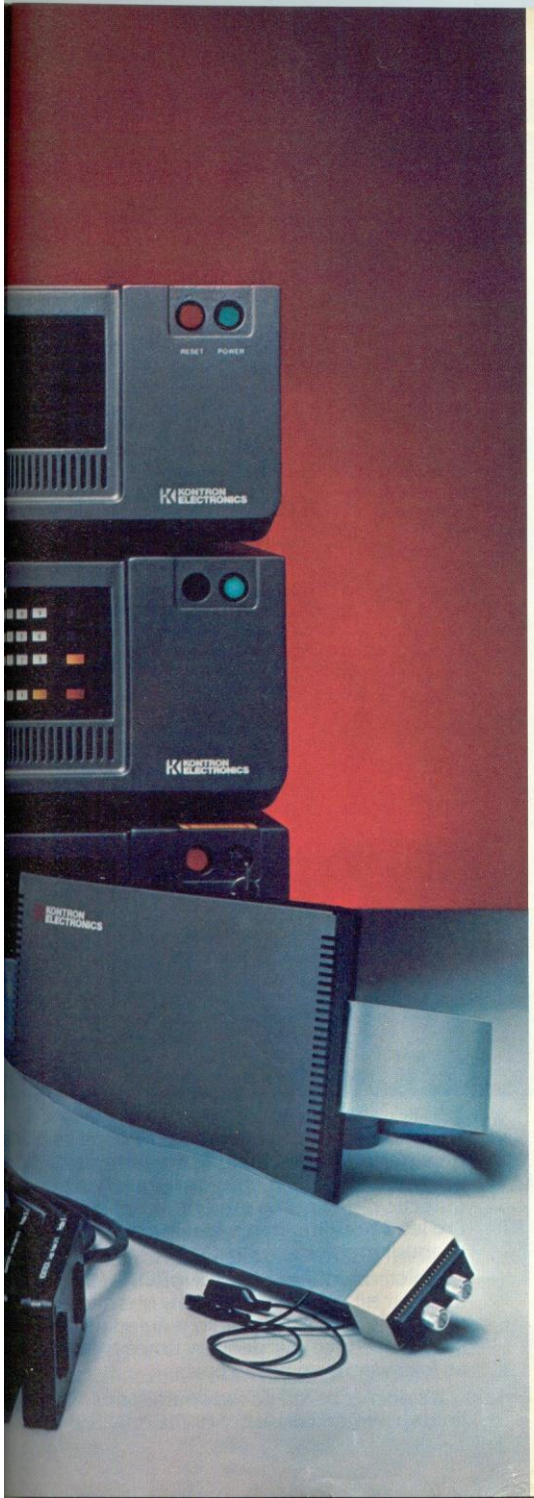

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THE C LANGUAGE: KEY TO PORTABILITY

A machine-independent compiler and system function library, rather than a universal operating system, are the keys to software portability.

by Edward M. Rifkin and Steve Williams

Powerful 16-bit microcomputer based systems now offer the same computer power as minicomputers. Thus, protecting software investments while taking advantage of new hardware is the biggest issue facing system integrators. A means is needed, therefore, to easily transport the large base of existing software from processor to processor, and from one operating system environment to another.

Much opinion favors the Unix operating system and the C language in which the majority of Unix based applications are written, for obtaining portability. However, even though Unix is written in C, the authors themselves point out that C is not tied to any one operating system. Digital Research believes that the C language, not Unix, is the key to software portability.

Edward M. Rifkin is a product marketing manager for Digital Research Inc, PO Box 579, Pacific Grove, CA 93950, where he is responsible for the C and Pascal/MT+ families of languages. Mr Rifkin holds a BSCSE and an MSCSE from Northwestern University, as well as an MBA from the Wharton School of Business.

Steve Williams is operating systems engineering manager for Digital Research Inc. He is responsible for new product development. Mr Williams holds a BSEE and an MSCS from the University of Tennessee.

C is powerful, concise, and most important, a machine-independent language. For this reason, the company has chosen C as its system implementation language instead of PL/M and assembly language. Further, while C is a powerful system programming language, it is also useful for developing commercial, industrial, and scientific applications. In fact, hundreds of such C programs already exist.

To gain access to the majority of this software, one simply needs a well-implemented C compiler. A program written in C, to run under Unix, can then be recompiled and executed under another operating system such as CP/M-86®. Thus, the language, not the operating system, makes portability possible.

The C language

C embodies versatility and speed, and makes few assumptions about the processor. Fundamental data objects are characters, integers, and floating point numbers. Complex data types can be constructed from these fundamental types using pointers, arrays, structures (records), unions, and functions.

Structured programming is supported with decision-making control statements (if-else), looping controls (while, for, do), and with case selection (switch). Compared with other structured programming languages (eg, Ada, Pascal, or PL/I), C is very concise. Commands are simple and terse, and functions can be called recursively. A simple

```
for (i=1, j=3, k=i+j; i<10; i++)
  a[i] = i>2 ? k+1: k-1;
```

(a)

```
j:=3;
k:=i+j;
for i:=1 to 9 do
  if (i>2) then
    a[i]:=k+1
  else
    a[i]:=k-1;
```

(b)

Fig 1 Comparison of routines written in C (a) and in Pascal (b) reveals that C's code retains its structure, but is much more compact than Pascal.

statement in C can perform an operation that would require several lines of code in other languages (Fig 1).

Most important, C neither provides built-in input/output (I/O) facilities, nor high level operations on character strings, sets, lists, or files. These operations require a corresponding set of functions in a runtime routine library; these routines are accessed through standard system calls. To a programmer accustomed to more richly defined languages, this may appear to be a drawback. But by keeping C simple, it can be implemented in a small memory and can be learned quickly. Moreover, programs are close to assembly language in efficiency.

Functions supported by the runtime library can be as many or as few as necessary for the application needs. For many programs, the runtime library functions used are minimal. Thus, total program space is quite small. As many high level functions can be created as desired, however. Experienced programmers have found that C is almost as efficient as assembly language, with normal functions as little as 20% larger. In fact, system function routines are often written in C. The language's small size and complete machine independence make it relatively simple to port from one processor to another. This characteristic, combined with the language's power, makes it ideal for promoting program portability.

Because of these features, C—not Unix or any one operating system—is the answer to program portability. The option to use both Unix and C does make sense in cases where large multiuser/multiprogramming systems are envisioned. In other cases, where a minimum of hardware is used to provide high performance for single users or a small number of users, alternatives such as CP/M-86, Concurrent CP/M-86™, or CP/M-68K™ can provide equal program portability and performance. Digital Research has itself benefited from the use of C since the CP/M-68K operating system was written in C and was ported to a Z8000 based system in six weeks. (See the Panel, "The CP/M-68K Operating System.")

Choosing a compiler

For the system integrator and program developer, several concerns should be addressed in selecting a compiler to implement the C language. First, the language must be fully compatible with the acknowledged standard, as defined by AT&T. Second, similar to the Unix version, the runtime library must provide functions for effective file manipulation,

The CP/M-68K operating system

Most 68000 based systems, designed to provide low cost computing power, require file management and a user interface. A standard operating system can provide these functions, among others, and can be a valuable base for transporting applications software. Until recently, however, the choices were limited to nonstandard proprietary operating systems and Unix from AT&T.

Unix, of course, is widely supported in the scientific and academic environments and is also being widely promoted as a commercial solution. However, for single-user, low cost applications where Unix is not economically viable, CP/M-68K is now available. CP/M-68K can provide a standard operating environment for many single-user applications written in C, BASIC, Pascal, and Cobol. Since it can operate on minimum systems with only 64K bytes of random access memory and a single floppy disk, it fills a gap between the larger multi-user Unix systems, which require hard disk storage, and the low end 8-bit microcomputer systems.

Written in C, CP/M-68K is fully CP/M® and CP/M-86 compatible. It has also been ported onto a Z8000 based 16-bit system. Configurations can be from 64K bytes to the full 16M bytes of main memory supported by the 68000, 68010, and 68020 processors. Moreover, from 1 to 16 disk drives can be supported, each with up to 512M bytes.

Upgrading existing programs written under CP/M is straightforward. While assembly language programs do require recoding, high level language programs should recompile with little or no modification. In addition, the C compiler included with CP/M-68K supports a subset of the Unix Version 7 runtime library routines. Thus, programs written in C under Unix can be easily transported to the CP/M environment.

Like previous CP/M versions, CP/M-68K is organized into the console command processor, the basic disk operating system, and the basic input/output system. The operating system can reside anywhere in memory except in the 68000 processor's interrupt vector area (0 Hex to 3FF Hex). Typically, it is placed at the top of memory; the transient program area (TPA) runs from 400 Hex to the base of the operating system. The only memory restriction is that the TPA must be in one contiguous memory block.

Resident System Extensions are supported and allow users to customize and extend the operating system functions. All standard CP/M utilities are provided as well. And, finally, the end user will notice no significant difference between CP/M-68K and other versions of CP/M.

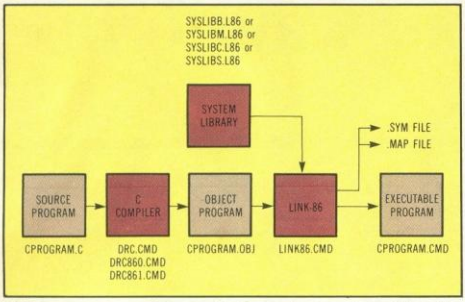

Fig 2 C program source code is compiled and an object file is created. Function calls to various runtime library system routines are made within the program. The linker combines the program's object code and the library's called routines to create an executable copy of the final program.

memory management, and other functions. Third, the implementation chosen should also provide program development support features to aid developing and debugging complex code. Fourth, the implementation should include features to help take advantage of specific processor architecture where possible. And fifth, the language should interface smoothly with program development tools (eg, screen builders and file access managers).

Since the overwhelming majority of application programs written in C have been developed using the language as defined by Kernighan and Ritchie, and as supported in the Unix Version 7 environment, the company's C compiler was designed to provide full compatibility with the Unix Version 7 language standard. To ensure portability, the compiler's compatibility with Unix Version 7 must include all type specifiers, storage class specifiers, operators, statements, and preprocessor commands. C can then provide very distinct advantages.

Type specifiers—short, long, and unsigned—are adjectives that can be used in combination with numeric specifiers like int (integer) and float (floating point numbers). A union is a variable that can sequentially contain objects of different types and sizes. It is useful in creating data tables that may be called upon to contain different types of data, but must be retained in memory as a fixed-sized table. A struct (structure) is a collection of variables grouped under a single name—called a "record" in other languages.

Storage class specifiers cause variable-sized memory spaces to be reserved. The register declaration is unique because it denotes a variable that will be heavily used. The compiler will store such variables in a processor register where possible. This leads to small, fast programs.

Operators include the standard variety of logical additive, multiplicative, shift, and relational operations. Additional bit-wise operations permit shifting, ANDing, ORing, and complementing operations to be performed on nonfloating point variables on a bit-by-bit basis. This is very useful in hardware-intensive applications requiring close control of hardware signals.

Statements include the program flow control constructions previously mentioned (if, while, for, etc), and permit declarations and statements to be grouped into functional blocks of program code. And, finally, the C compiler includes a preprocessor that lets the programmer use macro substitutions (#define), and allows conditional compilation (#if, #ifdef, etc) and file inclusion (#include).

For maximum portability, the language implementation selected by the system integrator should include all of these Kernighan and Ritchie defined commands and features. Fig 2 shows how a C program is created. First, the compiler generates an object file from the source code. Then this is linked to any called runtime routines from the system library and forms an executable program file.

Extensive runtime library support

It is equally important that the system runtime library routines be compatible, as they contain the I/O routines, memory allocation commands, and file access operations. Since the vast majority of C programs have been written in the Unix environment, the runtime library must be accessed like the Unix standard. Digital Research C™ does conform to the Unix Version 7 runtime library conventions by supporting the functions shown in the Table, "Unix Compatible System Library Functions." By adhering to function-calling sequences and parameter-passing structures, the Digital Research C is compatible with almost all Unix based C programs. About 85% of the standard Unix library of functions are included with Digital Research C, except functions that relate to multitasking, pipes, and other special facilities of the Unix operating system. Typically, an application program written in C under Unix can be recompiled using Digital Research C and executed under CP/M-86, with little or no program modification.

Important concerns to the active program developer should be the availability of sophisticated error warning and reporting facilities, and the ability to get directly to useful compiler-generated listings. The company's C has error checking features similar to LINT, the Unix diagnostic program. It applies a strict check to the program at compile time. If it detects problems such as type mismatches, inconsistent arguments, and mishandled variables, it will print error messages.

There are two types of error messages: reports and warnings. Error reports indicate mistakes in the source code, such as syntax errors and

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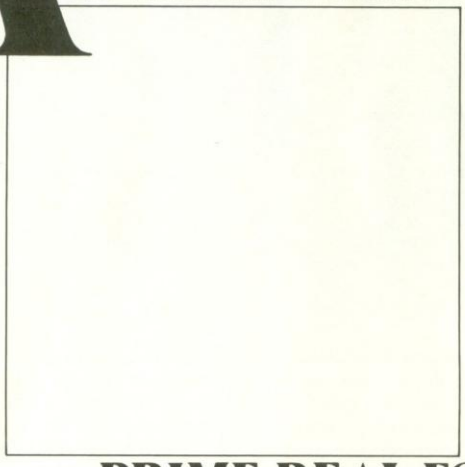

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CIRCLE 77

Unix Compatible System Library Functions

Stream file access functions		
clearerr	fputc	gets
fclose	fputs	getw
fdopen	fread	printf
feof	freopen	putc
ferror	fscanf	putchar
fflush	fseek	putl
fgetc	ftell	puts
fgets	fwrite	putw
fileno	getc	rewind
fopen	getchar	scanf
fprintf	getl	ungetc

String functions		
atoi	sprintf	strlen
atol	sscanf	strncat
index	strcat	strncmp
mktemp	strcmp	strncpy
rindex	strcpy	

ASCII character macros		
isalnum	islower	isupper
isalpha	isprint	toascii
isascii	ispunct	tolower
iscntrl	isspace	toupper
isdigit		

Block file access functions		
close	seek	read
creat	open	tell
creata	opena	unlink
creatb	openb	write

Memory management functions		
brk	free	realloc
calloc	maloc	sbrk

Double-precision floating point functions		
atan	fabs	sin
atof	log	sqrt
cos	log10	tan
exp		

Utility functions		
abs	_exit	qsort
access	getpass	rand
=BDOS	getpid	setjmp
chmod	isatty	srand
chown	longjmp	swab
exit	perror	ttyname

improper data type specifications. Error warnings include messages such as "operand types do not match" or "right brace expected." Some error warnings indicate that an error can occur if corrective action is not taken. For example, error message #83 "indirection on nonpointers is dangerous," suggests caution if using the indirection operators with integers, since this feature may not be portable to other processor implementations. Other error warnings simply indicate that an action has been taken, such as #95, "subscript being truncated to integer."

Programs that pass the error reporting facility have a good chance of running properly. However, for those programs that still do not execute as expected, the C compiler has provided access to the disassembled object code generated by the compiler. In addition, the macros expanded by the preprocessor can be examined with a reverse preprocessor program. This is useful when attempting to understand a problem related to the macro section of a program.

Powerful program environment

C supports a wide range of command line options that add flexibility and power to compilation. The switches are set by a dash, followed by a tag character that sends special instructions to the compiler output. These give the programmer flexibility in tailoring the compiler. The programmer can link in all or selected runtime library routines and enable/disable compiler options such as a code optimizer or a short/long jump optimizer; specify target hardware memory options; and set error message display levels.

When used with the 8086 or 8088 microprocessor, the compiler offers four memory configuration options. This is useful when programming various-sized 8086/8088 systems. The 8086/8088 has four segment registers that point to the base of program storage (code segment register), data area (data segment register), stack memory (stack segment register), and an extra memory area most often used as a second data area (extra segment register). As C programs can have various amounts of code, data, and stack space, the memory model selection determines the size of the different areas and the initial values of the segment registers. The C compiler supports four different memory models (small, compact, medium, and big) to provide a range of program configurations that take full advantage of the 8086/8088 architecture (Fig 3).

Another command switch option enables the use of an 8087 coprocessor chip (if present in the system) to perform floating point arithmetic operations. This is much faster than using the IEEE floating point routines in the runtime library. While these features can help tailor programs to specific hardware environments, they do not affect the language's compatibility or portability.

Program development is facilitated by options that display markers when a significant event takes place during compile time. Options include displaying a # character as the compiler processes each

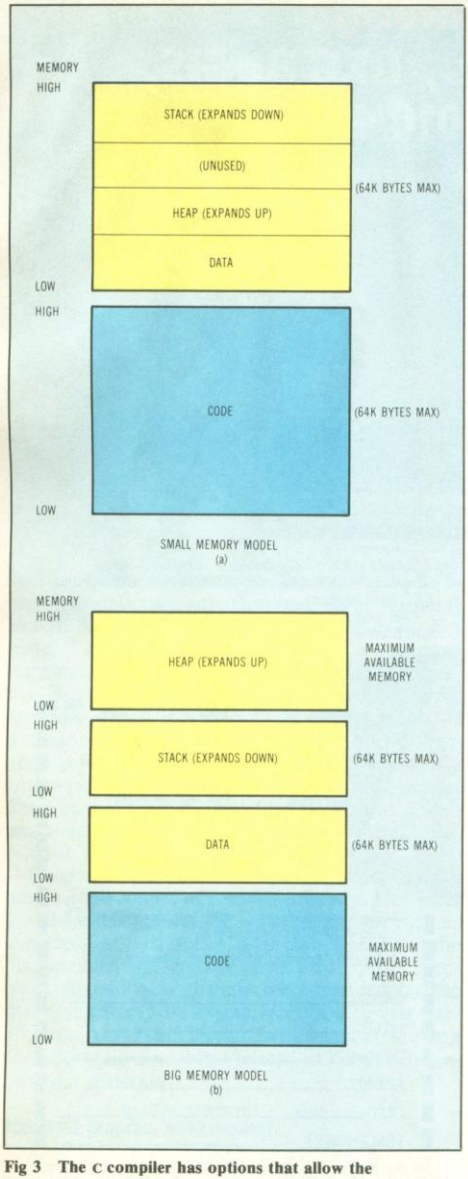

Fig 3 The C compiler has options that allow the programmer to define four memory configurations in which 8086 based programs will run. The small memory model (a) supports a separate code space and a data/stack/heap space, each of which may not exceed 64K bytes. The big memory model (b) allows the data and stack segments to be as large as 64K bytes, and code and heap areas to be as large as available memory.

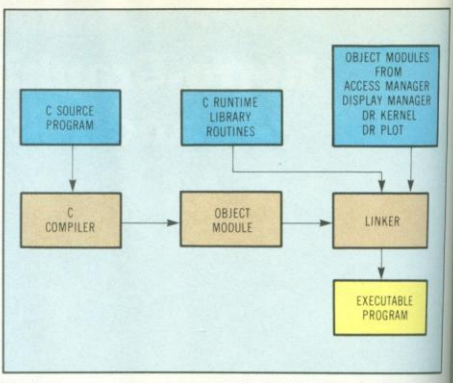

Fig 4 C programs can be compiled with object code created by other programs. Code generated by tools such as Access Manager, Display Manager, DR-Kernel, and DR-Plot can be linked into a C applications program, compiled with Digital Research C.

function, displaying the name of each function processed, displaying start/end messages, and displaying file name and line number as the compiler processes each line. For program debug, the interlist option creates a listing that shows the C source lines, the object code output, and a disassembled listing showing assembly language instructions. This greatly aids in debugging and critical code optimization.

This C compiler is fully compatible with the company's application program development tools, such as Display Manager™ for creating and manipulating video display screens, and Access Manager™ for file management. In addition, Digital Research supports graphics oriented programming with DR Kernel™ and DR Plot™ subroutine libraries that supply 2-dimensional graphic primitives and high level graphics functions. These routines can also be used by application programs written with the C compiler. This is accomplished by a common system call and a parameter passing interface that allow the C programs to easily call other programming tools (Fig 4).

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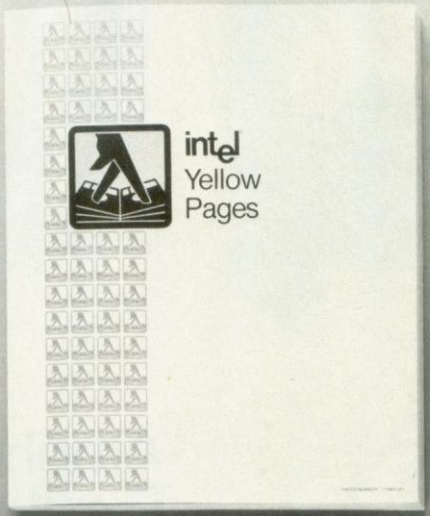

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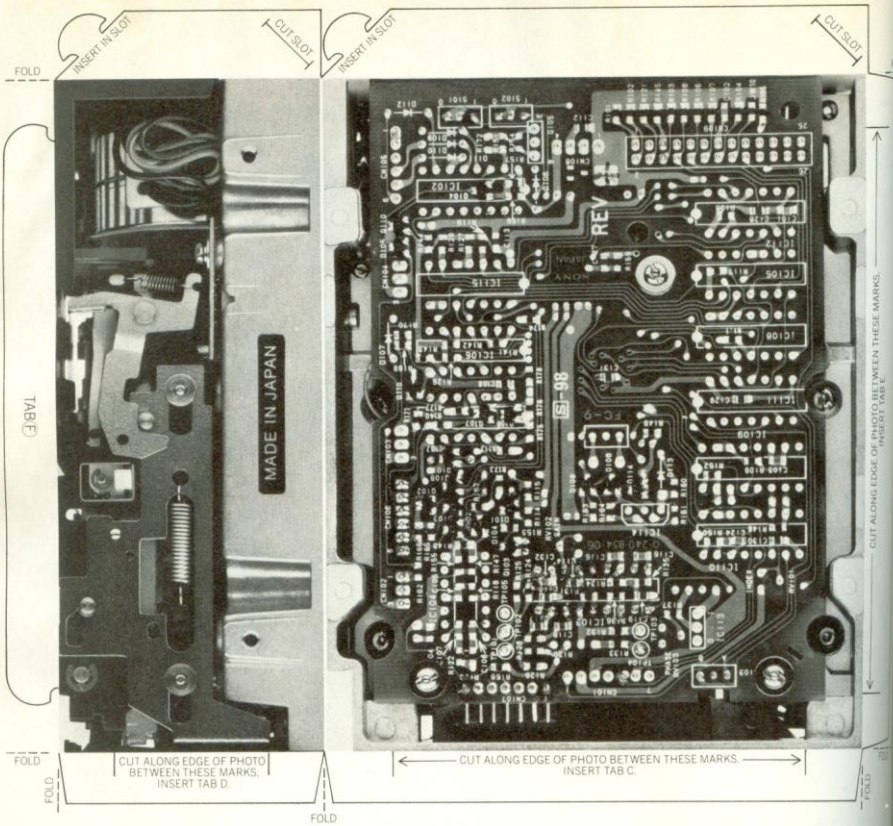

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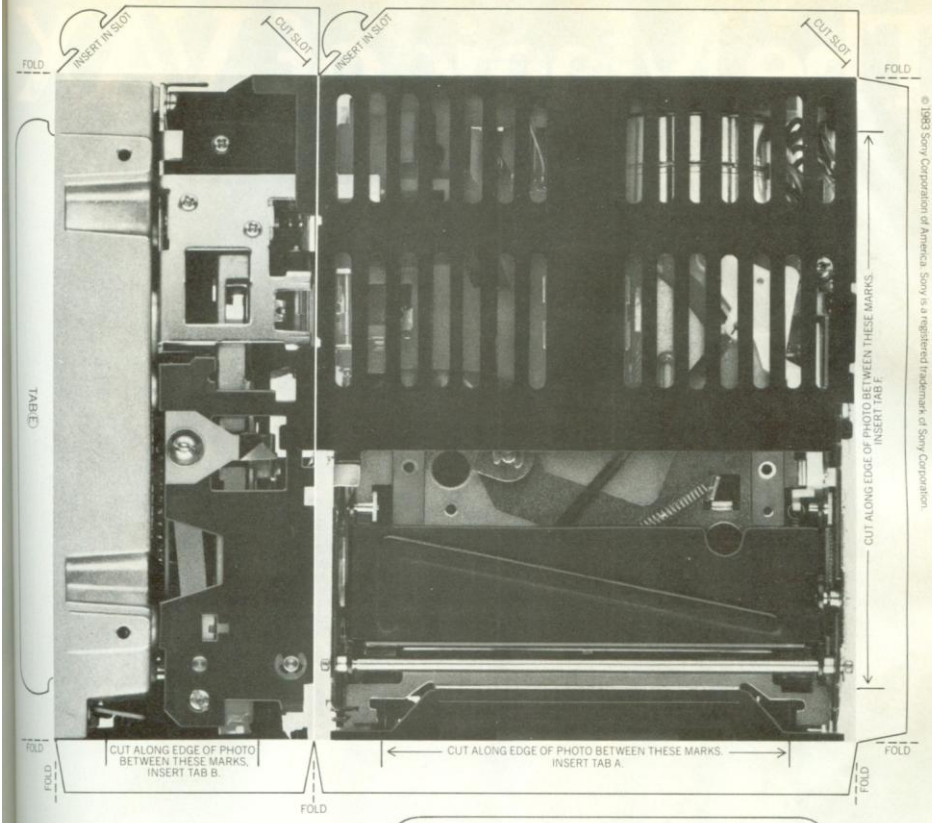

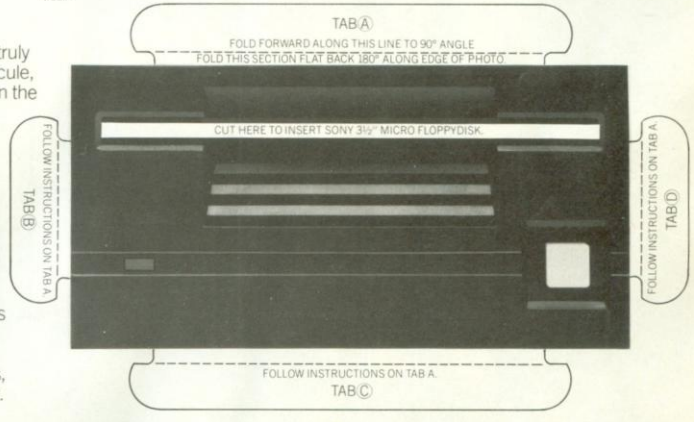

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LISA'S ALTERNATIVE OPERATING SYSTEM

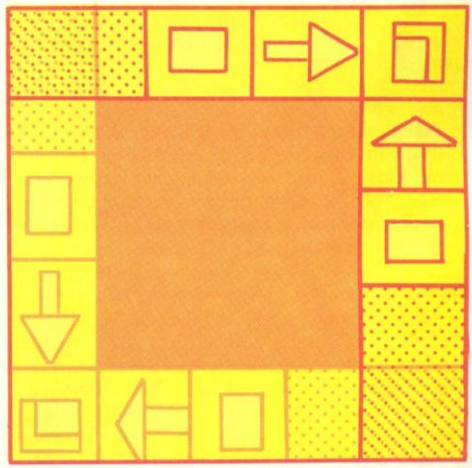
The rigid command language syntax and mode based structures of conventional operating systems may be a thing of the past.

by Bruce Daniels

Lisa, an advanced personal computer system, radically changes the way people interact with a computer. In traditional microcomputer operating systems, interaction occurs strictly via a special command language. With Lisa, however, the use of a very intuitive and consistent electronic desktop model allows interaction through pointing and graphics.

Although traditional operating systems provide a raw capability for general purpose computing, they are excessively complex, arcane, and difficult to use. Thus, they do not meet the needs of nonexpert computer users. Nor do these systems provide all the required functionality since they do not support rapid switching between simultaneous activities. In addition, the convenient examination and transfer of data between these interdependent activities are not supported. Furthermore, existing systems cannot be easily modified.

The Apple's Local Integrated Software Architecture (Lisa) takes a revolutionary approach to operating system software, resulting in an integrated system that is an order of magnitude easier to use. This new approach, not constrained by the traditional structures of existing operating systems, is concerned almost exclusively with providing features that make the computer easier or more convenient for the nonexpert user. With today's technology, the difficulty of providing such a feature is minimal.



Five concepts are implicit in Lisa's operating system. First, Lisa is a personal computer. As

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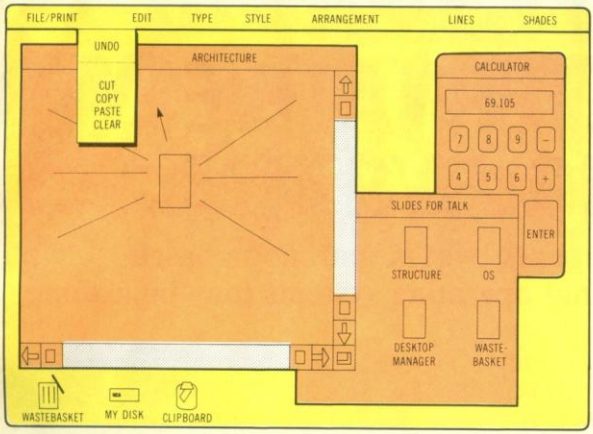

Fig 1 The Lisa user interface takes the form of a littered desktop. Windows on various foreground and background tasks can be manipulated at will, and icons pointed to for the initiation of system functions. This visual/symbolic implementation avoids the constraints associated with command languages and mode based operations.

demonstrated by the microcomputer revolution, it is economically and technically sound to dedicate a single computer to a single person, rather than forcing many users to share part of a remote computer. Second, Lisa is intuitive; it works the way people do. Third, Lisa is consistent; commands are invoked the same way throughout the system and, where it makes sense, commands apply uniformly throughout the system. Fourth, Lisa is comprehensive; simultaneous multiple activities can be performed with easy transfer of information between them. Finally, Lisa is communicative; working together with other computers, it can access and share the information and resources of local Lisas, or of remote computers.

What is the Lisa?

Lisa represents over 200 person years and $50 million of development effort. Its intellectual inspiration came from the Smalltalk language and operating system developed at the Xerox Palo Alto Research Center. This system's pioneering use of graphics and a mouse to present the fundamental concepts of overlapping pieces of paper on an electronic desktop marked a departure in computer operating software. Taking the Smalltalk concepts, Apple spent three years refining them, adding innovations, and reducing costs.

Hardware is based on the MC68000 microprocessor. This chip's large, uniform address space, 32-bit wide internal data paths, and powerful regular instruction set give it a clear advantage over many of today's microprocessors. Since Lisa was intended to be the first member of a powerful, long-lived family of computer systems, this microprocessor's capability to gracefully evolve into faster and more powerful versions through the 1980s was also important.

As standard equipment, Lisa has a 1M-byte main memory—fully parity checked to ensure reliable operation. Designed to support up to 2M-byte main memory, this system also has special memory management hardware to support multiprocessing. Lisa uses a 5M-byte Winchester disk and two built-in floppy disk drives. These floppies, storing over 860K bytes of information, are specially designed and developed to provide large capacity, reliability, and foolproof operation. An IBM-like layout and numeric keypad are included on Lisa's detachable keyboard.

The most interesting feature of the hardware is the mouse—a comfortable, convenient pointing device. Lisa's mouse contains a single button in order to eliminate user confusion. Also included is a built-in 12″ black and white bit-mapped display. This high resolution device allows users to simultaneously display graphics symbols, multiple fonts, and type styles on the screen.

The user interface is modeled around a desktop (see Fig 1) and contains graphical images of familiar office objects such as documents, folders, and stationery. Users control the machine by pointing at these images with the mouse. Graphics and multiple type styles, up to one-third of an inch tall, appear on the screen. These are reproduced with unparalleled quality on the printed page. A companion dot matrix printer produces high resolution text and graphics.

Standard with the Lisa system are six integrated, consistent software applications: a word processor; an electronic spreadsheet; a program that turns numbers into meaningful business charts and graphs; a graphics editor to create diagrams, drawings, and illustrations; a project scheduling program; and a database program. Also available is a seventh application—an asynchronous communication package emulating TTY, VT52, and VT100 terminals. IBM hosts can be accessed through a 3270 communications package and 3270 cluster controller.

Existing solutions are inadequate

Although a wide variety of microcomputers are currently available, many do not satisfy the needs of the typical information user. A major deficiency in current microcomputers is the lack of suitable software.

Software consists of the operating system and applications that it supports. Currently, such popular microcomputer operating systems as CP/M, MS-DOS, Apple DOS, UCSD p-System, and Unix are fundamentally alike. Certainly, they differ in the way to use the system, but the basic manner in which users interact with the system is qualitatively similar. In reality, the computer industry is developing the same operating system over and over.

Thus, it is not surprising that traditional operating systems do not meet the needs of modern users since computer experts (ie, programmers) designed them all for other computer experts' use. Such expert users are comfortable with the artificial concepts and terms upon which these operating systems are built. They know, for instance, what a program is and what it means to execute such a program. They understand the concept of a file, a directory or catalog, and a disk volume. Most important, such experts are obviously accustomed and willing to spend many hours studying the cryptic manuals required to master such a technical subject. Soon, people like this will represent a minority of microcomputer users. The Lisa user interface offers a welcome alternative.

The Lisa user interface

Consider the user interface of an operating system. This is the executive portion that the users see when they first turn on the machine. Through this interface a user controls the system, runs the programs, and manipulates data files. On a traditional operating system, the system executive is a command interpreter. The command interpreter interacts with the user through a predefined command language similar to conventional programming languages. It is a rigid, somewhat cryptic, and artificial syntax for the commands that the interpreter will legally accept. For example, examine the commands used in several popular operating systems to delete the file containing a *Computer Design* article:

CP/M	`ERA B:CmprDsgn.Tex`
Apple DOS	`DELETE Computer Design Article,S6,D2`
MS-Dos	`ERASE B:CmprDsgn.Tex`
Unix	`RM/USR/Bruce/Publications/Computer Design`
UCSD p-System	`F R Pubs:CmptrDesgn.Text`

Compare these traditional operating system commands with the Lisa user interface. Here, a document icon is simply dropped into the Wastebasket Icon. While both methods perform essentially the same function, the command syntaxes are certainly not intuitive or easy to remember. If the actual command is ERA, it then does no good to try KILL, DELETE, REMOVE, or even ERASE. Also, commands will not work if B-, B–, or B/ instead of the B= are used in the file name. And, of course, every data object in the system must have a unique file name to be used when it is accessed. Because file names must be abbreviated to fit within the maximum file name length allowed by each system, they tend to be very cryptic. Lisa allows the name of a document to be almost any length or form. Names need not even be unique.

Why use a command language to communicate with traditional operating systems? Because programmers have a lot of experience with such languages and get plenty of practice in using them. Knowing how to precisely specify syntax and knowing certain programming techniques allow them to implement languages quickly and efficiently. Therefore, the choice of a command language interface for operating systems is largely for the convenience of the designer and implementer of that system. Such a command language interface is certainly not selected for the convenience of a user who is not a computer expert.

An unfortunate side effect of a command language interface is the heavy use of modes that restrict system functions. For example, most text editors have an insert mode that allows typed text to be inserted into the file. Modes are objectionable for many reasons. The biggest reason, however, is the myriad details that users must remember. These include how to get into and out of a mode, what commands are and are not available, and most importantly, what mode they are currently in.

It is probably impossible to design a serious system that has no modes whatsoever. However, too many modes gives a user a feeling of constantly

navigating a command maze. This may be fun in a game like Adventure, but it is frustrating and tiresome in the everyday use of an operating system.

Heavy use of modes also produces an inconsistent user interface. Commands and capabilities in one mode are not usually available in another. In most systems, for example, the commands for editing text entered into a text editor are not available for editing the text entered to a file name request. Worse still, the same command may not even have the same meaning in every mode. For example, in one system, the command R is used to Run a program, Remove a file, Replace selected text, or even to insert the letter R into a text file. Conversely, two completely different commands may actually invoke similar or even identical functions; for example, lines are *deleted*, but files are *erased*.

Compounding this problem of inconsistency in the user interface are the application programs used with an operating system. Because application programs are designed and sold separately from the system itself, more differences exist between such programs and the operating system than between various parts of the system. This is particularly true of portable application programs. Clearly, such programs, designed to operate with a number of different operating systems, will not be particularly consistent with any of them. It is practically impossible to expect one conventional application to provide commands that invoke functions similar with another.

Operating system calls

Although it is Lisa's user interface that one first notices, the fundamental system calls of the operating system are what make the software revolutionary. Lisa's operating system, designed specifically as a single-user system, does not need the excess capabilities built into multi-user, timesharing operating systems.

The operating system kernel provides multitasking support to the multiple, simultaneous windows displayed on the Lisa screen and the switching among them. In fact, an independent Lisa task is associated with each window. Lisa's multitasking is also used to allow such concurrent operations as foreground user interaction and background printing. Sophisticated memory management allows these multiple tasks to efficiently use and share system memory.

Specially designed to provide reliable storage of information, the Lisa File System redundantly distributes and stores critical file system data such as file directories. In the event of damage to the storage media, an operating system Scavenger can repair damaged data and recover the user's information. The file system provides device independent access to information through a byte-stream input/output interface.

Management capabilities of the graphics screen are an integral part of the operating system design.

Lisa's operating system has additional capabilities that distinguish it from traditional systems. Graphics and the desktop model are not just simply an appendage to the operating system. Management capabilities of the graphics screen are an integral part of the operating system design. The Window Manager is responsible for keeping track of the number of open windows, the location of each on the screen, the size of each, and which windows are in front of or behind the other windows. For each window covered by other windows, and therefore partially obscured, this Window Manager calculates that portion currently visible. QuickDraw, a high speed, bit-map graphics package, automatically restricts or clips any output to just that portion of the visible display window. When windows are moved, resized, or otherwise changed, Window Manager redisplays uncovered portions of windows. As a result, application designers need not worry about where on the screen windows are located, or how much is currently visible.

Similarly, mouse and keyboard support are an integral part of the operating system. Hardware interface software responds to interrupts from such input devices as the mouse or keyboard and queues input event information so that it is not lost if the application is busy. The Event Manager classifies these events and routes them to the proper window.

One of the most important aspects of Lisa is its printing technology. Superb drawings, calculations, or reports on a computer are insufficient if one cannot then print this information for others. Lisa supports both dot-matrix and daisy wheel printers. The guiding philosophy behind Lisa's advanced printing technology is, what you see on the screen is exactly what you will get on the printed page. This even extends to printing good quality graphics, as well as the usual text, on a daisy wheel printer.

Closely associated with the Lisa Operating System is a library of software modules (Fig 2). These modules perform various functions frequently needed by the Lisa application programs. The use of library modules saves an application designer the time it would take to develop similar

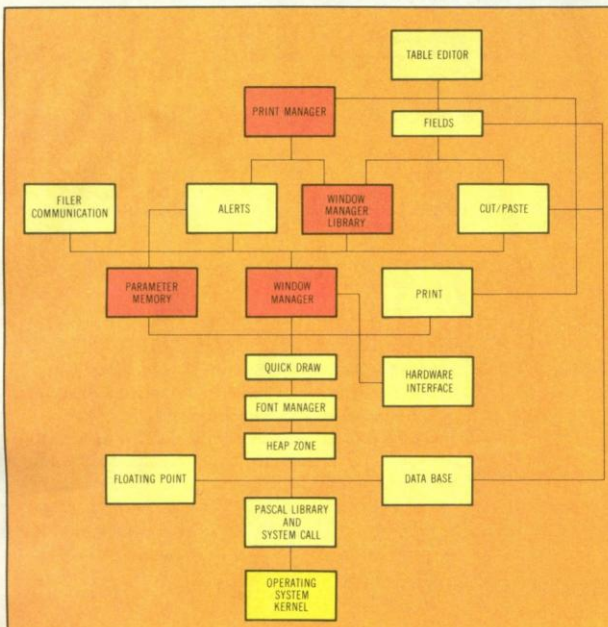

Fig 2 An integrated package of software supports all Lisa functions. The operating system kernel draws upon applications through system calls to the software library.

modules; it saves space on the disk; space in memory; and, most importantly, guarantees consistency among the applications. There are modules to display and select from pulldown menus, to allow viewing of different portions of a document via scroll bars, to display alert messages informing the user of errors, to enter and edit single lines of text, to perform floating point computations, and to access database information.

The level of capability and power provided by Lisa's operating system and its library of software modules goes far beyond any traditional system. But, providing additional capability allows the Lisa system to present the user with a degree of simplicity never seen before in traditional operating systems. The high degree of integration between hardware and operating system software makes these advances possible.

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OPTIMIZING XENIX I/O

The realtime I/O burden associated with Unix-like operating systems running on 16-bit computers can be overcome with tightly coupled processors and carefully designed disk subsystems.

by Paul Bottorff and Bill Potts

High performance microprocessors, inexpensive Winchester disk drives, and low cost high density dynamic random access memories are making it feasible to incorporate minicomputer operating systems like Unix into multi-user/multitasking microcomputers. The only operating system that runs successfully on all classes of computers from mainframe to micro, Unix has emerged as a *de facto* standard for high end 16-bit multi-user applications. However, before Unix and its derivatives can be efficiently integrated into a microcomputer environment, certain hardware design problems previously limited to larger computer systems must be solved.

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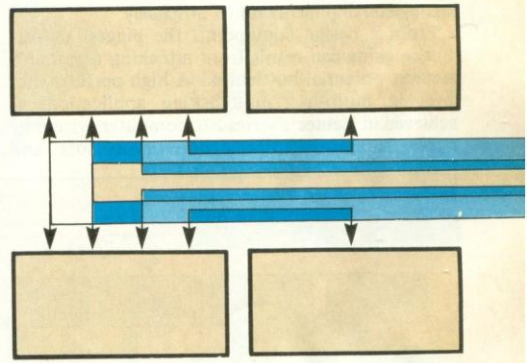

The features of Unix are well documented. It is an interactive, machine-independent operating system that runs programs concurrently, allowing information exchange among operating programs. Moreover, it features a powerful command set, hierarchical file structure, and hundreds of utilities for program development. Microsoft's Xenix version further enhances file management and increases data integrity and file protection.

In an effective multitasking operating system, the processor must provide hardware support for multiplexing both processing time and addresses. Such hardware is typically divided into two sections; one handles memory management and the other, program protection. The memory management unit (MMU) allows the operating system to

The biggest performance gains can result from attacking a system's greatest potential bottleneck.

efficiently execute more programs than it has physical memory to hold, while the program protection unit keeps programs from damaging one another in case of an operational error.

Xenix operates in a highly multiplexed environment. Since it requires a computer system that can accommodate 3M to 12M bytes of code, it places a much heavier load on its input/output (I/O) devices than single-user/single-tasking operating systems. As a result of the heavy load placed on the disk file system for programs, data, and temporary storage, a Xenix based system is typically paced by its system disk. Moreover, the demands of several users generate very high interrupt loads on the system bus. In theory, the line load under byte-by-byte interrupts could totally consume the processing capacity of a 16-bit microprocessor.

Bus mastership increases I/O efficiency

From a design standpoint, the biggest performance gains can result from attacking a system's greatest potential bottleneck. A high performance level in multi-user/multitasking applications is achieved in Zentec's series 2000 computer system by tightly coupling multiple microprocessors and establishing an arbitration scheme to maximize I/O efficiency (Fig 1). Each processor shares the common parallel bus path. Also, each processor is a bus master—no one device is slaved to another. Moreover, each processor performs a different system function, and no processor subset can duplicate the function of any individual one.

Due to the high demand Xenix places on disk I/O, the main system bottleneck is the disk access. The disk system stores the operating system programs, and contains much of the data these programs use. Occasionally, it must swap programs and data that are waiting for operator intervention into and out of memory. Each of these functions places different demands on the disk subsystem. For example, operating system programs for Xenix occupy from 3M to 12M bytes, and require the storage capacity of a hard disk. From a performance standpoint, the operating system must be able to retrieve segments of itself from disk very quickly. A disk controller with a high transfer rate and multisector transfer capability can optimize the system for program load.

Xenix also supports linked files. This allows files stored on the system to change without an operator intervening to assign or clear file space. Since the actual file data are not necessarily contiguous, the system must have fast random access characteristics. The drive's characteristics primarily determine the random access time for a disk subsystem. The subsystem can optimize file accesses in multidrive systems through seek overlap.

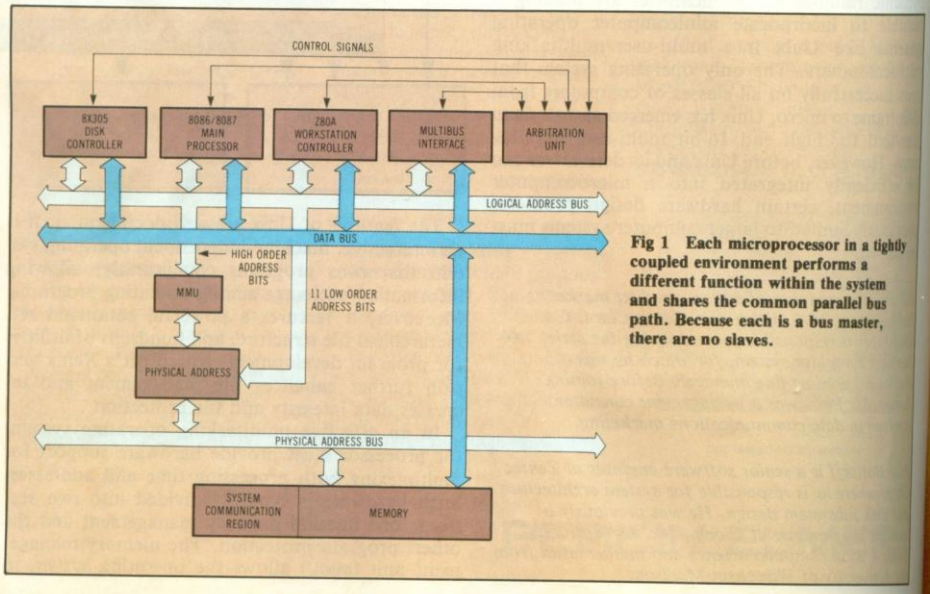

Fig 1 Each microprocessor in a tightly coupled environment performs a different function within the system and shares the common parallel bus path. Because each is a bus master, there are no slaves.

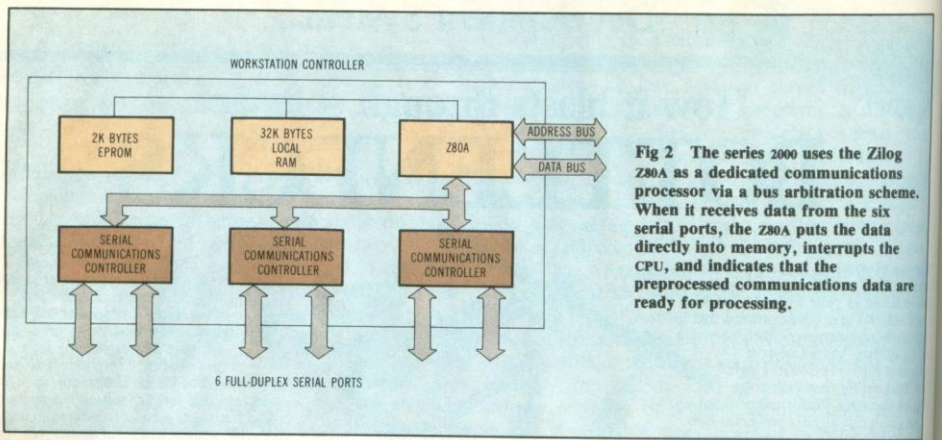

Fig 2 The series 2000 uses the Zilog Z80A as a dedicated communications processor via a bus arbitration scheme. When it receives data from the six serial ports, the Z80A puts the data directly into memory, interrupts the CPU, and indicates that the preprocessed communications data are ready for processing.

Xenix allows more programs to run concurrently than it can store in physical random access memory (RAM), although no one program can exceed physical memory size. This is accomplished by transferring inactive programs to a special disk region called the swap area, which is organized in contiguous regions instead of linked ones. Swap area management dictates moving large portions of program code and data to and from disk quickly. This is best accomplished by realtime multisector transfers.

Since the Xenix system is multi-user, the disk subsystem should not hinder the central processing unit (CPU) by locking the bus for excessive time periods, or by forcing the processor to move data blocks from the controller buffers. One common method for unburdening the processor from heavy disk I/O activity uses direct memory access (DMA) controllers. DMA controllers transfer data between peripherals, such as a disk and memory, without involving the main processor. This approach's primary drawback is that although the main processor is not directly involved in the data transfer, it is typically not allowed to perform any other processing function. It simply waits. This is because the main processor's ability to access memory is interrupted while the DMA controller completes the data transfer.

To eliminate this waiting period, the series 2000 data bus features a high speed bus arbitration scheme. This arbitration scheme is actually an active part of the system bus that allows all processors and peripheral devices to access RAM on a priority basis. DMA controllers are not used because each I/O and system processor on the bus can access RAM. Since the bus arbitration overhead is very low (approximately 40 ns/word), all processors can compete on a word-by-word basis with a total bus bandwidth of 1.2M words/s (2.4M bytes/s). Thus, all processors on the bus are assured rapid access to RAM without locking out any other processor for an undue amount of time.

In particular, this high speed bus is used to accelerate disk transfers. Buffering is unnecessary in the disk controller because the bus can accommodate a 625k-byte/s transfer rate direct from a Winchester disk drive (without blocking the CPU or other I/O processors during a transfer. Instead, the system can realize the full transfer rate of a Winchester to move data into system RAM. Since it is unnecessary to slow the disk transfer rate at the controller, it is possible to transfer multiple sectors (up to 126k bytes) without resorting to disk interleaving. The series 2000 disk subsystem uses its drives at their maximum performance rate without appreciably degrading CPU execution. This microprocessor based multi-user/multitasking system is also one of the few of its kind to support up to four Winchester disk drives.

Dedicated processor decreases CPU interrupt load

Another I/O consideration in a multi-user/multitasking system is the interrupt load on the processor. Consider the interrupt load on a processor imposed by six input lines all running at 9.6k bps. Under typical conditions, the load is much less. However, the processing time per byte can be much more. It is best to remove from the CPU the burden of receiving byte-by-byte interrupts. To solve this problem, the system couples a Z80A dedicated communications processor through the bus arbitration scheme (Fig 2). In this way, the CPU need not process I/O a byte at a time.

Instead, the dedicated communications processor receives bytes and places them directly into system RAM. Once a line of data is completed or a special line condition is detected, the communications processor interrupts the CPU and informs it

that a block of preprocessed data is located in the CPU's RAM. The communications processor can operate in both local and shared memory. Therefore, it can process line activity without contending for the system bus and deposit the data directly into the CPU's RAM without CPU intervention.

In a multitasking environment, whether single-user or multi-user, the operating system must share a common RAM area with a number of user programs. To increase efficiency, the system hardware has to support the operating system. In addition, two problems must be addressed for efficient implementation. First, in order to access RAM, the hardware has to map the logical addresses that the CPU generates into physical addresses. This mapping must be done in a way that permits the operating system to alter it. The hardware must also make a number of physically noncontiguous RAM areas look logically contiguous to the processor.

Since all programs executed in a Xenix environment are bound to the same memory addresses, and more than one program must be resident in RAM at a time, it is necessary to make two or more distinct RAM areas seem to have the same logical addresses. In its simplest form, this can be accomplished in software by a pointer set. This pointer value is then added to each address the processor generates to form a physical RAM address. When the Xenix system decides to switch to a different program (context switch), it simply changes the pointer value.

The second problem that must be solved (in part by the MMU) is memory allocation for a new program being loaded into RAM. Consider what happens to RAM under multitasking as program

Unlike segmentation, the paging scheme never requires the operating system to reorganize RAM.

memory is allocated and de-allocated. As the system begins execution, no programs are in memory and it is easy to find RAM area for the new program. For example, suppose programs A, B, and C are initially loaded into RAM. After a time, program B completes. The system now attempts to run program D. However, if program D is larger than program B, it will not fit into the memory area made available by program B's completion. At this point, either the MMU must remap program D into memory areas that look logically contiguous to the CPU, or, the operating system must completely rearrange memory—a very time-consuming operation.

Two methods are used by MMUs to do this: segmentation (not to be confused with 8086-type segmentation) and paging. The series 2000 uses a paged memory management system (Fig 3). Under paging, the physical memory is divided into pages of some fixed size (in this case 2K bytes). The MMU implements a set of pointers that the operating system uses to point to physical memory pages. As a processor presents logical addresses to the MMU, each is used as a lookup address in a page table array. The new address is formed by replacing the high order bits of the logical address with the bits contained in the MMU pointer. In this way, a single program can be scattered throughout physical memory and still look logically contiguous.

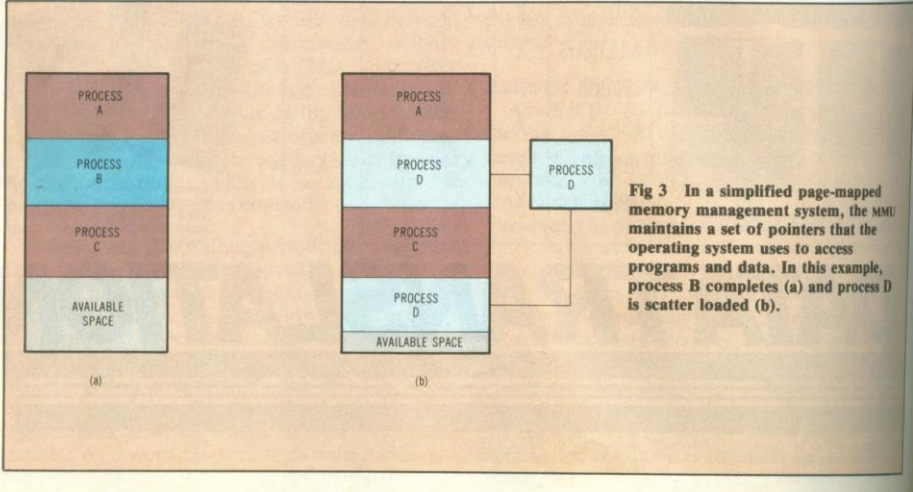

Fig 3 In a simplified page-mapped memory management system, the MMU maintains a set of pointers that the operating system uses to access programs and data. In this example, process B completes (a) and process D is scatter loaded (b).

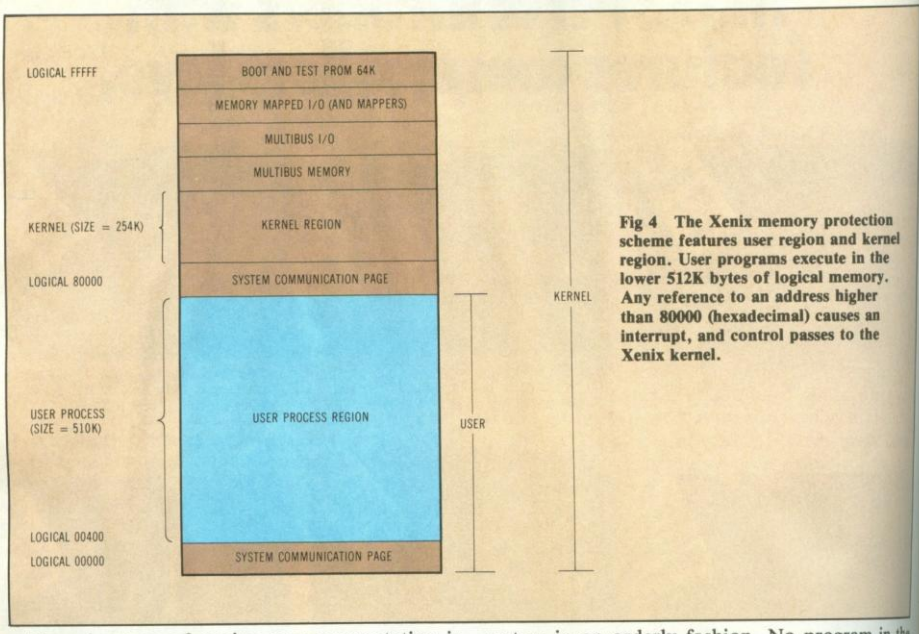

Fig 4 The Xenix memory protection scheme features user region and kernel region. User programs execute in the lower 512K bytes of logical memory. Any reference to an address higher than 80000 (hexadecimal) causes an interrupt, and control passes to the Xenix kernel.

The advantage of paging over segmentation is that the paging scheme never requires the operating system to reorganize RAM. Instead, programs can be placed anywhere in memory. Under a segmented system, where the size of the physical memory slot varies, the memory eventually becomes fragmented. This results in a high processing overhead.

To marry the MMU with the Xenix operating system, one more consideration must be made. The system not only manages running programs in memory, but also implements virtual memory to handle the programs. To perform the necessary management operations efficiently, the system must be able to move programs into and out of the swap area quickly, with as little overhead as possible. In particular, the system needs to take advantage of the disk controller's multisector transfer facilities.

To move a whole program to disk in a single command, the MMU must also be able to map the program area into a logically contiguous area for the disk controller. I/O mapping is accomplished in this system by associating the MMU with the system bus itself instead of with the processor. In this way, all disk transfers (or other I/O operation) can take advantage of the MMU.

Hardware protects programs

The Xenix operating system requires hardware to protect one program from another. This protection hardware must ensure that programs use the system in an orderly fashion. No program in the Xenix system can alter any memory it does not occupy, perform an I/O operation without requesting the system's assistance, or preclude the system from protecting itself against a detrimental program. To accomplish this, the series 2000 has a program protection unit (PPU) that captures illegal user program instructions (disable interrupts, out to I/O, etc). Moreover, the protection system prevents a user's program from altering any memory locations not assigned to that program.

The PPU also provides two methods of protection: page attributes and ring partitions. For each page map register, three attribute bits are available. These are Write Protect, Read Protect, and Stack Protect. Read and Write Protect prevent programs from reading or writing selected pages of logical memory. Stack Protect informs the system when the stack grows to within 128 bytes of the selected stack page's end. Stack warning also allows the system to dynamically allocate program stack space.

The second method the PPU provides is a 2-ring protection partition (Fig 4). Protection rings in the series 2000 are bound to logical addresses. The two rings are referred to as the user ring and the kernel ring. When the PPU operates in user mode, programs are restricted to operating in only the first 512K bytes of logical address space. If a reference to a high logical address space is made, an interrupt is presented to the CPU and the PPU switches to the kernel mode. Thus, programs running in the user

area are prevented from damaging the Xenix kernel located in high logical memory.

All I/O is memory mapped to high logical addresses. This prevents user programs from performing I/O operations. To further protect the system from user processes, the Halt and Interrupt Disable instructions are detected when the PPU is in the user mode. Should either be executed, a nonmaskable interrupt is presented to the CPU, and the PPU switches to the kernel state.

Given the design considerations for high system performance and efficient Xenix implementation, attention must eventually be focused on the system bus. With the intense pressure Xenix puts on all resources, and the necessity for memory management protection hardware, the CPU is indeed busy despite the help that the tightly coupled microprocessors provide.

Within this context, it is not necessary to consider the bus' theoretical bandwidth. Instead, consider the total amount of delay involved in reading and writing data to RAM. The actual access time for any system processor is determined by four factors: the RAM access time; the bus arbitration time; the MMU and PPU propagation delays; and the bus contender's priority. Since one design objective is to operate with unbuffered disk transfers, the disk controller is assigned the highest priority. The next priority is given to the bus so that the line processor can run free. Moreover, since Multibus devices can be synchronous, this option is given next priority. The CPU has the lowest bus priority.

In addition to being affected by low bus priority, the CPU must be able to cope with access times of approximately 800 ns. Therefore, the limit on processor execution speed is access time, not raw processor speed. There may also be longer intervals where the CPU is locked out by one of the other processors on the bus.

Pipelining decreases instruction access time

To solve RAM-bound and bus-bound problems, the Intel 8086 serves as the system microprocessor because of its pipelining capabilities. For a typical microprocessor (with or without prefetch), several steps are used to process an instruction, including fetching the instruction from memory, decoding it, fetching operands, executing the instruction, and storing the result in a register or memory. Each of these operations generally requires a single machine cycle.

The 8086 employs a bus interface unit (BIU) and an execution unit (EU). The BIU prefetches words from memory and places them in an instruction pipe that can store 6 bytes. The EU then takes instructions out of the pipe and executes them asynchronously, independent of the BIU. Whenever the pipe is less than full, the BIU fetches additional words—independent of and asynchronous to EU cycles. This pipelining architecture can significantly increase the RAM access time allowed for a given code execution speed. In addition, the 8086 need not wait for fetch completion before it starts instruction execution. The periodic long wait caused by bus contention does not prevent the processor from executing. An added benefit of using the 8086 in the system is availability of the 8087 arithmetic coprocessor.

An added benefit of using the 8086 in the system is availability of the 8087 arithmetic coprocessor.

Each of the other system processors has been selected to solve the particular demands of its function area. The Zilog Z80A serves as the workstation controller because it has low interrupt latency and a well-structured interrupt system. This, coupled with the Zilog serial communications controller, generates a complete prioritized interrupt daisy chain with good synchronous response characteristics. The Signetics 8X305 makes a good disk controller because it is a fast bipolar microprocessor with an instruction set specifically tailored for high speed I/O functions. This processor lets the series 2000 disk controller handle data at Winchester rates while maintaining small package size and interface intelligence.

The combination of Xenix and well-designed hardware results in a system optimized for a wide range of applications. As Xenix becomes more accepted, the market for such systems will no doubt be determined at the operating system level.

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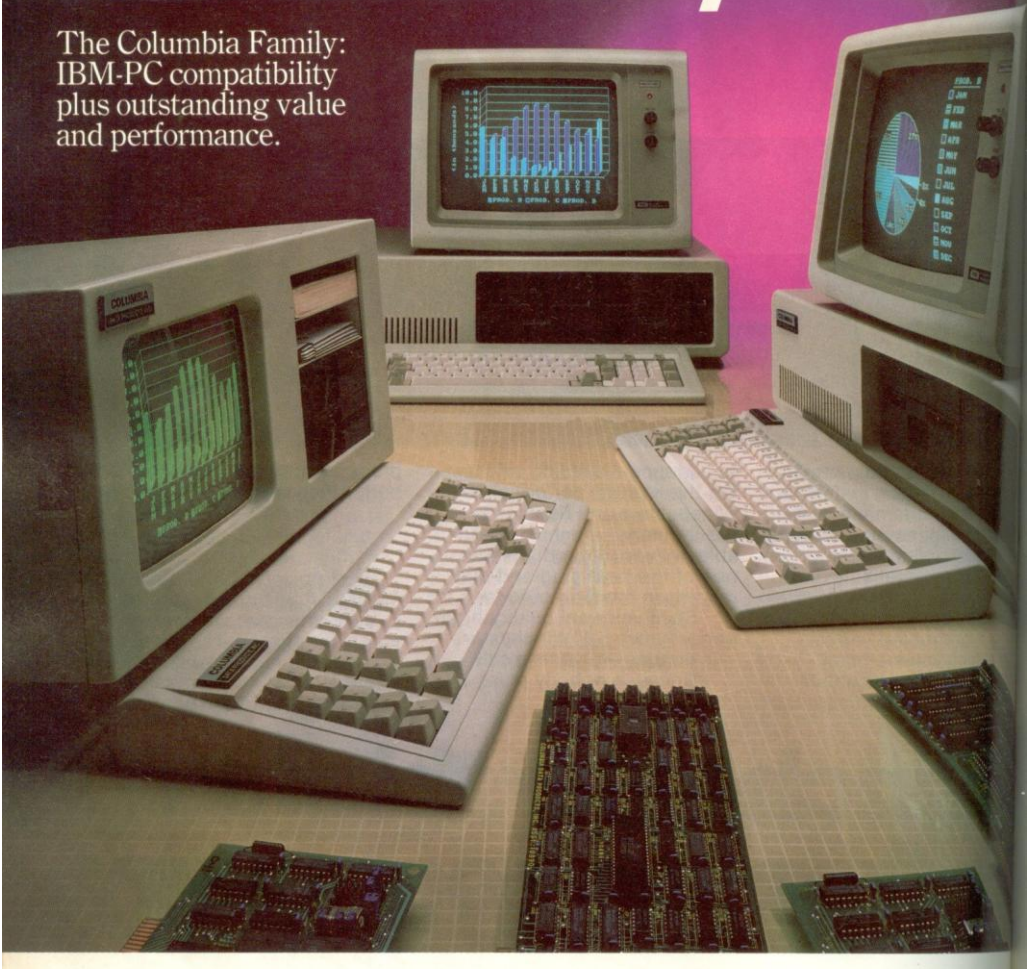

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CIRCLE 99

Compression unit squeezes data for high throughput

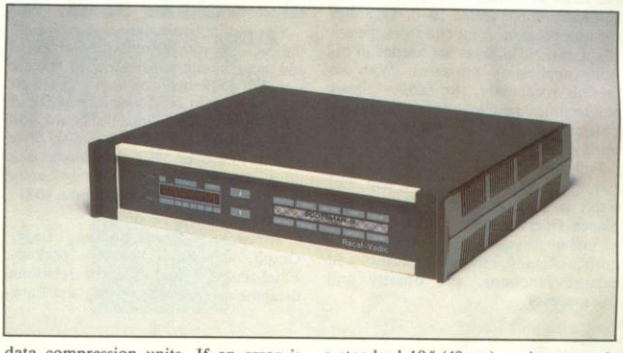
Scotsman III is a data compression unit designed to increase throughput in data networks by compressing data at a 2:1 ratio. It thereby effectively doubles the line capacity of existing communication links.

Hardware is divided into 3 sections; I/O processing, data compression, and data expansion. Initially, uncompressed digital data enter the I/O processing section through the port attached to the data terminal equipment (DTE). The bit stream's sync byte(s) and cyclic redundancy check (CRC) bits are removed, leaving only the message data. Data pass through the data compression section for transformation. At this point, the I/O section retrieves and inserts the data into a protocol. Data are then transmitted out of a port to the digital circuit-terminating equipment (DCE).

At the receiving end of the communications link, another compression unit accepts the compressed data and removes the protocol. Data are then sent to the expansion section where they are transformed into their original uncompressed state. Again, the I/O section takes the data, reinserts the original protocol, reconstructs the CRC, if any, and sends the data out to the DTE port.

To ensure data integrity, a CRC is generated that checks for errors between data compression units. If an error is introduced, the expanded data on the receiving end will not correspond to the original data from the transmitting side. The CRC sent to the receiving DTE is regenerated from the expanded data, masking the error. One bit of the data stream is inverted after the CRC is generated so the new CRC and the expanded data no longer correspond. This inversion allows the receiving DTE to detect an error.

Housed in a 3.5″ x 17.5″ (8.8- x 44.4-cm) plastic enclosure, the tabletop unit can be adapted for rackmounting in a standard 19″ (48-cm) equipment rack using a supplied rackmounting kit. The front panel contains 12 membrane switches, eight 7-segment LEDs and 3 indicator LEDs.

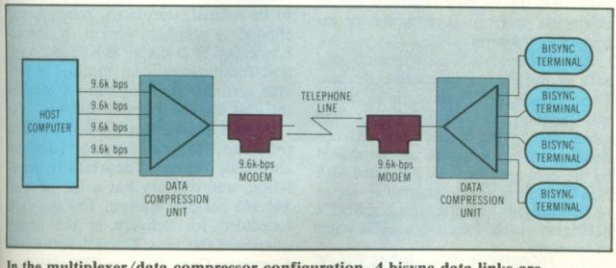


The data compressor is compatible with ASCII, EBCDIC or BAUDOT character codes with bisync, async, X.25, SDLC, or HDLC protocols. The Scotsman is interface compatible with standard RS-232-C/V.24 interfaces. It provides 15 functional diagnostics and end to end transparent operation.

Using the Scotsman III in conjunction with the Scotsman I and II statistical multiplexers can double the throughput of a high speed link. A 19.2k-bit data stream can be transmitted over conventional 9.6k-bps modems, or a 9.6k-bps high speed link over low cost 4.8k-bps modems and unconditioned telephone lines.

The data compressor has certain limitations. First, it does not compress random data but passes them through at a 1:1 ratio. Second, the unit has a 25-byte end to end delay, according to the DTE rate.

The unit price for the Scotsman III data compressor is $5000. Delivery is 90 days from receipt of order. **Racal-Vadic**, 1525 McCarthy Blvd, Milpitas, CA 95035. **Circle 258**



In the multiplexer/data compressor configuration, 4 bisync data links are compressed onto a single transmission line.

Workstation/software supports frontend development

The Easel Author workstation is designed as a support system for creating and handling dynamic visual images. It consists of 3 parts. The Easel software facility allows graphics and text to be created and manipulated, the video display is high resolution and touch sensitive, and the microprocessor system can be used either as a standalone system or a user station.

This workstation is designed for use in developing application interfaces by creating visual images along with their actions or by altering existing ones via the Easel authoring facility. The Easel software, implemented in C, separates the user program front end from the applications. No changes are needed in existing application programs. With an English vocabulary, the facility allows non-technical people to operate complex systems and trained programmers to become more efficient.

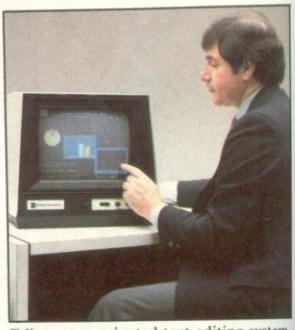
Full-color graphic capabilities include zoom, enlarge, shrink, distort, pan, and scroll in both horizontal and vertical planes. Operations include management of unlimited segments, windows, viewports, clipping, framing, shrink and enlarge functions, and opacity and transparency.

Easel's software permits flexibility at runtime. Runtime responses to users or applications can modify the screen; areas of the screen can become active or stop being responsive. Additionally, multiple regions can transmit data to or receive data from applications running remotely or locally.

Further, Easel offers pixel level addressing, stacking of regions with automatic visual priorities, and user definable, multiple fonts. The user can execute commands, complete routines, and create files and graphic images by touching the appropriate information on the screen.

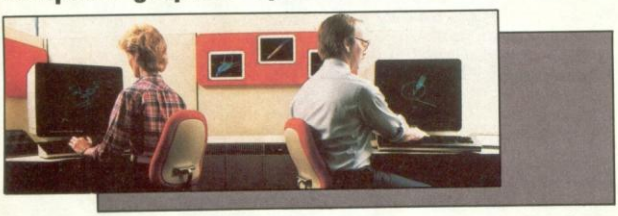
The author workstation is based on the MC68000 with automatic segmented and paged memory management. It has a standard 512K bytes of RAM expandable to 1.5M bytes in 256K-byte increments. A Winchester/floppy controller board controls a 1M-byte 5¼" floppy disk drive and a 10M-byte 5¼" Winchester disk drive. The video display is a 14" color monitor with a touch screen and a 1000 x 750 resolution.

Software options include Easel-Graph, a business graphics package; Easel-DBMS, a user oriented relational database management system; and Easel-Edit, a user oriented text editing system. A C compiler is offered with the standard system; Pascal, BASIC, COBOL, and FORTRAN compilers are optional.



Easel software is licensed on a per CPU basis, and the licensing fee varies according to volume and type of computer. Price of the Easel author workstation is $19,900. A range of options are available including hardcopy printout, keyboard, and digitizer tablet. **Interactive Images Inc,** 21 Olympia Ave, Woburn, MA 01801.
Circle 259

Computer graphics system offers dual workstations



For applications requiring high performance, realtime, and 2-D and 3-D graphics capabilities, the PS 300 series of computer graphics systems offers model PS 320 with dual graphics stations. The system allows 2 users to share 1 control unit for a cost-effective approach to graphics requirements.

Two independent users are supported by the system architecture. They share a common control unit consisting of a graphics control processor, mass memory, and a display processor. A second graphics control processor can be added to improve interactive performance in applications where extensive local computations are required. Memory capacity is 1M byte in the standard configuration; as an option, memory capacity can be increased to 4M bytes.

Additionally, each user station can have a variety of interactive devices. These include an alphanumeric keyboard with function keys, control dials, a data tablet, and lighted function keys. An optional hardcopy interface can be shared by the dual user stations. Equipped with high resolution, monochromatic, vector refresh displays, each station has 8192 x 8192 addressable locations and 64 levels of intensity.

Using standard RS-232-C or RS-449 communications lines, the system will operate with virtually any size or model host computer. High speed data transfer interfaces are also supported. These include DEC DMR11-AE, PS 300/IBM 3278, and the DEC VAX parallel.

The architecture of the PS 300 family allows the system to be expanded and upgraded. All members of the family are program compatible, permitting programs to run on other models without complex conversions.

Compatibility also exists in software routines. Software features allow images to be rotated, translated, zoomed, and clipped. A graphics support routine enhancement is available as a collection of host computer resident routines to provide efficient communications between the host and the graphics systems.

A basic PS 320 configuration, including processor, 1M byte of memory, 2 monochromatic displays, 2 data tablets, installation, and delivery has a list price of $40,945 per user station. The system is scheduled for delivery in the fourth quarter of this year. **Evans & Sutherland Computer Corp,** PO Box 8700, 580 Arapeen Dr, Salt Lake City, UT 84108.
Circle 260

Voice data entry terminal provides speech recognition

Using speech recognition technology, the Verbex 3000 voice data entry terminal allows efficient data entry. A user workstation and a speech processing unit (SPU) form the terminal.

All user workstations feature a close talking directional microphone headset, either wired or wireless, through which the user verbally enters data or commands. The user receives visual prompting and data verification via an alphanumeric display console. Workstation options include an audio response unit that repeats an input through the headset for verification, a remote visual display, and a keyboard CRT.

The SPU consists of a control computer, audio I/O, a high speed continuous speech processor, and a 1M-byte floppy disk drive. For I/O, 3 RS-232 ASCII serial ports are available with 9.6k-baud rates. Hardware options include an additional 1M-byte floppy disk drive or a 10M-byte Winchester disk drive, a printer, and additional communication interfaces.

After converting speech into digital form, the SPU compares it with the digitized user word patterns stored in memory. Establishment of the voice pattern in memory requires initial training and minimal retraining (under normal operation). The system responds to the voice pattern regardless of dialect, accent, or language. When the system recognizes the voice pattern, the data are repeated in less than 300 ms in visual or audio form. This allows the user to verify the accuracy of the input and the response immediately.

The 120-word standard vocabulary, which is determined by the customer, can be expanded to 360 words. An important system feature is its high accuracy (99%+) even if background noise reaches 85 dB. Background noise includes conversation, other equipment, and day to day variations in the user's voice.

Additionally, the terminal includes continuous speech recognition algorithm software, as well as software for enrollment and training, voice/keyboard data entry, and control and operating systems. Built-in self-test diagnostics ensure product integrity.

Designed for industrial environments, the system has 3 major application areas: CAD/CAM or CAE, material management, and quality control. In CAD/CAM or CAE, the terminal is appropriate for editing and entering symbol or label data. In material management, the terminal functions as the link between operators and automated equipment. In quality control, inspection speed and accuracy are increased through the fast verification of entered data.

Complete documentation and customer support packages are provided with the terminal. These packages include installation and training, applications development, and terminal use and maintenance. **Verbex, a div of Exxon Enterprises,** 2 Oak Park, Bedford, MA 01730.
Circle 261

Board test family features high throughput capacity

Based on a "computer behind the pins" approach, the HP 3065 board test family provides high-yield testing of large, complex digital and hybrid PC boards. All test stations in the system use a vector processor (bit-slice computer) to reduce long overhead time between tests and a HP minicomputer for overall control of the system.

Each vector processor increases the number of test vectors that can be executed using a set amount of test-pin memory. Complete vector sequences are applied to VLSI devices without reloading local RAM behind each pin. This allows thorough testing of devices without throughput penalties. The processor supports the 1, 0, Z, and X logic states, as well as K (keep) and T (toggle). The K and T states allow a single vector to perform different functions by deriving the next vector state from the previous one.

The system offers a testing speed greater than 30 ICs/s—a speed unaffected by IC complexity. At megahertz rates, most IC overdrive bursts are less than 500 μs. In this system, to decrease the inter-test time to this level, the amount of data required to describe a test is reduced and a local response comparison is performed. The hardware and software work together to transfer and store unique vectors only once.

Automatic test generation software allows the tests to be created quickly. ASCII data from a CAD system can be used to describe a board. A forms-entry package allows non-technical personnel to enter a board description or add to CAD generated data. Flexibility in naming nodes and devices permits schematics to be copied onto forms. Default forms, which reduce typing efforts, are available for each type of device.

The system provides software for in-circuit testing. This software, known as Safeguard In-Circuit, analyzes modified tests and minimizes damage or degradation potential. Traditional testing techniques require overdriving the outputs of upstream devices, which can cause device failure during testing or latent failures. The Safeguard software considers each test duration, number of outputs overdriven, and max overdrive current when analyzing each circuit test. It safeguards the board by keeping current, voltage, and IC temps below recommended levels.

The system controller is based on an HP minicomputer with a 132M-byte Winchester disk drive that has an integral tape backup. With a user friendly software environment, it supports various peripherals including line printers, magnetic tape drives, and any device fitting the IEEE 488 standard. Up to 3 programming stations and 3 test stations can be managed simultaneously by

the controller. Or it can concurrently manage up to 6 programming stations.

For the 3065 family components, the minimum usable configuration prices are $95,000 for the digital test station, $120,000 for the analog/digital test station, and $70,000 for the controller. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 262

Low cost color graphics terminals and copier

The Tektronix 4100 family of color graphics terminals is tailored to meet the needs of general data analysis, presentation graphing, CAD previewing, programming, and text editing. Combined with the 4695 color graphics copier, the terminals offer a low cost way to increase productivity with computer graphics tools.

Terminals are available in 3 models. Model 4105 features a 13″ color raster-scan display. It offers a display resolution of 480 x 360 pixels and a coordinate space of 4096 x 4096 addressable points. Model 4107 also features a 13″ display, with a display resolution of 640 x 480 pixels. The 4109 model features a 19″ display and a resolution of 640 x 480.

Common to all models are display graphics of up to 8 colors from a palette of 64 and a Color User Interface. The interface allows the operator to interactively select and mix colors through a set of special function keys. By using these keys, the operator can replace any color with a selected color.

A low-profile, detached keyboard is designed with 86 keys that include 4 special function keys, 8 user-definable function keys, and a 14-key numeric keypad. For graphic data input, a "joy disk" is built into the keyboard.

Data baud rates of 19.2k over an RS-232-C interface port are supported. Vector graphics can be sent at rates up to 9.6k baud.

The 4695 color graphics copier is plug compatible with the 4100 series of terminals through its parallel interface. The copier can place 120 dots/in both in horizontal and vertical directions, allowing up to 1280 x 960 dots per A-size image.

Copier speed is 1024 x 4 dots/s or 2.5 min/page for a typical copy. The unit also functions as a bidirectional matrix printer with speeds up to 20 chars/s.

Model 4105 is priced at $3995, model 4107 at $6950, and model 4109 at $9950. The copier costs $1950. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.
Circle 263

Thin-film heads/plated disks are Winchester features

The Cricket Winchester disk drive (CDC 9270-6) consists of read/write and control electronics, read/write heads, a track positioning actuator, media, and an air filtration system. The 3½″ disk drive was specifically designed for the OEM market.

The drive provides 6.38M bytes unformatted and 5M bytes formatted storage capacity. It is timing and format compatible with the industry standard ST506 interface that transfers data at a 5M-bps rate. Average seek time is 117 ms using a band stepper positioning method. Linear recording densities are 15,390 bpi and 450 tpi.

Using LSI circuit technology, the Cricket fits all drive electronics on a single PCB that is approximately one-third the size of boards used in 5¼″ Winchester drives. The drive measures 1.63″ x 4″ x 6.37″ (4.14 x 10 x 16.18 cm).

The drive operates with a direct-drive, brushless dc motor that rotates the spindle at 3566 rpm. A closed loop digital servo system uses servo information written on each track at the index mark. When a seek operation is done, the servo information is read and an internal microcomputer corrects track misalignments. The band actuator (connected to the stepper motor shaft) positions the read/write heads. Accurate positioning is performed by a stepper that stops at 0.9° per step.

These Winchesters use thin-film flying heads and a negative pressure air-bearing slider. Such a technique allows a lower head flying height and reduces the force of the self-loading heads. Thin-film heads and nickel-cobalt plated media also allow a design MTBF of 30,000 operating hours and an estimated service life of over 5 years. No preventive maintenance or operating adjustments are required.

Data reliability specifications include recoverable read errors of 1 in 10^{10} bits read, unrecoverable read errors of 1 in 10^{12} bits read, and seek errors of 1 in 10^{6} seeks. Power requirements are 5 V (±5%) at 0.6 A (0.7 A surge) and 12 V (±5%) at 0.9 A (1.6 A surge). Power dissipation is 14 W (run).

The drive has applications in small business systems, intelligent terminals, personal computers, word processing systems, and portable computers. In OEM quantities, the Cricket is priced at $465. Initial customer evaluation units will be available in this quarter. **Control Data Corp, OEM Product Sales,** PO Box 0, Minneapolis, MN 55440.
Circle 264

Magnetic printer

The MP6090 is a high speed printer offering 6000 1pm (88 pages/min) and perpendicular recording to produce 240- x 240-dot resolution. A line printer emulation capability permits std line printer formats using multiple fonts in both horizontal and vertical directions. Interface supports std Dataproducts protocols, while video interface allows custom fitting of printer to system for graphics applications. The system is $25,000 in OEM quantities. **Cynthia Peripheral Corp,** 3606 W Bayshore Rd, Palo Alto, CA 94303. **Circle 265**

Small computer printers

Three models of letter-quality daisy wheel printers are available. The MP100 (100-col) prints 14 cps and is priced at $595. The MP200 (132-col) prints 20 cps and is priced at $945. The MP300 (132-col) prints 31 cps and is priced at $1195. All models offer bidirectional printing and a noise level under 65 dB. Full support is provided for wordprocessing functions. The MP200 and MP300 have an auto-load feature that loads single-sheet paper. The printers use std Silver-Reed ribbons. **Morrow,** 600 McCormick St, San Leandro, CA 94577. **Circle 266**

Printer for data processing

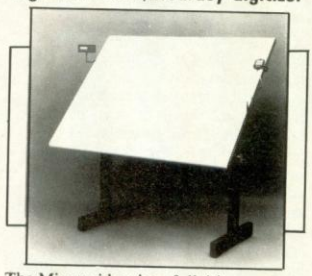
The DP-6500 Rapid/Scribe data processing printer uses an 18-needle printhead consisting of 2 vertical cols of 9 each. The printer achieves speeds of 500 chars/s at 10 chars/in and 540 chars/s at 12 chars/in with 275 lines/min when printing 80 cols. Features include enhanced mode printing with proportional spacing or at 10, 12, 15, and 16.4 chars/in at speeds up to 410 chars/s. There are 7 foreign character sets and USASCII. High resolution graphics provide a dot resolution of 72 or 144 dots/in. Std buffer storage is 4.5K bytes. In single quantities, the printer is $2995. **Anadex, Inc,** 9825 De Soto Ave, Chatsworth, CA 91311.

Circle 267

Expanded graphics terminals

Models D410 and D460 expand the Dasher® line of terminals. These terminals feature windowing and screen management capabilities. The 12″ terminals feature 24 lines of 81 cols displayed in a 10 x 12 dot matrix or 135 cols in a 12 x 12 dot matrix. There are up to 24 user definable windows. Bidirectional vertical scrolling and 162-col horizontal scrolling is available. The terminals support a complete set of editing commands and provide the ability to define up to 3572 additional characters (downline loadable from the host). The D410 is priced at $1635 the D460 is $1785. **Data General, Information Systems Div,** 4400 Computer Dr, Westboro, MA 01581. **Circle 268**

High resolution/accuracy digitizer



The Microgrid series of digitizer systems is both plug and I/O compatible with ID, Supergrid, and Summagrid digitizers. It offers 1k-1pi resolution and ±0.010″ accuracy, with increased accuracy available as an option. Reliability features include a single controller/interface board, a power-up self-test, and interactive terminal diagnostics. Std interfaces include dual RS-232 ports and an 8-bit parallel port. All tablet functions, including operating modes, sampling rate, and resolution, are remotely controllable from the host. **Summagraphics Corp,** 35 Brentwood Ave, PO Box 781, Fairfield, CT 06430. **Circle 269**

Portable terminal

The model 740 Port-a-Store is a handheld portable data entry device featuring 4k chars of memory and visual display capabilities. Online, the user can enter data manually or transmit stored data to voice response based data collection systems. Offline, the user can store and review data. The 20-key battery operated unit transmits touchtone signals

through an acoustic coupler that press fits over a telephone mouth piece. User programmable features include line terminator, line length, transmission speed, and transmission delay. The 740 is priced at $333, single quantity. **Interface Technology Inc,** 10500 Kahlmeyer Dr, St Louis, MO 63132. **Circle 270**

Display terminal

A display station, the UTS 30 can function as an editing terminal or a user-programmable terminal/desktop computer. It supports 4 printers, a 5¼″ diskette subsystem with up to 2.6M bytes of storage, and a magnetic strip reader. Operating modes include Uniscope and DDP-4000 protocols. Character generation is in a 10 x 16 dot matrix with a refresh rate of 70 times/s. Soft character generator stores 256 or 512 chars. Transmission code is 7 level ASCII plus parity bit with transmission rates up to 9.6k bps. Terminal costs $2277. **Sperry Corp, Computer Systems,** PO Box 500, Blue Bell, PA 19424. **Circle 271**

CAD/CAM graphics terminal

The GXT-1000 is an interactive color graphics terminal for use in single- or multi-user CAD/CAM systems. It has a display resolution of up to 1280 x 1024, 20k-vector/s max system throughput, and 16 video memory planes. Full 2-D transformations are std with 3-D hidden surface removal and shading optional. Easy roam, a realtime pan function and smooth zoom, exists in a 64K x 64K space. Interfaces include data tablet, mouse, printer, and color plotter. Host communications are via RS-232 (19.2k baud), optional RS-422 (300k baud), or parallel DMA (400k words/s). Pricing is set at $14,560. In 100s, pricing is under $10,000. **Matrox Electronic Systems Ltd,** 5800 Andover Ave, Montreal, Quebec H4T 1H4. **Circle 272**

ANSI-std CRT

The Guru is a CRT terminal that gives users ANSI stds with max storage and display capability. The terminal provides 28K of display memory, which can be scrolled or zoomed horizontally and vertically. It has user selectable memory formats ranging up to 255 col x 250 lines and displays up to 170 col x 66 lines. The keyboard offers 38 programmable keys on 60 levels. The keys are programmable with any ASCII string with local only, send only, and repeat control. The terminal is priced at $2395. **Ann Arbor Terminals, Inc**, 6175 Jackson Rd, Ann Arbor, MI 48103. **Circle 273**

Versatile terminal unit

The 8105 is a multipurpose unit that performs like an electronic typewriter, a send-receive computer terminal, and a printer. It has a 105-char printwheel for use in typewriter mode. This mode includes a format memory for 10 different margin and tab stops, line memory of 1000 chars, and lift-off correction. An RS-232 interface is used in data transmission. Printer speed is 22 chars/s. Baud rates range from 110 to 9.6k bps. Users can keyboard select parameters for parity, data bits, and stop bits. Unit is priced at $1895. **Facit, Inc**, 235 Main Dunstable Rd, Nashua, NH 03061.

Circle 274

Computer/telecomm terminal

The Communicator II, a compact communications terminal, is capable of both voice and data communications. It provides online or auto-programmed delay transmission of text or voice and access to in-house or remote computers. Additional features include a word processor, memory typewriter, telephone answering machine and recorder, dictating machine, and dictionary and auto-dialer. The terminal can save up to 70% of phone line charges by auto-send/receive at low-rate hours. **The Scott-Thompson Corp**, 7 Westchester Plaza, Elmsford, NY 10523.

Circle 275

DATA CONVERSION

STD bus D-A converter

The LM16STD D-A converter provides up to 16 channels of conversion with 4-quadrant multiplication. Features include 4 buffered, precision, 0- to 12-V sources, 8-bit resolution, and a 1-μs data rate along with $\pm$ ½ LSB accuracy, $\pm$2 LSB gain error, and 16 independently latched channels. Power requirements are 5V and $\pm$12 V at 100 mA. Channel outputs are buffered by op amps capable of supplying full scale voltage swings with a 5-kΩ load. Operating temp range is 0 to 70 °C. **LM Inc**, 2046 Armacost Ave, Los Angeles, CA 90025.

Circle 276

8-line MUX

The Saturn SZV11 is a Q-bus, RS-232-C, 8-line MUX that is compatible with DEC's DZ11 or DZV11. The chip supports 22-bit addressing and runs all standard DEC diagnostics and operating system software. Other features include per-line programmable baud rate, configuration flexibility, and modem controls for full-duplex, dial-up auto-answer operation. Using dual UARTS and a microprogrammed state machine allows the device's packing density to quadruple. The MUX lists for $1150, with discounts available. **Saturn Systems Inc**, 6875 Washington Ave S, Minneapolis, MN 55435. **Circle 277**

DAC board

For process control applications, the U-8680 analog output board converts digital commands on a dual 8-bit parallel bus in 30 independent analog output channels. Each channel contains a 10-bit latched DAC and is equipped with 20-turn precision zero and full-scale adjust pots. Each channel also has a 4- to 20-mA current loop output plus a switch selectable $-$5- to 5-V or 0- to 10-V output. Single-piece price of a 30-channel board is $2995; a 15-channel board is available for $1995. **Ranon Technology Corp**, 1420 E St Andrew Pl, Santa Ana, CA 92705. **Circle 278**

Hybrid A-D converter

Using gate-array technology, the MN574A is a successive-approx, 12-bit A-D converter offering 4 user selectable input ranges. Packaged in a 28-pin DIP, the device contains all the interface logic and control circuitry to mate with popular 8- and 16-bit microprocessors. The 3-state output buffer connects to the data bus and can be read either as one 12-bit word or as two 8-bit bytes. Initial zero and full-scale accuracy errors are below $\pm$0.05% FSR and $\pm$0.3% FSR, respectively. Six versions of the device are available with no missing codes over both 0 to 70 °C and $-$55 to 125 °C ranges. Prices (100s) range from $34.50 to $230. **Micro Networks Co**, 324 Clark St, Worcester, MA 01606.

Circle 279

Low priced DAC

To generate precision voltages or currents, the DAC1146 offers $\pm$0.00076% FSR accuracy and 18-bit resolution. DAC features an output amp and a 10-V internal reference with analog output ranges of $-$2 mA, $\pm$1 mA, 5 V, 10 V, $\pm$5 V, and $\pm$10 V, all pin programmable. Device operates with power supplies ranging from $\pm$11.5 to $\pm$16 V and dissipates 600 mW. For digital audio applications, the parameters include max 6-μs settling time and a dynamic range of 96 dB for 16-bit input. Chip is priced at $130 in 100-piece quantities. **Analog Devices, Inc**, Route 1 Industrial Pk, Norwood, MA 02062. **Circle 280**

IBM PC alternative

The VP is a 16-bit microcomputer that offers both IBM hardware and software compatibility. The system is bundled with business software at a price lower than an IBM system. The VP provides 128K to 256K bytes of memory with additional storage capacity available in dual half-high 320K-byte floppy disk drives. Features include one RS-232 port, a parallel printer port, and a 9″ monitor with graphics capability. The unit will be sold, complete with software, for $2995. **Columbia Data Products, Inc, Computer/Peripherals Systems,** 8990 Rte 108, Columbia, MD 21045.
Circle 281

Standalone or CPU board

The OB68K1A single-board computer implements the MC68000 on the Multibus/IEEE 796 bus. Board is designed to operate as a standalone computer system for realtime applications or as a system CPU. Supporting the CPU is either 32K or 128K bytes of dual-ported RAM operating through a hardware refresh controller. Device uses 256K-byte RAM chips (upgradable to 512K bytes) and has six 28-pin sockets for EPROMS. I/O is provided by 2 RS-232-C serial ports and 40 lines of programmable parallel I/O. **Omnibyte Corp,** 245 W Roosevelt Rd, Building 1-5, West Chicago, IL 60185.
Circle 282

Piggyback micro

Based on the piggyback PROM concept, the MK97501 and MK97521 incorporate a 28-pin socket located directly on top of a single-chip microcomputer. The chips feature 8K bytes of externally addressable memory, 8K bytes of ROM, 64-byte scratchpad RAM, 64-byte executable RAM, and a programmable binary counter. The MK97521 has 16 bits of TTL and 16 bits of open drain I/O, while the MK97501 has all TTL I/O. The parts are hardware and software compatible with the MK3870 family so existing data bases can be used. The entire micro requires the space needed for a 40-pin package. In 100-piece quantities, the price is $45.30 for either model. **Mostek Corp, sub of United Technologies Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 283

Industrial microcomputer board

The CMOS Industrial Microcomputer (CIM-804) is a high speed 4-MHz microcomputer board. It features 2K bytes of RAM, 4K bytes of shadow PROM, and 22 programmable I/O lines. The CPU is based on the NSC800 and executes the Z80 instruction set. Applications include industrial instrumentation, pipeline monitoring and control, and robotics. Boards operate at temps from −40 to 85 °C with low power consumption levels. Available immediately, the boards are priced at $590. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 284

CPU enhances LSI-11 performance

Model SBP-68Q is a 68000 based CPU designed for increased speed and performance of LSI-11 computers. For high speed multitasking, multi-user operations on a Q-bus system, the board provides a high speed memory bus and multiple MMUS. Internally, the processor provides 32-bit data and address registers, memory-mapped I/O and 14 addressing modes. The board executes 16M-byte programs and permits direct addressing of up to 16M bytes of main memory. The processor is $2880. **Ranyan Computer Enhancement Systems,** 15239 Springdale St, Huntington Beach, CA 92649.
Circle 285

Video disk computer

Touché is an interactive video disk system with an infrared touch-sensitive screen. The screen gives rapid, fingertip access to 54k frames of studio quality visuals, computer generated text and graphics, and stereo sound tracks stored on laser optical video disks. The unit consists of an Apple IIe microcomputer, video disk player, high resolution video monitor, and a 5¼″ disk drive. The storage capacity is 300K bytes with space available for additions of a second drive or 5M-to 20M-byte hard disk. The complete system is priced at $4995. **International Institute of Applied Technology,** 2121 Wisconsin Ave NW, Washington, DC 20007.
Circle 286

Multi-user microcomputer

The CARIBE microcomputer offers 2 operating systems, 5 applications languages, and peripheral devices from over 60 different manufacturers. BLIS/COBOL and BITS/BASIC operating systems provide flexibility in upgrading software to the supermini and mainframe level. The CPU uses the Fairchild 9445 microprocessor, with MTBF of 10k hours. Five standard configurations offer 20M-, 30M-, or 50M-byte Winchester disk storage and streaming tape backup. Pricing for the system runs from $9980 to $13,830. **Rianda Electronics,** 2535 Via Palma, Anaheim, CA 92801.
Circle 287

Portable computer

The Kaypro 4 portable computer features a total floppy disk capacity of 788K bytes in 2 double-sided double-density disks. Machine is sold with all programming bundled and packaged with the system. Computer is Z80 based and includes a keyboard with 20 programmable keys and a 9″ green phosphor screen. Available software allows the computer to read and write files of Osborne, Radio Shack, and Xerox. The system is priced at $1995. **Kaypro Div, Non-Linear Systems, Inc,** 533 Stevens Ave, Solana Beach, CA 92075.
Circle 288

Multibus board computer

The AM97/8605 is a 16-bit computer system on a single Multibus board. It includes an 8086 CPU with 5- or 8-MHz operation, 8K bytes of RAM, 2 serial ports, and 24 programmable I/O lines. The board has sockets for 64K bytes of EPROM, 16K-byte expansion memory, and an 8087 numeric data coprocessor. It features 9 levels of vectored interrupt control and a Multibus multimaster interface. The configuration makes it suitable for ROM-intensive control and I/O applications. It is designed to work as both a standalone CPU and a slave CPU in a multiple-master system. Computer is priced at $1645. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 289

Low cost keyboard

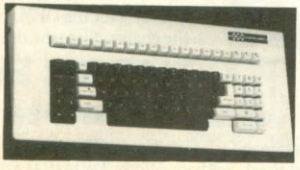
A microprocessor-based keyboard, the INDUCTRIC® is designed to DIN standards. Contactless keyswitch modules require no physical connection to the PCB and can be easily replaced. Additional features include true n-key rollover and 100M life cycle. Key locations, encoding, interface electronics, and keycap legends and colors are user defined. Other options are custom enclosures, tactile feel, and on- or offboard electronics. Style 84KT-14, without enclosure, is $200, and style 84KT-14E, with enclosure is $250. **Keytek Div, Elco Corp,** 6424 Warren Dr, Norcross, GA 30093.
Circle 290

Clock oscillators

Available at any frequency in the 1- to 15-MHz range, the CO-412 series are CMOS clock oscillators. Qualified Products Listed to MIL-0-55310/18, stability is ±50 ppm total over −55 to 125 °C, with an option of ±5 ppm over the 0 to 50 °C range. The oscillator series meets MIL-STD-883 fine leak of 10^{-8} atm cc/s, and internal hybrid conforms to MIL-M-38510. Random vibration of 20 g to 2 kHz is met through the use of a 3-point crystal mount. Housed in a 0.2″ (5.1-mm) resistance welded case, the series is available with either a 4- or 14-pin DIP compatible header. **Vectron Laboratories, Inc,** 166 Glover Ave, Norwalk, CT 06850.
Circle 291

High-tech keyboard

The 8000 series microprocessor keyboard is a 96-key system that is compatible with computer systems having a serial keyboard interface. The key layout consists of a std 53-key typewriter arrangement, a left-hand function keypad of 10 keys, and a 13-key numeric keypad on the right. Each keyboard uses a single-chip microcomputer controller that handles all keyboard functions. All keycaps are nonglare, 2 shot molded sculptured style. A metal frame provides easy mounting, resistance to static electricity and ESD, and acts as a barrier to foreign objects and spills. **George Risk Industries, Inc,** GRI Plaza, Kimball, NE 69145.
Circle 292



SOFTWARE

Circuit design software

An Electrical Ladder Diagramming (ELD) software module has applications in electromechanical and process control. With minimal input, design automation features enable designers to create up to 128 sheets of both intricate and unusual ladder structures in full compliance with ANSI and JIC stds. For component placement, features include a potent symbol capacity, intelligent device library, and a snap-to-position function. Auto generation of wire net lists ensures that documentation identifies production requirements. The module is base priced at $15,000. **Gerber Systems Technology, Inc,** 40 Gerber Rd East, South Windsor, CT 06074.
Circle 293

Enhanced Unix system

Aux is an enhanced version of the Unix operating system and is offered as a supplement to the operating system for the DN series of workstations. The user has access to a network-wide virtual memory and will not experience performance degradation as workstations are added to the network. The combination of Berkeley and Bell Unix allows over 100 commands, including VI Editor and C shell. Also supported is the Unix-to-Unix communications program for sending electronic mail between local and remote Unix systems. The license for the operating environment is priced at $1000 per workstation. **Apollo Computer Inc,** 15 Elizabeth Dr, Chelmsford, MA 01824.
Circle 294

16-bit assembler

A structured macro cross assembler, designated the ASM-68200, offers assembly language programming for the MK68200 16-bit single-chip computer. It consists of the cross assembler and a relocating linkage editor. The assembler will generate absolute or relocatable code and assemble std instruction mnemonics and directives. The linkage editor combines relocatable object code modules into an absolute load module. The package will run on any PDP-11 under RSX-11M or on any VAX under VMS in compatibility mode. The software package is priced at $3000; a software license agreement is required. **Mostek Corp, sub of United Technologies Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 295

Pascal cross assembler

The NSX16 Cross Software package includes a Pascal compiler, linker, assembler, target-system debugger, and librarian. The ASM16 Cross Assembler package includes all NSX16 components, except the Pascal compiler. This software is designed to run on CP/M 2.2 operating systems and can be used to create, link, and run Pascal or NS16000 assembler programs on NS16000 based systems. Once generated, the code is downloaded via a serial port to the development board for execution and debugging. The cross assembler supports macroinstructions and directly generates files. The NSX16 is priced at $1500; the ASM16 is $1000. **Solutionware Corp,** 1283 Mountain View-Alviso Rd, Sunnyvale, CA 94086.
Circle 296

Microfloppy system

The MicroDOS operating system, the CDP18S845 is designed for microfloppies. The system provides program construction, storage, editing, assembly, and program checkout while supporting 4 microfloppy drives. Supporting MicroDOS is a monitor program that allows users to examine and alter memory and begin programs at selected locations. File management software provides rapid access to programs and supports file name structure for dynamic allocation of file space. It contains a translation program to convert files from 8″ to 3½″ format. MicroDOS is $300; the monitor program is $49. **RCA Microsystems,** Box 3200, Somerville, NJ 08876.
Circle 297

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

Right angle connectors

A line of molded cable assemblies with right angle DIN connectors is available for keyboard or I/O applications. The assembly interconnects analog and digital signals in computers, test equipment, and control devices. The fully molded male connector has a strain relief, high dielectric insulation, positive polarized mating, and friction retention. Available with 3, 5, 6, 7, and 8 pins, the plug can be molded onto unshielded or shielded cables of any practical length. **Belden,** 2000 S Batavia Ave, Geneva, IL 60134.
Circle 298

Connector and flat cable system

The CW "D" flat/cable connector system is an emi/rfi shielded D-subminiature connector. The flat cable is in response to the requirements of FCC docket 20780, part 15. It uses a metal mounting flange and a tin-plated steel shield to enclose the IDC connector. It can be used to terminate cable ends or in a daisy chain configuration. Its unique snap-together shield design eliminates the need for screws, and teeth provide a strain relief grip on the cable jacket. The connector can be supplied fully assembled to the jacketed cable or as a separate component. It is available in 25-conductor pin or socket contacts. **CW Industries,** 130 James Way, Southampton, PA 18966.
Circle 299

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

INTEGRATED CIRCUITS

Ethernet code converter

The CMOS 8002 Manchester Code Converter (MCC) provides data encoding and decoding functions for the Ethernet network. The 5-V MCC is compatible with Ethernet transceivers and IEEE 802.3 CSMA/CD std. The chip has 2 portions: the transmitter uses encoding to combine clock and data into a serial stream; the receiver detects data frames and collisions while recovering encoded data. Filtered data are processed with transition width asymmetry of 12 ns to −12 ns within a worst-case 12-bit cell time. Incoming data are sampled within an 18-ns to −18-ns width. In a 20-pin cerDIP, the 8002 MCC is priced at $22.50 in 100-unit quantities. **Seeq Technology, Inc,** 1849 Fortune Dr, San Jose, CA 95131.
Circle 300

Logic circuits

Designed to replace Schottky TTL, the 74F series offers 7 logic circuits including 2 gates, 2 flipflops, demultiplexer, quad multiplexer, and a shift register. The circuits are available in 14- or 16-pin DIPS for the 0 to 70 °C commercial temp range. Series 54F military temp range versions (−55° to 125 °C) in ceramic packages will be offered in 1984. Prices in the 100 to 999 unit range from $0.56 for a 3.5-ns triple nand gate to $1.62 for a 150-MHz shift register. **Signetics Corp,** 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086.
Circle 301

CMOS EPROMs

Available in CMOS, the HN27C64 is an 8K x 8 EPROM. The 64K-byte device has 30 mA max active current at 5 MHz and 100 μA max at standby. Packaged in a std JEDEC B-type 28-pin DIP, it has a transparent lid to erase memory contents with ultraviolet light. The EPROM is pin and function compatible with industry std 2764. It will be offered in 3 different speeds: 200 ns, 250 ns, and 300 ns. In 100-piece quantities, the -20 is $54.70; the -25 is $42.50; the -30 is $37.20. **Hitachi America, Ltd, c/o Hitachi Information Services,** 22 E 49th St, New York, NY 10017.
Circle 302

ROM/EEPROM combination

A combination of ROM and EEPROM memory on a single chip is available as the MCM6836 (CREEM) chip. Offering 14K bytes of mask ROM and 2K bytes of EEPROM, the memory is delivered in a single 28-pin package. Two versions are available; the MCM6836R16 offers an option that allows the user to substitute 256 bytes of relocatable memory anywhere in the 16K-byte memory map; the MCM6836E16 offers 250-ns access time with an active current draw of 100 mA and a 25-mA standby current. Pricing for the MCM6836R16 in 1k quantities is $29.50, $24.50 for the MCM6836E16. **Motorola Inc, MOS Microprocessor Div,** 3501 Ed Bluestein Blvd, Austin TX 78721.
Circle 303

Data separator for disk drive

A data separator IC for disk memory systems, the DP8460 includes PLL with onboard VCO, MFM decoder, and missing clock detector. Chip data rates allow up to 25M bps with accurate data window positioning of ⩽ 3.2 ns at a 5M-bps rate, and a power dissipation of 300 mW from a 5-V supply. Design provides read data synchronization and separation in a 24-pin skinny-DIP IC. Pricing in plastic is $25.75 per unit in quantities of 100. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 304

High speed CMOS driver

A monolithic CMOS quad driver, the D469 interfaces low-level outputs from logic circuits with high current, high voltage switching transistors. Four sets of complementary inputs are TTL compatible. Each output can drive a 500-pF load with less than 25-ns transitions. Internal logic circuits eliminate the possibility of shorting 2 devices directly across the power supply to ground. Available with 14-pin cerDIP or plastic DIP options, the driver operates from a single 12-V supply. The 100-piece price is $2.92. **Siliconix, Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054.
Circle 305

CRT driver

A linear IC can directly drive the cathode of CRT displays in data display monitors. The circuit uses proprietary implanted junction bipolar technology for a 200-V drive capacity. It features exceptional slew rate and low power dissipation specs. The circuit is constructed using std diffusion technology rather than the complex dielectrically isolated process formerly required for ICs with high voltage capability. It is packaged in a 20-pin DIP and will be available in the 4th quarter of this year. **SGS Semiconductor Corp,** 1000 East Bell Rd, Phoenix, AZ 85022. **Circle 306**

High throughput comm controller

A multiprotocol communication controller, the R68561 is designed to support circuits for the 68000 16-bit family. It has serial data rates of up to 4M bps and a 16-bit data space. The controller supports sync (in either ASCII or EBCDIC), bit oriented (SDLC/HDLC), async, and isochronous protocols. The device is compatible with Z80, 8080, and Multibus. It has 24 directly addressable registers for status reporting and rapid data transfer. The controller supports the 16-bit 68000 bus in a 48-pin device and is priced at $36 in 1k quantities. **Rockwell International, Electronic Devices Div**, 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.
Circle 307

Telecom switch IC

The MT8981 is a telecommunications IC for switching PCM encoded voice and/or data. Microprocessor controlled, the device offers a nonblocking matrix, 128 x 128 channels running at 64K bps. The chip can either switch 4 serial input streams of 32 channels to 4 output streams or an 8-bit word on any input channel to any output channel. The device outputs can be 3 stated on a per channel or all channel basis. With applications in compressed voice, data, and image systems, the device sells for $48 for 100 and up, in a 40-pin cerDIP. **Mitel Semiconductor**, PO Box 1663, Buffalo, NY 14203.
Circle 308

Clock driver chip

The Z8581 clock generator and controller provides the ability to stretch both phases of the clock signal using external control. The chip uses 2 independent crystal-controlled 20-MHz oscillators to generate a TTL-compatible or MOS-compatible clock signal at source frequencies. Featured is a system reset output that is synched with the clock output. It generates a CPU reset pulse for a minimum of 30 ms. External input can be used to initiate system reset. The 18-pin slimline DIP is priced at $7.00 in 1000-unit quantities. **Zilog, Inc**, 1315 Dell Ave, Campbell, CA 95008.
Circle 309

Parallel FIFO

The MK4501 is a 512 x 9 bit dual-port FIFO memory component. Expansion capability is unlimited because word length and depth can be increased by adding FIFOs. Reads and writes are internally sequential so that no address information is required. The main application of the FIFO is as a rate buffer, sourcing and absorbing data at different rates. Data transfer problems are solved by providing async connection without arbitration. A full and empty flag and 2-port cell arrangement permit simultaneous R/W statements. The FIFO is available with access speeds of 120, 150, and 200 ns; prices range from $28.50 to $31.50 in 100-piece quantities. **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 310

EPROM with 150-ns access time

The AM2732A ultraviolet-light EPROM features access times as low as 150 ns. Organized as 4096 x 8, it allows operation with high speed microprocessors without any wait states. To eliminate bus contention in multiple-bus microprocessor systems, the device has separate output-enable and chip-enable controls. It uses a single 5-V supply with a power dissipation of 525 mW active and 130 mW standby. The 32K-byte EPROM has TTL-compatible inputs and 3-state outputs and can be programmed by either single-bit location, in single blocks, or at random. The chip is priced at $17.80 in 100s. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 311

Cache memory comparator

An 8-bit cache-address comparator, the TMS2150 allows large low cost dynamic memory to perform like high speed RAM. The device performs address-matching functions, reduces tag-memory implementation cost and complexity, and provides label comparison times equivalent to TTL and ECL implementations. Comparator is available in 4 delay versions: 45, 55, 70, and 90 ns. It is also adaptable to wider tag addresses or deeper tag memories. Operating from a single 5-V supply, the 24-pin cerDIP is available in 100-piece quantities for $18.28 (70 ns) and $23.75 (45 ns). **Texas Instruments Inc, Semiconductor Group**, PO Box 401560, Dallas, TX 75240. **Circle 312**

Mini array processor

The AP-4, a mini array processor, offers 16-bit, fixed point processing at speeds up to 12 x 10^6 operations/s. The board's avg power consumption is 22 W with a single 5-V supply. Processor uses 12 single-word instructions for operation and self-test and all algorithms are resident in onboard PROM. Specific applications include FFT processing of up to 1024 points and digital filtering with a 50-kHz realtime bandwidth. The AP-4 is priced at $3800. **DSP Systems Corp,** 1081 N Shepard St, Anaheim, CA 92806.
Circle 313

Fast supermini

Designed with VLSI technology, the Hawk/32 is a 32-bit supermini. The computer system includes distributed processors, an 8M-byte memory subsystem, and an I/O interface subsystem. The CPU executes instructions at an avg 2.5 MIPS; on the Whetstone benchmark it has 1300k WETS/s. It handles data rate requirements with a 14M-byte/s I/O channel bandwidth to main memory. The supermini is compatible with the full ROLM line of 16- and 32-bit military Eclipse® computer systems, and uses the AOS/VS operating software. In a std configuration the system will sell for $190,000. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 314

VLSI design package

An integrated CAE/CAD IC design package can translate schematics into custom VLSI circuits. The Cell Compiler library verifies interconnection and function of the physical layout to the schematic diagram. Also included are the schematic editor (for design synthesis, network entry, and documentation) and a logic/timing simulator (for verification). A composition editor allows building of a chip by interactively placing the configured cells where needed; the editor also permits automatic routing of cells. The complete design system will be available during the third quarter of this year. **VLSI Technology, Inc,** 1101 McKay Dr, San Jose, CA 95131. **Circle 315**

TEST & MEASUREMENT

Benchtop memory tester

The 1734M memory test system is a benchtop system designed to test memory chips at incoming inspections. It tests all popular static and dynamic RAMs, up to 256K bytes, as well as PROMs and EPROMs. The unit consists of 3 micros for test calculations, handling of tape storage and formatting, and functional testing. Page mode programming as an interactive data entry mode eliminates the need for programming languages. MicroCode programming allows the user to create custom test patterns, vary supply voltages, or change address and data limits. Prices for the 1734M begin at $55,000. **GenRad, Inc,** 170 Tracer Lane, Waltham, MA 02254.
Circle 316

Memory tester

The J386A memory test system is designed for high volume production testing. It can test 4 DRAMs in parallel, and up to 256K bytes of dynamic and static RAMs and ROMs. The system's Pascal-T software is compatible with other members of the memory test family. The operating program tests in any of 3 modes for quad-, dual-, and single-site testing of bit- and byte-wide RAMs and ROMs. By taking over the housekeeping details, the software allows the user to focus on device testing. The test system is priced at $170,000. **Teradyne, Inc,** 535 Morrissey Blvd, Boston, MA 02125.

Circle 317

Identification system

A microcomputer based multivision system, the VIEW 1101 stores complex details of parts and makes identification at any angle through 360°. It can search a part in 300 ms, which is the time required to compare a live video image with a stored reference. The device gives a part's location and determines its angle of orientation with a 0.2° accuracy. An optional gate processor board enables measurements to be made without fixturing. The system has applications in routing, sorting, robotics, and inspection. Prices range from $20,000 to $70,000, depending on configuration. **View Engineering,** 1650 N Voyager Ave, Simi Valley, CA 93063.
Circle 318

Measure and control system

The Station 10 is an industrial control station for plant floor environments. It uses Macsym 10, a PROM based system for reliable operation of mass storage devices. Integrated into the device are a 16-bit computer based measurement and control system, a touch-sensitive gas plasma operator interface, and a 40-col impact printer. Programmable in BASIC, the Station 10 has 30 A-D I/O cards, 96K bytes of RAM, and a PROM board that stores the operating system. The base system price is $19,900. **Analog Devices Inc,** 3 Technology Way, Norwood, MA 02062.
Circle 319

Data acquisition micro

A combination of A-D hardware on a single STD bus and std software supplied in source code, the Labtech 70 microcomputer achieves data acquisition speeds as high as 650 kHz. Using the precompiled, menu-driven Take-Data software allows the user to acquire data without programming. Alternatively, users can write their own programs in FORTRAN 77, Pascal, C, assembler, or BASIC. Because of hardware clocking and elimination of processor involvement, multiple boards can be added for simultaneous readings on multiple channels. **Laboratory Technologies Corp,** 328 Broadway, Cambridge, MA 02139.
Circle 320

INTERFACE

Controller establishes IEEE 488 bus

The 4835 bus controller makes the RS-232 or RS-422 serial data port appear and function as an IEEE 488 bus controller. Software control of the bus resides in the central computer and is transparent. Each user has access to the speed, information storage facilities, data base, and peripherals of the central computer. The 4835 has an independent architecture, operating system, and language. The controller can set up the bus up to 50′ away on RS-232 links or up to 4000′ away on RS-422 links. The controller costs $1450. **ICS Electronics Corp,** 1620 Zanker Rd, San Jose, CA 95112.
Circle 321

Q-bus repeater

A bus repeater, model 1953 is designed for transparent multibackplane Q-bus operation. Without using linking software or multiprocessor topography, the repeater reaches up to 21 slave units and up to 463 dual-height cards. It supports Q-bus memory parity plus block mode DMA at up to 2M words/s and bus parity for both data and control signals. The 1953 supports all modes of addressing including 16, 18, and 22 bits and 4 interrupt levels. It has high noise immunity, controlled rise times, and onboard arbitration for both DMA and interrupt levels. **ADAC Corp,** 70 Tower Office Park, Woburn, MA 01801. **Circle 322**

MUX interface

The self-contained PR-1100 MUX can interface up to 4 SMD disk drives with a single controller. The MUX features auto-response to the selected drive, eliminating the need for operator intervention. Additionally, the device has LED output connector lights to indicate selected drive and an IND/SCTR toggle switch for selection of either index or sector pulses. Included in the MUX are a power supply, logic for 4 drives, 26-pin SMD interface connector, and four 26-pin SMD output connectors. Single-quantity price is $1000. **Pioneer Research Inc,** 1745 Berkeley St, Santa Monica, CA 90404. **Circle 323**

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

Double-sided 3½" disk drive

An enhanced version of the 3½" microfloppy disk drive is available. It is capable of storing 1M byte of data in double-density mode. The drive is approx one-quarter the size and one-half the weight of conventional 5¼" drives and uses 50% less power. The disk is encased in a semirigid cartridge-type housing for easy use and damage protection. Format specs for the 3½" floppy disk are mutually compatible with 13 leading disk drive and media manufacturers. The 80-track disk drives will be available in the third quarter of this year. **Sony Corp, Data Products,** Sony Dr, Park Ridge, NJ 07656. **Circle 324**

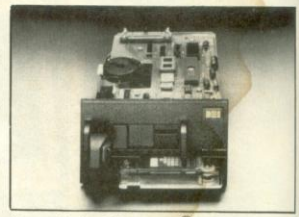
Single-board memory

The CI-796 EDC is a 128K- x 9- to 2M- x 9-byte Multibus/IEEE 796 compatible memory board. Features include double-bit error detection and single-bit error correction. Worst case access and cycle times are 270 and 425 ns, respectively (during error correcting read cycle). Three refresh options are available: internal refresh, external refresh, and external refresh with override. Memory protect logic and battery backup busing allow user to operate in battery backup mode. A control status register gives location of any failing RAM. Prices range from $1195 to $6495. **Chrislin Industries, Inc, Computer Products Div,** 31352 Via Colinas, Suite 102, Westlake Village, CA 91361. **Circle 325**

IBM PC disk subsystem

The Targa II is a hard disk subsystem for the IBM PC, available in 3 models. The first is a single-drive machine with 3 formatted storage capacities of 5M, 10M, or 15M bytes. The second provides a slot to allow the addition of a second drive. The third offers room for 5 extra IBM expansion cards. Targa II matches the IBM PC in color, shape, and design. The units begin at $1490 for the Model 1 with a 5M-byte capacity and go up to $2445 for the Model 3 with 15M bytes. **CMC International,** 1720-130th Ave NE, Bellevue, WA 98005.
Circle 326

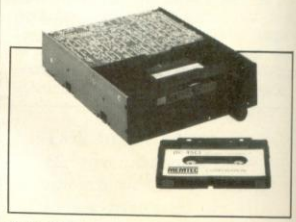
Streaming and start/stop drives



Part of the Microtape® series, the EL family consists of ¼" digital cartridge tape drives. They fit the std 5¼" footprint and feature end loading of the cartridge. The EL-1 (streaming) has a 13.3M-byte formatted capacity and applications as a mirror-image backup for Winchesters. The EL-5 and EL-6 (start/stop) have 21.3M-byte capacities and file update and reorganization functions. The EL-5 is media and interface compatible with the Funnel high density tape drive, while the EL-6 uses serpentine recording. Prices in 1k quantities range from $450 to about $700. **Data Electronics, Inc,** 10150 Sorrento Valley Rd, San Diego, CA 92121.
Circle 327

Compact Winchester backup

A miniature reel-to-reel tape drive backup, the Companion Model 440 has a 40M-byte capacity. It fits the same half high form factor as 5¼" Winchester and minifloppy drives. With synchronized twin motors and electronic control of tape tension, the system raises the bit-error ratio to 10^{10}. The MTBF is 7k h; 40M bytes can be backed up in 9 min on 9-track tape. The system is compatible with std interfaces (SASI and QIC II) and its read-after-write capability allows for data comparison and improved data recovery. Unit prices begin at $350 for OEM quantities. **Memtec Corp,** Keewaydin Dr, Salem, NH 03079.



Circle 328

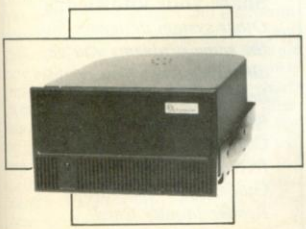
Half-height 10M-byte Winchester

The HH-612 is a 5¼″ Winchester disk drive. The half-height drive has a 10M-byte capacity and is suited for integration with small business and personal computers. Device measures 1.63″ x 5.75″ x 8″ (4.14 x 14.60 x 20 cm), weighs 30 lb (1.4 kg), and requires 0.9 A of direct current. The HH-612 features technologies associated with 14″ drives including plated media, microprocessor-controlled closed-loop servo positioning and spindle motor speed, guard bands, and onboard diagnostics. Single-unit price is $999; quantities of 2500 to 4999 are priced at $580 per unit. **Microscience International Corp,** 575 E Middlefield Rd, Mountain View, CA 94043.

Circle 329

5¼″ drives

D-700 series 5¼″ Winchesters have capacities of 26.9M, 44.9M, and 62.7M bytes (unformatted). Data are carried on 2, 3, or 4 thin film plated fixed disks with a surface reserved for track following servo information. A landing/shipping zone protects against data errors and loss. All 3 models have a 35-ms access time and a heat dissipation of 20 W. The Winchesters have std 5¼″ minifloppy form factor and use 5/12-V dc voltages and std ST412 interfacing. In small OEM quantities, prices range from $745 to $990. **Disctron, Inc, sub of CCT,** 1701 McCarthy Blvd, Milpitas, CA 95035.



Circle 330

Fast Winchester subsystems

A Winchester disk subsystem, model 6236 has a 354M-byte capacity. Model 6237 offers users over 1.06G bytes of storage with a peripheral package that includes three 354M-byte drives and 1 intelligent controller. For high reliability, the drive has few moving parts, a closed-loop air system, and a dedicated landing zone to maximize data integrity. The disk performs with a 5-ms seek time; avg seek time is 20 ms. Full stroke time is 35 ms and disk rotation is 3000 rpm with an avg rotational latency of 10 ms. The disk is formatted into 512 bytes/sector and 56 sectors/track. **Data General Corp, Information Systems Div,** 4400 Computer Dr, Westboro, MA 01581.

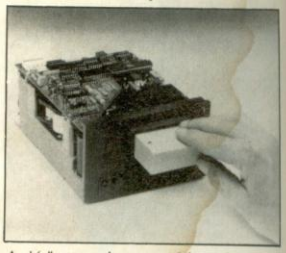
Circle 331

Winchester subsystem

A memory subsystem, the model HD-20 consists of a 21M-byte (unformatted) Winchester disk drive and the WDI-II hard disk interface card. The drive has a stepper motor design that permits slewing from track to track. It has a sealed chamber for the media and R/W heads. The heads are designed to fly above the surface of the spinning disk for higher recording density. The WDI-II interface card provides the interface between an S-100 bus computer system and the drive. It also allows high speed memory-to-memory data transfers. The price of the drive is $3995 with a 1-yr warranty. **Cromemco, Inc,** 280 Bernardo Ave, PO Box 7400, Mountain View, CA 94039.

Circle 332

Tape drive backup



A ½" streaming tape drive, the TM951 has a storage capacity of 50M bytes. Compatible with std 5¼" flexible and Winchester drives, the device provides an affordable backup for computers with high capacity drives. Using a video-style single reel of ½" std computer tape, the drive has a serpentine recording format on 20 tracks. Track density is 48 tpi, recording density is 6.4k bpi, recording speed is 40 ips, and data transfer rate is 250k bps. OEM prices range from $500 to $700. **Tandon Corp,** 20320 Prairie St, Chatsworth, CA 91311.

Circle 333

Add-in memory board

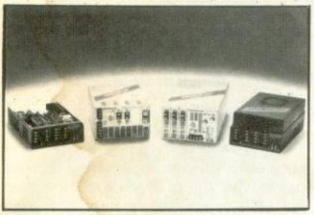
The DR-240 is a 1M-byte add-in board for the NOVA 4 and Eclipse S/140 minicomputers. Std word length is 22 bits (16 data and 6 ECC). The 6 ECC bits allow single-bit error correction and double-bit error detection. For error-sniffing operations, unused memory locations are refreshed and single-bit errors are corrected. Features include a starting address set in 32K-byte increments throughout the entire address range, a 400-ns R/W cycle time, and a refresh interval of 15.2 μs. Single-unit pricing ranges from $1315 to $5385 for capacities from 128K to 1M byte. **Dataram Corp,** Princeton Rd, Cranbury, NJ 08512.

Circle 334

Share your knowledge

Other system designers face the same problems you've already solved. You could help them by writing a technical article for Computer Design. For a free copy of our Author's Guide, circle **503** *on the Reader Inquiry Card.*

Expanded power supply series



The MultiMod series of power supplies has expanded with a 2-V, 50-A auxiliary module. The high current module plugs into the 600-W 6JA and 6JB power packages and the 1000-W 6M power package. A modular approach using a selection of power packages and std plug-in output modules provides voltage/current outputs for specific requirements. The MultiMod is available in 300-, 400-, 600-, and 1000-W power packages. Two to 7 outputs using plug-in modules of 2, 5, 12, 15, 24, and 48 V are available depending on the selected model. **Powertec, Inc,** 20550 Nordhoff St, Chatsworth, CA 91311.

Circle 335

High current output regulator

A 5-V, 5-A regulator, the LT1003 is pin compatible with the 3-A LM123/323, but provides a higher current output. It features a guaranteed 2% output voltage tolerance at 25 °C, and under worst-case conditions the tolerance is within 4%. The devices will be used as oncard logic supply regulators designed into bench-top power supplies. Minimum input voltage required is 7.5 V and thermal resistance is 1.5 °C/W or less. The regulator, in a hermetic steel package, sells for $5.40 in quantities of 100. Meeting military specs, the device sells for $21.50 in 100s. **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle 336

Std line of switchers

A std line of switching power supplies has applications in mini and microcomputers, printers, disk drives, and modems. The power supplies feature line and load regulation, high efficiency, input surge current, and short circuit protection. With built-in emi/rfi filtering, the supplies are UL, CSA, and VDE approved or approvable. The std switching supply line has been tailored and customized to meet particular specs. **Zenith Radio Corp,** 1000 Milwaukee Ave, Glenview, IL 60025.

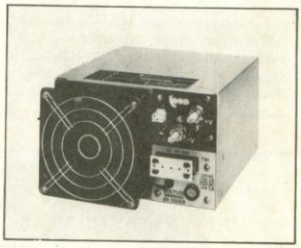
Circle 337

Cost-effective power supplies

The XL100 and XL125 are switching power supplies designed to meet the requirements in the 80- to 130-W range cost effectively. Both models feature input surge protection, 110/220 user selectable, overvoltage protection on 5-V output, and short circuit protection. The XL125 is available in 3 versions and includes an L bracket for heat sinking the power dissipated in 130-W applications. The XL100 is identical to the XL125 but it has no L bracket. Free standing, it will supply up to 100 W; attached to a chassis, it will supply up to 130 W. The 100-piece prices are $127 for the XL100 and $140 for the XL125. **Boschert Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.

Circle 338

Modular switchers



The basic SOX5-125 625-W switching power supply offers a choice of 7 output voltages from 2 to 28 Vdc. The supply delivers 5 Vdc at 125 A; other std voltages are 2, 3, 12, 24, 28, and 48 Vdc. Output voltages are floating and adj within ±10%. Line and load regulation is ±1% and ripple and noise are less than 10 mV rms, 50 mV peak to peak. Protection features include overvoltage, auto-resetting thermal, and current-limiting overload. Choice of input line voltage is 90 to 132 V or 180 to 264 V, 47 to 63 Hz. Supplies are priced at $374 in quantities over 1000. **Todd Products Corp,** 50 Emjay Blvd, Brentwood, NY 11717. **Circle 339**

Power conditioning systems

A line of power systems designed to safeguard computer equipment and data from damage are ac output rated at 120, 208, or 240 V, depending on the model. They neutralize voltage spikes up to 6000 V, lasting as little as 0.5μs, and eliminate current-transmitted irregularities. Noise rejection is rated at 120 dB common mode, and 60 dB transverse mode. Each model has multiple output receptacles that allow several computer devices to be plugged in at once. Prices range from $595 for a 1 kVA to $3150 for 7.5 kVA. **Data General Corp, Field Engineering Div,** 50 Maple St, Milford, MA 01757. **Circle 340**

Rackmounted power supplies

An expanding line of rackmounted power supplies offers output ratings from 3 Vdc/48 A to 28 Vdc/19 A. The 12 models have 19″ (48-cm) wide front panels sized for mounting in std racks, and are 3.5″ (8.9 cm) high and 17″ (43 cm) deep. Line and load regulation are each ±0.5% and ripple is 1 mV rms max. Std input is 105 to 125 Vac, 50 to 400 Hz; 210 to 250 Vac input is also available. Other options include metering, overvoltage protection, front panel voltage control, and handles. The price is $675. **Acopian Corp,** Easton, PA 18042. **Circle 341**

Power supplies

MRM series power supplies have been expanded for the office automation market. The multi-output, frameless style power supplies range in power from 43 to 75 W. They offer 3 to 4 stabilized dc outputs for the requirements of microcomputers, terminals, modems, and disk drives. One model offers 2 independent 12-V outputs for mass storage devices and CRTs. A special circuit minimizes the interaction of transient events on the output that drives the CRT display. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352.

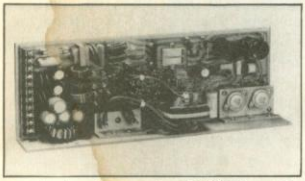
Circle 342

Dual-output converters

Two dc to dc converters, model MHE2812D (±12 Vo at ±625 mA) and model MHE2815D (±15 Vo at ±500 mA) are rated at 15 W. They are hermetically sealed in metal packages that are 2.1″ x 1.1″ x 0.5″ (5.3 x 2.8 x 1.2 cm). Thick-film hybrid construction provides a typ efficiency of 85% over the full input range of 16 to 32 Vdc. An optocoupler in the feedback loop provides electrical isolation between input and output. Features include short-circuit protection, internal input ripple filter, and shutdown capability. The price is $165 in 100-piece quantities. **Integrated Circuits Inc,** 13256 Northrup Way, Bellevue, WA 98005. **Circle 343**

September Preview—
Watch for a major staff-written review on printer technology.

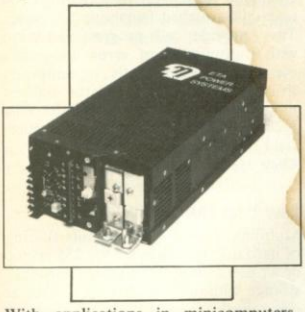
Worldwide power supplies



Q150 designates a series of 150-W, quad-output switchers. They are available in 4 models and in open or closed frame chassis. Q150 Cool 1 supplies have input ratings of 90 to 132 and 180 to 264 Vac, field selectable links, 47 to 440 Hz. The units offer a tightly regulated output and aux outputs can be quasi-regulated. Reliability features include 2 surge limiting varistors, 2 voltage clipping varistors, TO-3 hermetic switch transistors, and anti-saturation Baker clamps. Price of the units, in 1 to 9 pieces, is $290. **Deltron, Inc,** PO Box 1369, Wissahickon Ave, North Wales, PA 19454.

Circle 344

High current switchers



With applications in minicomputers, CAD/CAM systems, high speed ATE, and video image processing, 1500-W, 1- to 4-output switching power supplies are available. They have an 80% efficiency, with the hottest component not more than 35 °C above ambient. Features include instantaneous current limiting, SCR soft-started circuitry, and hybrid thermal design. The switchers operate on 180 to 264 or 90 to 132 Vac, and the outputs are rated from 2 to 48 Vdc up to 350 A. Prices range from $1090 for single-output to $1465 for 4-output. **ETA Power Systems,** 11602 Knott Ave, Bldg 12, Garden Grove, CA 92641.

Circle 345

EMI PROTECTION

RFI filters

The F2100 and F2200 international series filters feature IEC connectors for general purpose rfi control of line-to-ground noise. The filters are available in 1-, 3-, and 6-A models and meet low leakage current requirements of UL, CSA, VDE, and SEV. Rated voltage is 115/250 Vac, line frequency of 50/60 Hz max. Max operating ambient temp at rated current is 40 °C. Max leakage current each line to ground is 0.25 mA at 115 Vac, 60 Hz and 0.48 mA at 250 Vac, 60 Hz. **Curtis Industries, Inc,** 8000 W Tower Ave, Milwaukee, WI 53223.

Circle 346

DATA COMMUNICATIONS

Time division MUX

The UltraMux system is a 10M-bps time-division MUX that operates over 1.544M-bps T-1 digital lines. The MUX can mix voice, data, and video transmissions and accommodate any combination of std and non-std data rates. Features include channel routing and broadcast, reconfiguration capabilities, and diagnostics control. The MUX is compatible with Bell M12, MC2, and MIC MUX frames. The device can be monitored and diagnosed from anywhere in the network or from a terminal with communication abilities. A typ 16-channel system is priced at approx $16,000; a 64-channel system, approx $42,000. **Avanti Communications Corp,** Aquidneck Industrial Park, Newport, RI 02840.

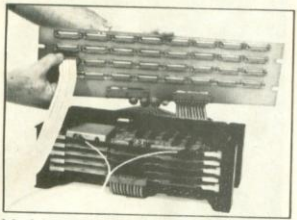
Circle 347

Printer and time server for LAN

The Omninet Utility Server functions as a network printer server and time server. It is capable of operating with printers that have data transfer rates of 9.6k baud. The server features an intelligent controller with a Z80 micro having 64K bytes of RAM and will automatically boot from a network disk. The server was designed for Omninet, a CSMA LAN. It operates over an end-to-end network up to 4000′, at a rate of 1M bps. The system lets users combine up to 64 micros with different operating systems on 1 network. The server is priced at $990. **Corvus Systems, Inc,** 2029 O'Toole Ave, San Jose, CA 95131.

Circle 348

Fiber optic MUX



Model FMX fiber optic MUX provides a tradeoff in flexibility, economy, performance, and reliability. For users requiring a large number of short-haul digital interconnects, the MUX provides 8 to 128 async digital channels. These channels are transmitted over a 2-fiber optic cable using time division multiplexing techniques. The fiber optic medium provides an emi-free path with an error rate of less than 1 in a billion for a distance of 2 km. The max bit rate is 125k bps for 8 channels to 9.6k bps for 128 channels. **Atlantic Scientific Corp,** 2711 S Harbour City Blvd, Melbourne, FL 32901.
Circle 349

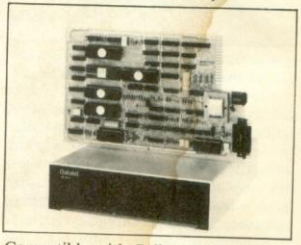
SNA protocol converter board

Interfacing up to 32 async communications lines to an IBM host, the MZ-68K is a Multibus compatible board based on the MC68000. The board uses SNA/SDLC protocol and, when combined with SNA firmware, adds SNA capability to any Multibus compatible device. These devices can include dumb ASCII terminals, LANS (such as Ethernet), and intelligent instrumentation. The converter board is priced at $2000; the firmware, called MZ-SNA, is priced at $1000. **Thomas Engineering Co,** 1040 Oak Grove Rd, Concord, CA 94518.
Circle 350

Small modem card

The OEM212A is a full-duplex async modem card offering custom applications ability due to its small size. The board measures 5.4″ x 8.8″ (13.7 x 22.4 cm). Operating speeds are 300 bps, or character async at 1.2k bps over phone lines. All commands including auto dial, auto log on, and options are controlled from the keyboard and stored in memory. The auto dialer can store up to 10 numbers of 60 chars each. A single keystroke displays stored numbers, automatically dials, and executes auto log-on sequences. The modem is compatible with Bell 212A, 103, and 113 modems. The price is $360. **Rixon Inc,** 2120 Industrial Parkway, Silver Spring, MD 20904.
Circle 351

Intelligent modem family



Compatible with Bell 103/113 and 212A, this family of auto-dial/auto-answer intelligent modems operates in 2-wire full-duplex mode. Dial selection information is passed to the modems via the RS-232-C interface in std ASCII format. Both versions are available in PCB form for rack-mounting. Each modem uses the same command format for direct connection to public-switched telephone networks. They provide call progress detection with transmission of error and result messages to a CRT, printer, or computer. Prices are under $300 for the 300-bps model and less than $500 for the 1.2k-bps model. **Databit Inc,** 110 Ricefield Lane, Hauppauge, NY 11788.
Circle 352

Low cost LAN

Multilink is a LAN that permits sharing of hard disk resources among 255 IBM PC or XT users. It provides shared hard disk storage without requiring hard disks at every workstation. Multiple file servers provide redundancy, flexibility, shared usage, and reduced cost. Based on ARCNET levels 1 and 2, the system is compatible with Xerox network systems protocols. The hardware uses token passing but high level protocols will be IEEE 802 compatible. Max distance between any 2 stations in the network is 20,000′ and max distance between hub and node, or between 2 active hubs, is 2000′. Data transfer is 2.5M bps with message sizes from 1 to 508 bytes. Interface card is $595 and connectors are $100 to $800. **Davong Systems,** 217 Humboldt, Sunnyvale, CA 94086.
Circle 353

CIRCLE 120

Stat MUX concentrators

Data Express/XL series data concentrators are available in 4-port (DE4/XL) and 8-port (DE8/XL) versions. Both stat MUXes feature full remote echoplex capabilities, ARQ error detection and correction, data buffering, and data flow control. The 4-port operates over sync or async networks up to 9.6k bps, while the 8-port operates at the same rate over sync networks. The DE4/XL allows an aggregate terminal input of 38.4k bps and is priced at $1850. The DE8/XL input is 76.8k bps and it is priced at $2650. **Compre Comm, Inc,** 3200 N Faber Dr, PO Box 3570, Champaign, IL 61821.
Circle 354

Modem chip

The TCM3101 modem is both Bell 202 and CCITT V.23 protocol compatible. The chip allows users to transmit data entered via buffered keyboard at the same time incoming data are received. In half-duplex mode, data rates are 1.2k bps; in full-duplex, data rates are 1.2k bps with a 150-bps transmission rate. Incorporating the modem into a device requires the use of a UART, a data-access arrangement, and a 2 to 4 wire converter. The 16-pin DIP sells for $21.34 each in 1000-piece quantities. **Texas Instruments, Inc, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.
Circle 355

Low cost network processor

The system 335 processor is based on an integrated architecture that allows interactive networks to grow in size and performance. It provides data communication capability for small to medium networks. The system drives series 100 or 200 stat MUXes. It also drives an X.25 gateway interface into a packet mode or public data network, or allows connections to another system 335. Std features include subnetting, port contention capability, host selection, and trunk link multidrop MUXing. **Digital Communications Associates, Inc,** 303 Technology Park, Norcross, GA 30092.
Circle 356

Data comm systems

The Series 1 is a family of data communications systems with a wide range of configurations. These vary from single CPU memory-only to multi-user/multi-processing disk based systems. The general purpose processor is a 32-bit CPU based on the 68000 with 4M bytes of memory. Channel control and data communications traffic is handled by the telecommunications processor, which contains control logic to support 1024 full-duplex channels. Std software packages include TRAX, a multiprocessing executive; COMEX, a virtual circuit manager; and a support library. For typ configurations, prices range from $29,500 to $93,000. **Telematics International, Inc,** Crown Center, 1415 NW 62nd St, Fort Lauderdale, FL 33309.
Circle 357

IBM PC compatible modem

The ModemCard 300 and the ModemCard 1200 are plug-in modems for the IBM PC. Model 300 runs at 300 baud and can be upgraded to 1200 baud with a piggyback adapter card. Model 1200 runs at 1200 baud and can be switched to 300-baud mode. Both are direct-connect, auto-dial/auto-answer and include a terminal program. They are Bell 103- and 212A-compatible for full-duplex operation at either baud rate. The modems support touch tone or pulse dialing, auto-dial tone sensing, call progress detection, auto-redial, and audio monitoring. The modems come with message oriented software. **SSM Microcomputer Products, Inc,** 2190 Paragon Dr, San Jose, CA 95131. **Circle 358**

Modem board

The Core is a programmable auto dial/auto answer modem. Designed for OEMs, the modem is made to fit available space within a terminal or computer shell. The system consists of a modulator/demodulator unit that provides 300 to 1200 baud and a phone line interface. Options include a phone line monitor system, self-contained power supply, and RS-232 or TTL interfaces. User interface features include manual original and answer modes, a DTR override, phone line adjustments, and LEDs. **U.S. Robotics Inc,** 1123 W Washington Blvd, Chicago, IL 60607.
Circle 359

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CONFERENCES

SEPT 12-14—IEEE Internat'l Conf on Computer Aided Design, Santa Clara, Calif. INFORMATION: John A. Domiter, American Bell Inc, PO Box 3505, New Brunswick, NJ 08903

SEPT 13-15—Autofact Europe, Palexpo Conf and Exhibition Ctr, Geneva, Switzerland. INFORMATION: Automated Systems Assoc, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

SEPT 13-15—Federal Computer Conf, Washington Conv Ctr, Washington, DC. INFORMATION: Federal Education Programs, PO Box 368, Wayland, MA 01778. Tel: 617/358-5181; 800/225-5926 (outside Mass)

SEPT 13-15—Midcon, O'Hare Expo Ctr and Hyatt Regency O'Hare, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Mini/Micro-Midwest, O'Hare Expo Ctr, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Peripherals, Moscone Ctr, San Francisco, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, 1350 E Touhy Ave, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311

SEPT 13-15—WPOE (Word Processing and Office Environment Show and Conf), San Jose Conv Ctr, San Jose, Calif. INFORMATION: Cartlidge & Assocs, Inc, 4030 Moorpark Ave, Suite 205, San Jose, CA 95117. Tel: 408/554-6644

SEPT 19-21—Advanced Control Conf, Purdue Univ, West Lafayette, Ind. INFORMATION: Henry Morris, Control Engineering, 1301 S Grove Ave, PO Box 1030, Barrington, IL 60010. Tel: 312/381-1840

SEPT 19-23—IFIP (Internat'l Federation for Information Processing) World Computer Congress, Paris, France. INFORMATION: Philip H. Dorn, Dorn Computer Consultants, Inc, 25 E 86th St, New York, NY 10028. Tel: 212/427-7460

SEPT 20-22—Informatics Exhibition and Conf, Roberto Clemente Coliseum, San Juan, Puerto Rico. INFORMATION: Informatics '83, 3421 M St NW, Suite 219, Washington, DC 20007. Tel: 703/920-9595

SEPT 26-29—Compcon Fall, Marriott Gateway, Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 26-28—Maecon, Kansas City Conv Ctr, Kansas City, Mo. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 29-30—CAD/CAM and Simulation Conf, Westin Hotel, Boston, Mass. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 619/459-3888

SEPT 29-OCT 1—CP/M East, Hynes Auditorium, Boston, Mass. INFORMATION: Northeast Expositions Inc, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/841-7000 (outside Mass)

OCT 2-5—Robotech (Internat'l Conf and Exposition for the Application of Automated Manufacturing Technology), Curtis Hixon Convention Hall, Tampa, Fla. INFORMATION: Tom Will, Latcom Inc, 4135 Laguna, Coral Gables, FL 33146. Tel: 305/667-5150

OCT 3-6—Data Communications Symposium, Sea Crest Lodge, Falmouth, Mass. INFORMATION: Kenneth J. Thurber, Architecture Technology Corp, PO Box 24344, Minneapolis, MN 55424. Tel: 612/935-2035

OCT 8-10—PC (Internat'l Exposition and Conf Featuring IBM Personal Computers and Compatibles), Bayside Exposition Ctr, Boston, Mass. INFORMATION: Northeast Expositions, Inc, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/841-7000 (outside Mass)

OCT 10-13—ISA (Instrument Society of America) Internat'l Conf and Exhibit, Astrohall, Houston, Tex. INFORMATION: Philip Meade, ISA, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.

OCT 12-14—Fiber Optic Communications Local Area Network Applications, Atlantic City, NJ. INFORMATION: Tom Coggeshall, IGI, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022

OCT 18-20—Internat'l Test Conf, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Doris Thomas, PO Box 371, Cedar Knolls, NJ 07927. Tel: 201/267-7120

OCT 24-26—IEEE Internat'l Symposium on Electromagnetic Compatibility, Shoreham Dunfey Hotel, Washington, DC. INFORMATION: IEEE EMC '83, PO Box 2228, Rockville, MD 20852. Tel: 301/984-8400; 800/638-0111 (outside Md)

OCT 31-NOV 3—Internat'l Conf on Computer Design: VLSI in Computers, Rye Town Hilton, Port Chester, NY. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

NOV 1-3—Federal Office Automation Conf, Washington Convention Ctr, Washington, DC. INFORMATION: Nat'l Council for Education on Information Strategies, PO Box N, Wayland, MA 01778. Tel: 617/358-5356; 800/343-6944 (outside Mass)

NOV 7-11—IECON (IEEE Conf on Industrial Applications of Mini and Microcomputers), Hyatt Regency, San Francisco, Calif. INFORMATION: Patrick P. Fasang, Siemens Corp, 105 College Rd E, Princeton, NJ 08540. Tel: 609/452-7070

NOV 8-11—Mini/Micro-West, Brooks Hall, San Francisco, Calif. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

NOV 8-11—Wescon, Moscone Ctr and Civic Auditorium, San Francisco, Calif. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

NOV 14-16—Connectors and Interconnections Technology Symposium, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 215/279-7084

NOV 14-17—Autofact 5 Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: CASA/SME Public Relations, PO Box 930, Dearborn, MI 48128. Tel: 313/271-0777

Switch catalog
A pictorial index and guides for switch selection, illumination, and accessories complement technical specs of miniature, illuminated, nonilluminated, oil- and water-tight, key lock, and push-button switches. **EAO Switch,** Milford, Conn.
Circle 410

Industrial S/R-D converters
Low-cost SDC-19100 Monobrid® series is detailed in data sheets that contain technical information for 10-, 12-, and 14-bit models, along with block diagram, figures, mechanical outline, and photo. **ILC Data Device Corp,** Bohemia, NY.
Circle 411

Metal-gate CMOS array
Brochure examines HI-3000, summarizing basic cell characteristics, absolute maximum voltage ratings, and package compatibility; component list and complete electrical characteristics for T_A at 25 °C are tabulated. **Holt, Inc,** Irvine, Calif.
Circle 412

Membrane keyboards
Brochure covers standard matrices and specs, showing cross-sectional and dimensional diagrams; charts cross-reference pin configuration and size with part number. **SMK Electronics Corp,** Placentia, Calif.
Circle 413

Thermal line printers
Literature describes high-speed 2″, 4″, and 8″ wide units with full character line. **KSC Electronics, Inc,** Arlington Heights, Ill.
Circle 414

Stock membrane switches
Catalog specifies 5/8″, 3/4″, 1″, and 1¼″ center-to-center switches, including dimensional drawings and a custom faceplate design guide; materials, production test methods, and termination schedules are tabulated. **W. H. Brady Co, Xymox Div,** Milwaukee, Wis.
Circle 415

Brushless synchros
Technical bulletin gives electrical, mechanical, and performance specs for 24 models; various sizes, speeds, and electrical configurations are described through outline drawings and schematics. **Harowe Servo Controls, Inc,** West Chester, Pa.
Circle 416

Chip capacitors and inductors
Brochure describes MLC leadless ceramic chip capacitors and inductors/transformers, presenting technical characteristics, voltage/temperature parameters, and aging/voltage effects. **SFE Technologies,** San Fernando, Calif.
Circle 417

Data communication products
Brochure profiles capabilities of fiber optic cables, copper cables, interconnecting hardware, and fiber optic integration services. **Siecor Corp,** Hickory, NC.
Circle 418

Disk drives
Memory product foldout gives short descriptions of cartridge drives and examines automation procedures. **Vermont Research Corp,** North Springfield, Vt.
Circle 419

Shielding emi
Guide outlines characteristics, sources, and ramifications of interference. **Tecknit,** Cranford, NJ.
Circle 420

Real-world interface
Brochure presents methods for interfacing sensors, transducers, output actuators, and digital I/O, and profiles key selection criteria for different methods. **Analog Devices,** Norwood, Mass.
Circle 421

Wire and cable
Specs and diagrams complement descriptions of stripping, cutting, twisting, tinning, marking, and braiding a range of electronic wire and cable, **Mil Spec Supply, Inc,** Chatsworth, Calif.
Circle 422

Optical data transmission
Tutorial presents basic theory and system considerations in transmitting electronic analog and digital data across optical fiber, along with application examples for several forms of data acquisition, transmission, and linking; design specs for FO Datalink family are included. **Dynamic Measurements Corp,** Winchester, Mass.
Circle 423

Digital multiplexers
Brochure covers TDM-150 series; voice, data, and program channels are described with application diagrams. **Tau-tron Inc,** Chelmsford, Mass.
Circle 424

Graphics systems software
Product guide features independently written applications packages that are compatible with Ramtek graphics and imaging display systems, listing cost, language, distributor, and availability for each package. **Ramtek Corp,** Santa Clara, Calif.
Circle 425

Concentrator switch
Brochure examines the Micro 860 switch, showing its operation, network management capabilities, and troubleshooting features through text and line drawings. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 426

Instrumentation modules
Photos, block diagrams, and specs depict Voltsensors, Bridgesensors, Linesensors, and I-supplies in this catalog of instrumentation op amps, modular power supplies, and packaging hardware. **Calex Mfg Co, Inc,** Pleasant Hill, Calif.
Circle 427

Microprocessor family in CMOS
Overall view of the 16-bit CMOS 80C86 microprocessor family is accompanied by product briefs of other industry standard devices and descriptions of future products. **Harris Corp, CMOS Digital Products Div,** Melbourne, Fla.
Circle 428

Push buttons and indicator lights
Heavy-duty 22- and 30-mm diameter models are shown in brochure featuring exploded mounting diagrams, unit construction system, and control station; accessories, technical data, and dimensional diagrams provide thorough reference. **Klockner-Moeller,** Natick, Mass.
Circle 429

Industrial meters
Booklet outlines features and specs of illuminance, luminance, incident, reflectance, and TV color-analyzer meters; charts and graphs complement text. **Minolta Corp,** Ramsey, NJ.
Circle 430

Color graphics terminals
Folder discusses how color graphics can enhance data comprehension, and explains how DEC's VT100® monochrome terminals can be converted to high performance color graphics stations. **ID Systems Corp,** Hilliard, Ohio.
Circle 431

Image analyzer
Descriptions and illustrations of the Quantimet 10 accompany technical specs, measurements, and system options. **Cambridge Instruments, Inc,** Monsey, NY.
Circle 432

Short-haul modems
Folder describes standalone and rack-mounted models, explaining star network topology applications. **Remark Datacom Inc,** Woodbury, NY. **Circle 433**

Assembly tools
Booklet features and specifies a new line of desoldering equipment, and catalogs other tools and accessories, including soldering aids, IC test clips, printed circuit boards, IC dispensers, and circuit troubleshooting kits. **OK Industries, Inc,** Bronx, NY. **Circle 434**

Electronic components
Brochure profiles research, products, system approach and applications support. **Philips, Electronic Components and Materials Div,** Eindhoven, The Netherlands. **Circle 435**

Overview of CAD/CAM
Brochure focuses on networking; third-party application software; communication systems; custom computing; and mechanical, architectural, civil, and electronics engineering. **Digital Equipment Corp,** Marlboro, Mass.
Circle 436

Switching power supplies
Information package contains product specs for the Companion 150- and 300-W models, details on the dc-dc converter and battery module, and an overview of the Companion series. **Reliance Comm/Tec,** Cleveland, Ohio.
Circle 437

Metric transition
Manual contains guidelines and strategies for metric changeover in design, engineering, manufacturing, and data processing services; standards, measurement units, training, purchasing, and production are covered. For a copy, send a self-addressed stamped envelope to **American National Metric Council,** 5410 Grosvenor Ln, Bethesda, MD 20814.

Ionized air
Folder presents 911 ionized air blower features, explaining the need for ionized air in the electronics workplace. **3M,** St Paul, Minn. **Circle 438**

Subminiature-D connectors
Bulletin introduces emi filtered and shielded connector line. **Spectrum Control, Inc,** Erie, Pa.
Circle 439

Logic analysis
Primer provides a general approach to analysis fundamentals followed by a discussion of the company's design approach to advanced options and their application. **Dolch Logic Instruments, Inc,** San Jose, Calif.
Circle 440

Micro systems and peripherals
Product information on the Z80 based QDP product line includes separate data sheets on the QDP-100, QDP-200, and QDP-300 systems. **Quasar Data Products,** Cleveland, Ohio.
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CIRCLE 124

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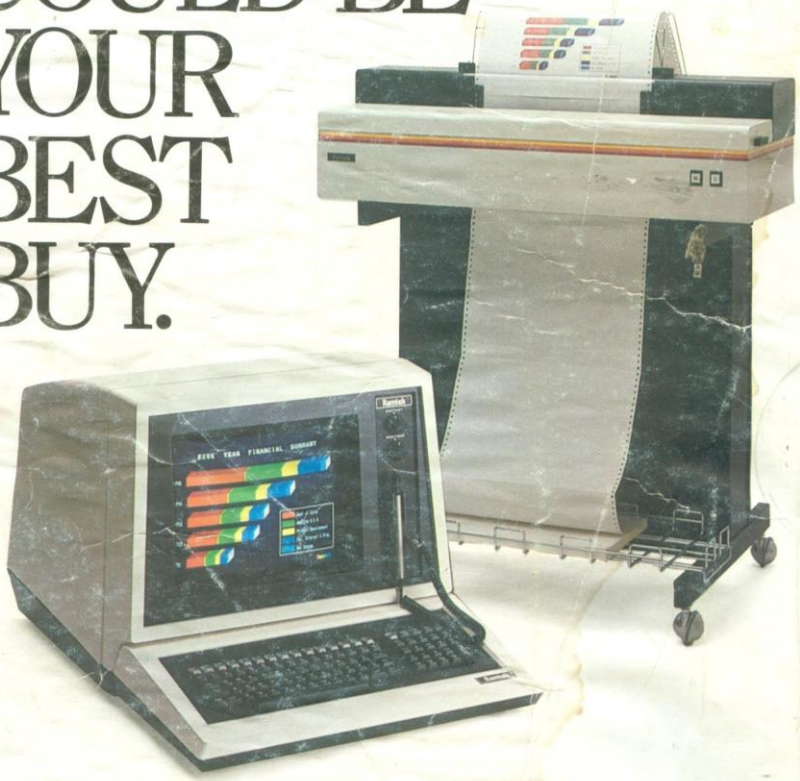

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