

MITSUBISHI LS Is M5M5178AP, J, FP-20, -25, -20L, -25L

65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 8192-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible.

FEATURES

- Fast access time M5M5178AP, J, FP-20, -20L... 20ns(max)
M5M5178AP, J, FP-25, -25L... 25ns(max)
- Low power dissipation Active 300mW(typ)
Stand-by(-20, -25) 5mW(typ)
Stand-by(-20L, -25L) ... 50μW(typ)
- Single +5V power supply
- Fully static operation: No clocks, no refresh
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by $\overline{S_1}$, S_2
- \overline{OE} prevents data contention in the I/O bus
- Common data I/O

APPLICATION

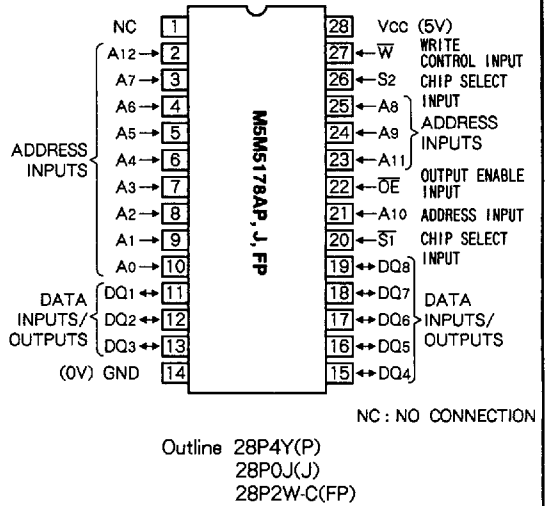
High-speed memory systems

FUNCTION

The operation mode of the M5M5178A is determined by a combination of the device control inputs $\overline{S_1}$, S_2 , \overline{W} and \overline{OE} . Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level \overline{W} overlaps with the low level $\overline{S_1}$ and the high level S_2 . The

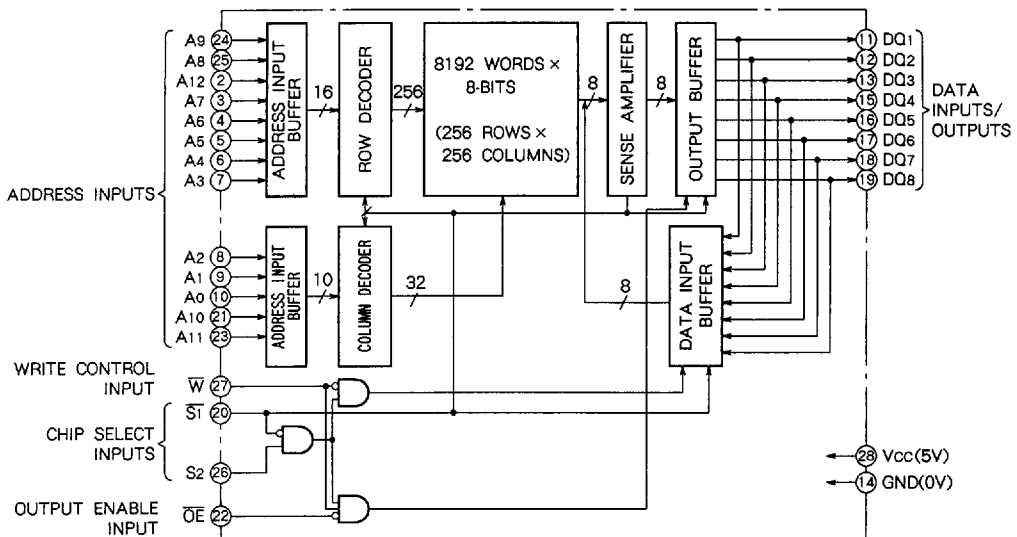
PIN CONFIGURATION (TOP VIEW)



address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1} = L, S_2 = H$)

BLOCK DIAGRAM



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When setting $\overline{S1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$. The power supply current is reduced as low as the stand-by current which is specified as I_{cc2} or I_{cc3} .

FUNCTION TABLE

$\overline{S1}$	S2	\overline{W}	\overline{OE}	Mode	DQ	I _{cc}
L	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

H : V_{IH} L : V_{IL} X : V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 0.5 * ~7	V
V _I	Input voltage		- 0.5 * ~V _{cc} + 0.3	V
V _O	Output voltage		0 ~ V _{cc}	V
P _d	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		- 10~85	°C
T _{stg}	Storage temperature		- 65~150	°C

* = -3.5V in case of AC (pulse width ≤ 20ns), -0.5V in case of DC

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{cc} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High input voltage		2.4		V _{cc} +0.3	V
V _{IL}	Low input voltage		- 0.5*		0.6	V
V _{OH}	High output voltage	I _{OH} = - 4mA	2.4			V
V _{OL}	Low output voltage	I _{OL} = 8mA			0.4	V
I _I	Input current	V _I = 0~V _{cc}			± 10	μA
I _{ozH}	High level output current in off-state	$\overline{S1} = V_{IH}$ or S2 = V _{IL} or $\overline{OE} = V_{IH}$			10	μA
I _{ozL}	Low level output current in off-state	V _{I/O} = 0~V _{cc}			- 10	μA
I _{cc1}	Active supply current	$\overline{S1} = V_{IL}$ or S2 = V _{IH} Output open Other inputs = V _{IH}	AC(25MHz)		120	mA
			DC	60	70	
I _{cc2}	Stand by supply current	S2 = V _{IL} , $\overline{S1} = V_{IH}$ Other inputs = 0~V _{cc}	AC(25MHz)		30	mA
			DC		20	
I _{cc3}	Stand by supply current	$\overline{S1} = V_{cc} - 0.2V$ Other inputs ≤ 0.2V or V _{cc} - 0.2V	-20, -25		2	mA
			-20L, -25L	50	100	
C _i	Input capacitance	$\overline{S1}, S2, \overline{OE}, W$ A ₀ ~A ₁₂	V _I = GND, V _I = 25mVrms, f = 1MHz		7	pF
					6	
C _o	Output capacitance		V _O = GND, V _O = 25mVrms, f = 1MHz		7	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark).

2. C_i, C_o are periodically sampled and are not 100% tested.

* = -3.0V in case of AC (pulse width ≤ 20ns), -0.5V in case of DC

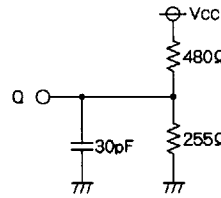
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AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)

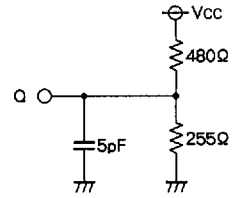
(1) MEASUREMENT CONDITIONS

Input pulse levels $V_{IH} = 3V, V_{IL} = 0V$
 Input rise and fall time 3ns
 Input timing standard levels $V_{IH} = V_{IL} = 1.5V$
 Output timing reference levels $V_{OH} = V_{OL} = 1.5V$
 Output loads Fig. 1, Fig. 2



(Including scope and JIG)

Fig. 1 Output load



(Including scope and JIG)

Fig. 2 Output load for t_{en}, t_{dis}

(2) Read cycle

Symbol	Parameter	Limits				Unit
		M5M5178A-20, -20L		M5M5178A-25, -25L		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	20		25		ns
$t_{a(A)}$	Address access time		20		25	ns
$t_{a(S1)}$	Chip select 1 access time		20		25	ns
$t_{a(S2)}$	Chip select 2 access time		15		18	ns
$t_{a(OE)}$	Output enable access time		10		12	ns
$t_{v(A)}$	Data valid time after address change	3		3		ns
$t_{en(S1)}$	Output enable time after $\overline{S1}$ low	3		3		ns
$t_{dis(S1)}$	Output disable time after $\overline{S1}$ high		10		15	ns
$t_{en(S2)}$	Output enable time after $S2$ high	2		2		ns
$t_{dis(S2)}$	Output disable time after $S2$ low		10		15	ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	2		2		ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high		10		15	ns
t_{PU}	Power-up time after chip selection	0		0		ns
t_{PD}	Power-down time after chip selection		20		25	ns

(3) Write cycle

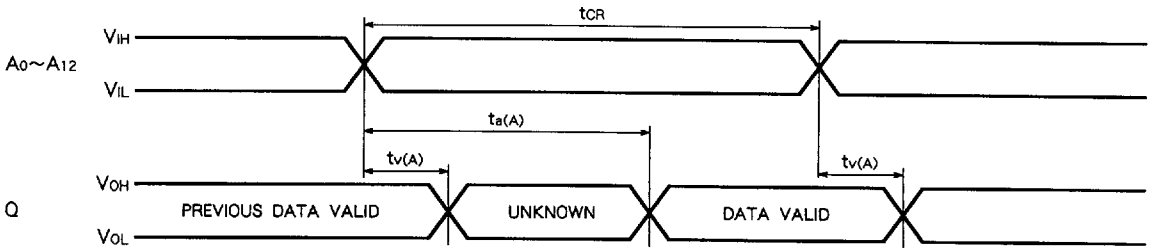
Symbol	Parameter	Limits				Unit
		M5M5178A-20, -20L		M5M5178A-25, -25L		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	20		25		ns
$t_{su(S1)}$	Chip select 1 set up time	16		20		ns
$t_{su(S2)}$	Chip select 2 set up time	12		15		ns
$t_{su(A)1}$	Address set up time 1 (\overline{W} control)	0		0		ns
$t_{su(A)2}$	Address set up time 2 ($\overline{S1}$ control)	0		0		ns
$t_{su(A)3}$	Address set up time 3 ($S2$ control)	0		0		ns
$t_{w(W)}$	Write pulse width	15		18		ns
$t_{rec(W)}$	Write recovery time	3		3		ns
$t_{au(D)}$	Data set up time	10		12		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{dis(W)}$	Output disable time after \overline{W} low		10		12	ns
$t_{en(W)}$	Output enable time after \overline{W} high	0		0		ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high		10		15	ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	2		2		ns
$t_{su(A-\overline{WH})}$	Address to \overline{W} high	15		18		ns

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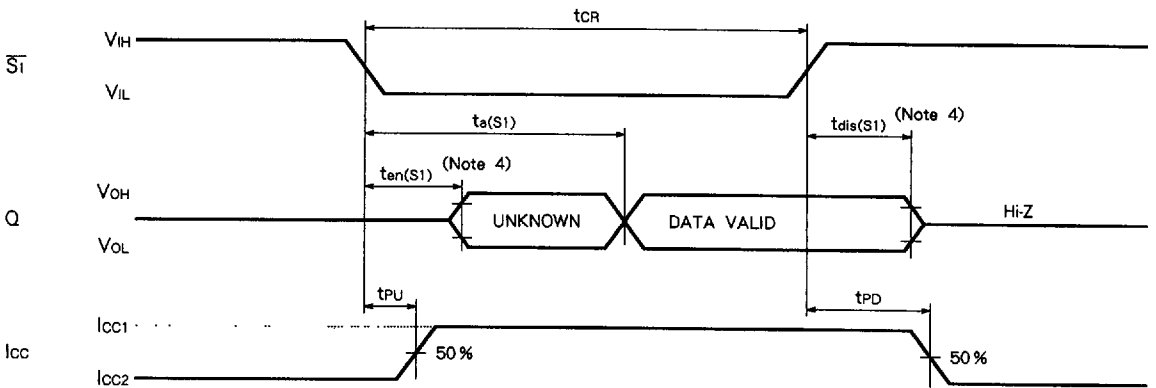
(4) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$$\begin{aligned} \overline{S_2} = \overline{W} = H \\ \overline{S_1} = \overline{OE} = L \end{aligned}$$

Read cycle 2 (Note 3)

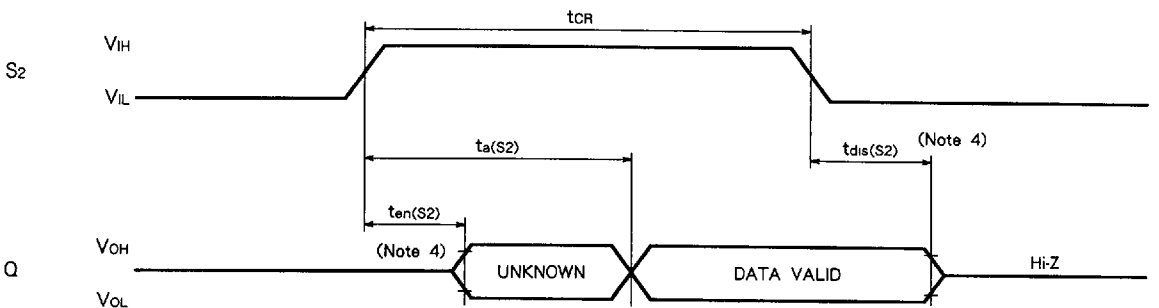


$$\begin{aligned} \overline{S_2} = \overline{W} = H \\ \overline{OE} = L \end{aligned}$$

Note 3. Addresses valid prior to or coincident with $\overline{S_1}$ transition low.

4. Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 5)



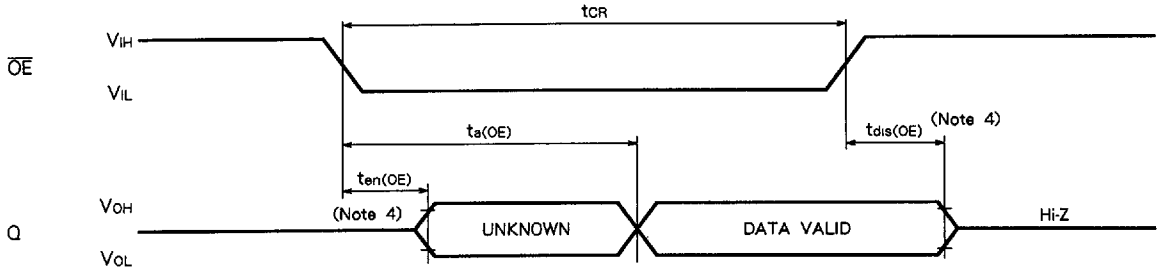
$$\begin{aligned} \overline{W} = H \\ \overline{S_1} = \overline{OE} = L \end{aligned}$$

Note 5. Addresses and $\overline{S_1}$ valid prior to S_2 transition high by $[t_{a(A)} - t_{a(S2)}, t_{a(S1)} - t_{a(S2)}]$.

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Read cycle 4 (Note 6)

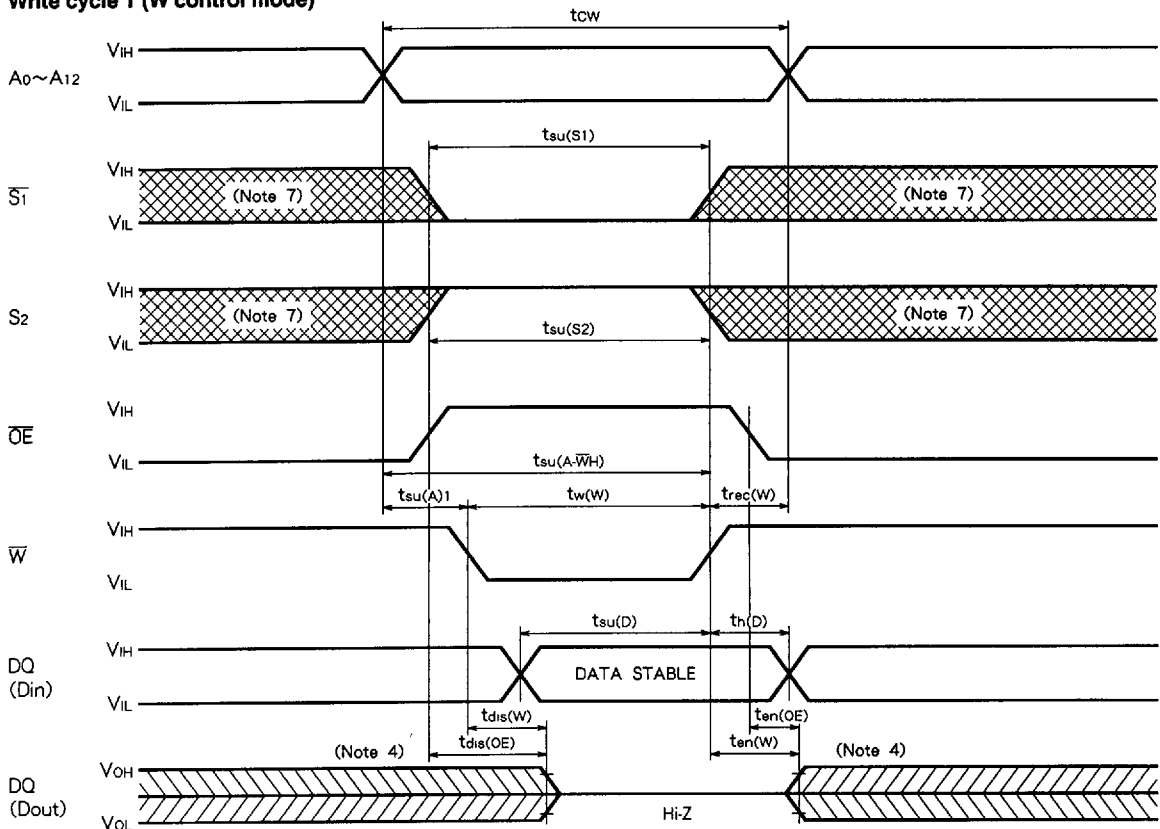


$$\begin{aligned} S_2 = \bar{W} = H \\ \bar{S}_1 = L \end{aligned}$$

Note 6. Addresses and \bar{S}_1 valid prior to \bar{OE} transition low by $[t_a(A) - t_a(OE), t_a(S_1) - t_a(OE)]$.

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 (\bar{W} control mode)

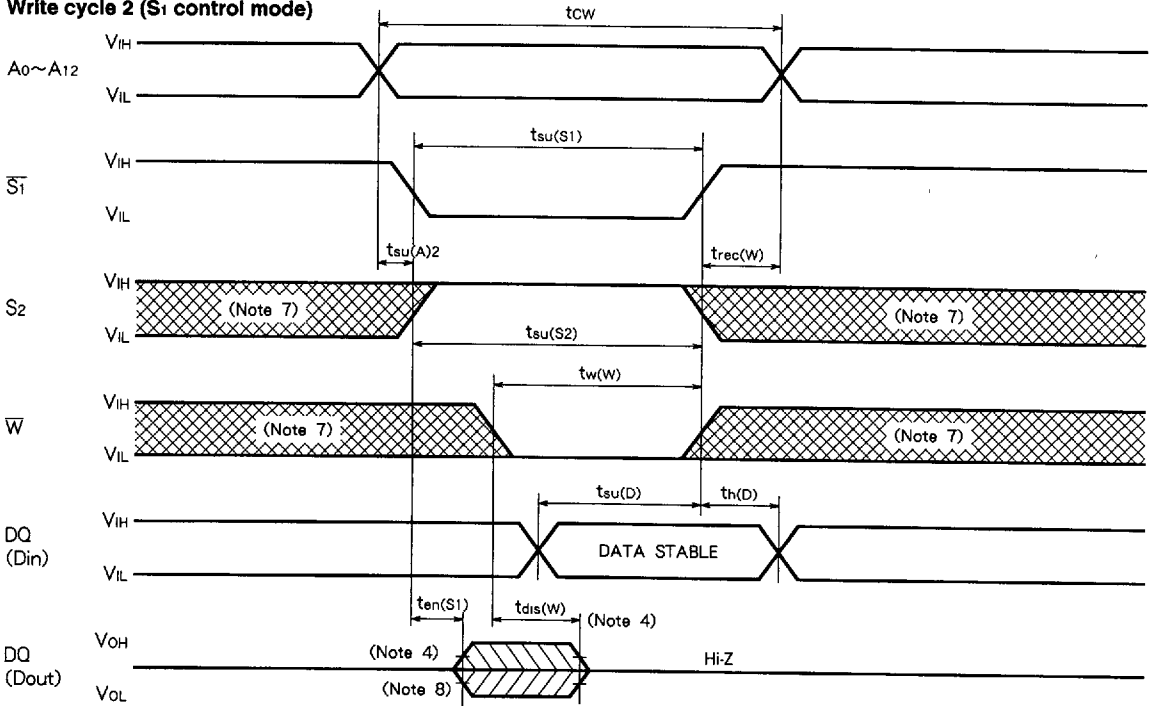


Note 7. Hatching indicates the state is don't care.

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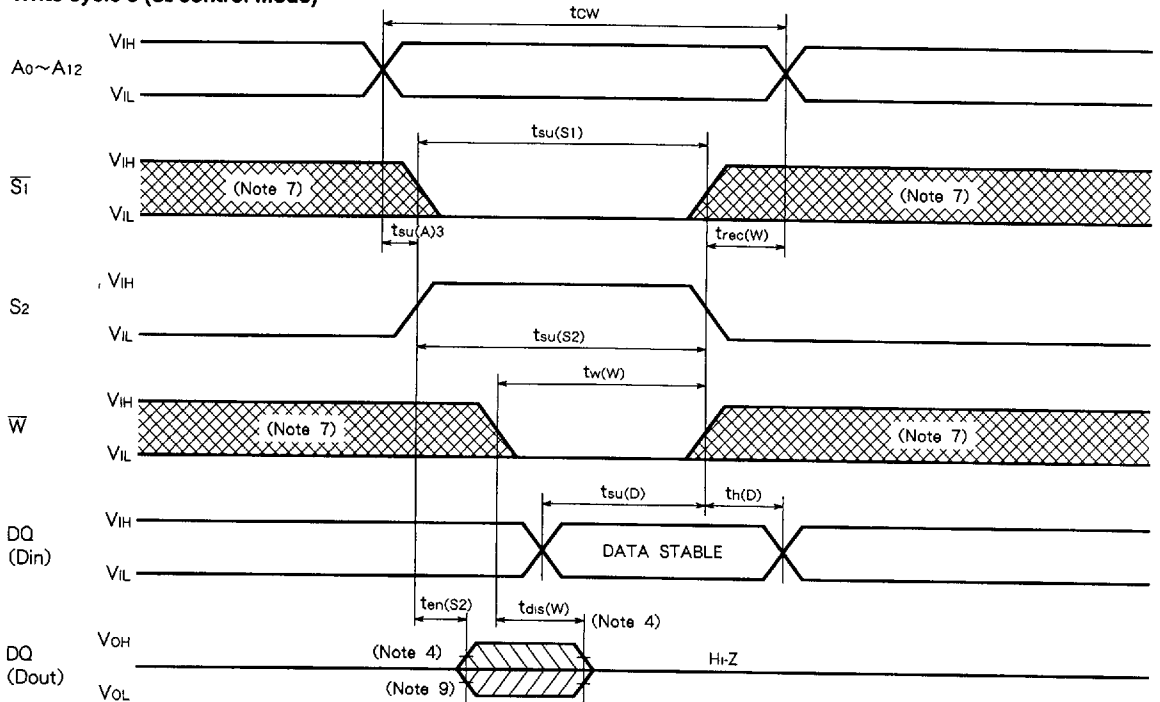
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Write cycle 2 ($\overline{S_1}$ control mode)



Note 8. When the falling edge of \overline{W} is simultaneous or prior to the falling edge of $\overline{S_1}$, the output is maintained in the high impedance.

Write cycle 3 (S_2 control mode)



Note 9. When the falling edge of \overline{W} is simultaneous or prior to the rising edge of S_2 , the output is maintained in the high impedance.

10. t_{en} , t_{dis} are periodically sampled and are not 100% tested.

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POWER DOWN CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC(PD)}	Power down supply voltage		2			V
V _{I(ST)}	Chip select input voltage	V _{I(ST)} ≥ V _{CC} - 0.2V	V _{CC} -0.2			V
t _{su(PD)}	Power down setup time	V _I ≥ V _{CC} - 0.2V or 0V ≤ V _I ≤ 0.2V	0			ns
t _{rec(PD)}	Power down recovery time		-20L -25L	20 25		ns
I _{CC(PD)}	Power down supply current	V _{CC} = 3.0V			50	μA
		V _{CC} = 5.5V			100	

Note 11. This is only M5M5178AP, J, FP-20L, -25L

TIMING WAVEFORM FOR POWER DOWN

