8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2063P-10, TMM2063P-12 TMM2063P-15

DESCRIPTION

The TMM2063P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When $\overline{CS_1}$ is a logical high or CS_2 is a logical low, the device is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2063P is most suitable for use in microcomputer peripheral memory where the low power applications are required, moreover, suitable for use in high density assembly as 0.3 inch width package is use for. The TMM2063P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

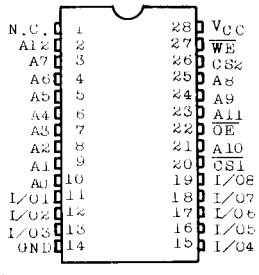
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2063P-10	100ns	80mA	10mA
TMM2063P-12	120ns	80mA	10mA
TMM2063P-15	150ns	80mA	10mA

- High Density Assembly Capability : 0.3 inch width package (28 pin plastic DIP)
- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : $\overline{CS_1}$, CS_2
- Output Buffer Control : $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

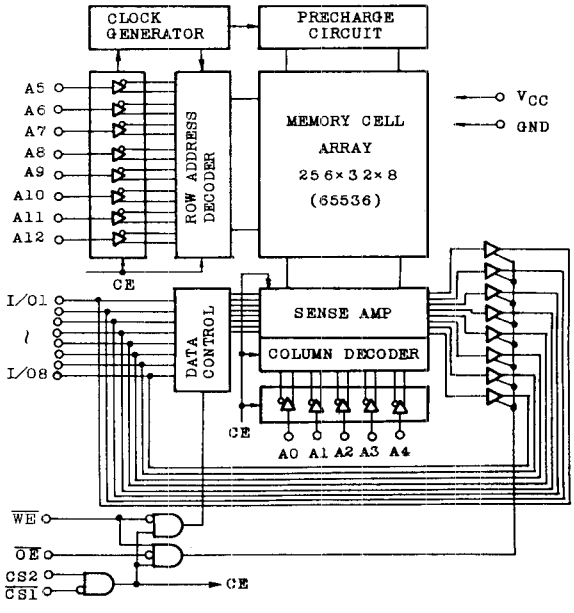
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_4$	Column Address Inputs
$A_5 \sim A_{12}$	Row Address Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	0.8	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS_1}$=V_{CC}, CS_2=0V I_{OUT}=0mA	—	—	20	mA
I_{SB}	Standby Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, I_{OUT}=0mA	—	—	10	mA
I_{CC}	Operating Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{OUT}=0mA	—	—	80	mA

CAPACITANCE*** (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta = 0~70°C, V_{CC} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CS_1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CS_2 Access Time	—	100	—	120	—	150	
t_{OE}	$\overline{OE}$ Access Time	—	40	—	50	—	60	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t_{CLZ}	Output Enable Time from $\overline{CS_1}$ or CS_2	10	—	10	—	10	—	
t_{CHZ}	Output Disable Time from $\overline{CS_1}$ or CS_2	—	40	—	40	—	55	
t_{OLZ}	Output Enable Time from $\overline{OE}$	5	—	5	—	5	—	
t_{OHZ}	Output Disable Time from $\overline{OE}$	—	35	—	35	—	50	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	60	—	60	

Write Cycle

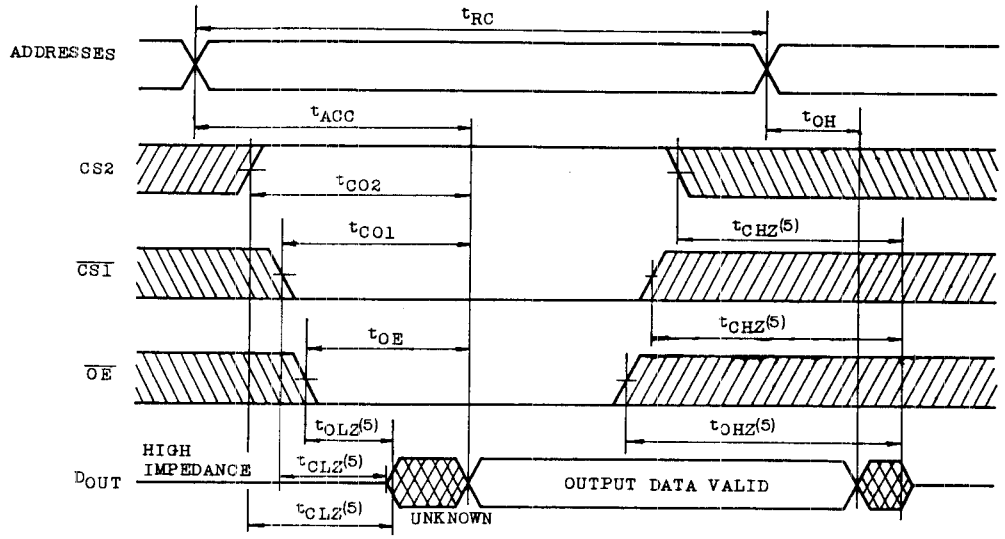
SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	80	—	100	—	120	—	
t_{AS}	Address Set Up Time	10	—	10	—	10	—	
t_{WP}	Write Pulse Width	70	—	85	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	Output Enable Time from $\overline{WE}$	5	—	5	—	5	—	
t_{WHZ}	Output Disable Time from $\overline{WE}$	—	30	—	35	—	40	

A. C. TEST CONDITIONS

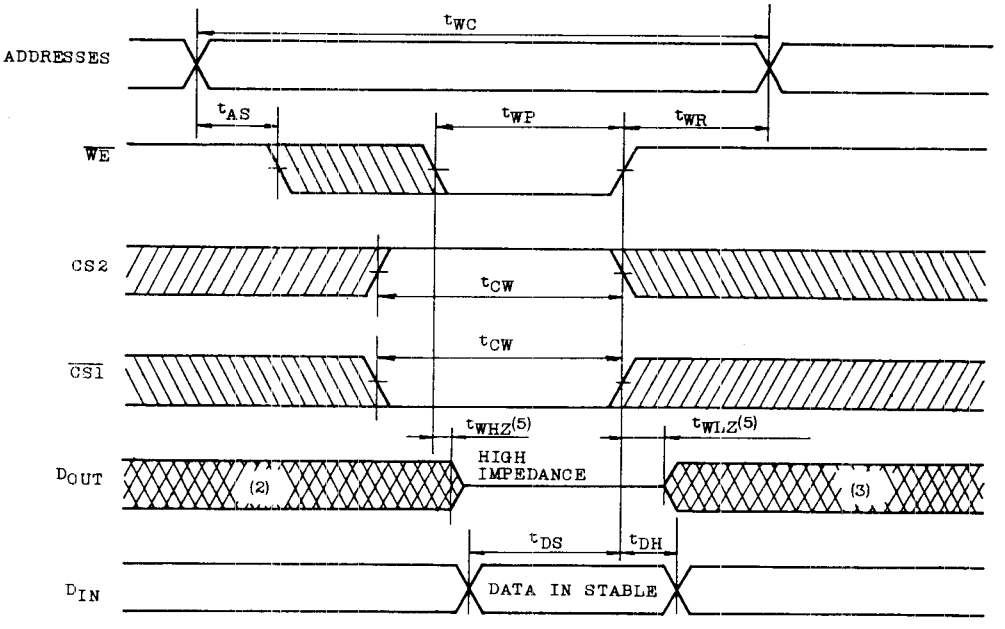
Input Pulse Levels	V_{IH} = 2.2V, V_{IL} = 0.6V
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & C_L = 100pF

TIMING WAVEFORMS

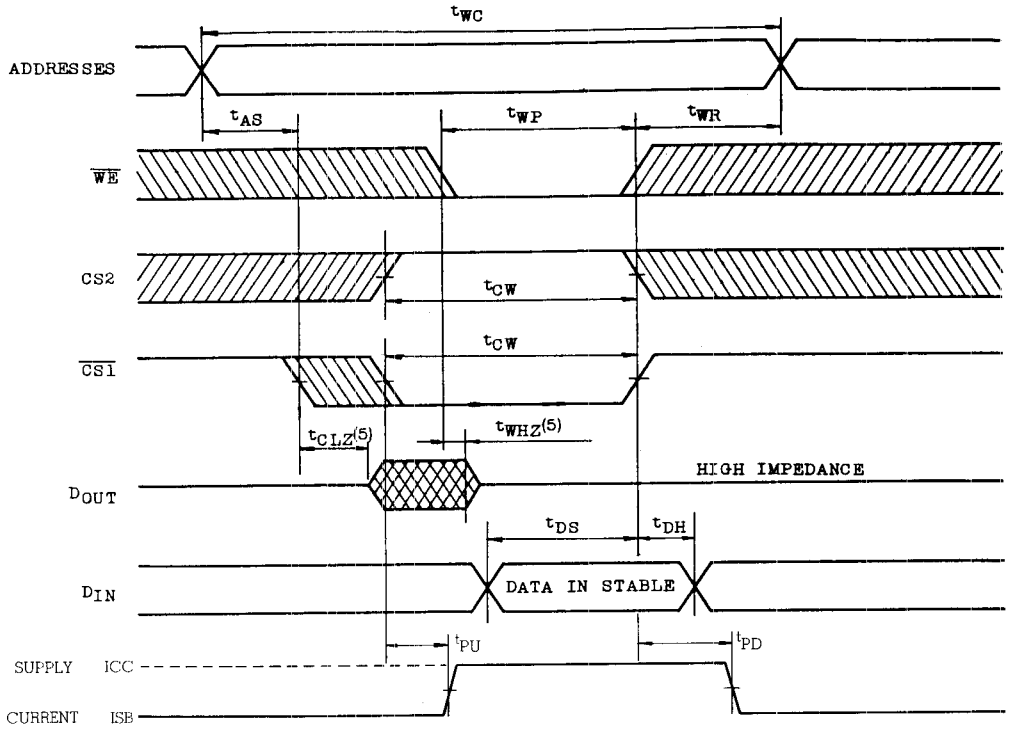
- READ CYCLE (1)



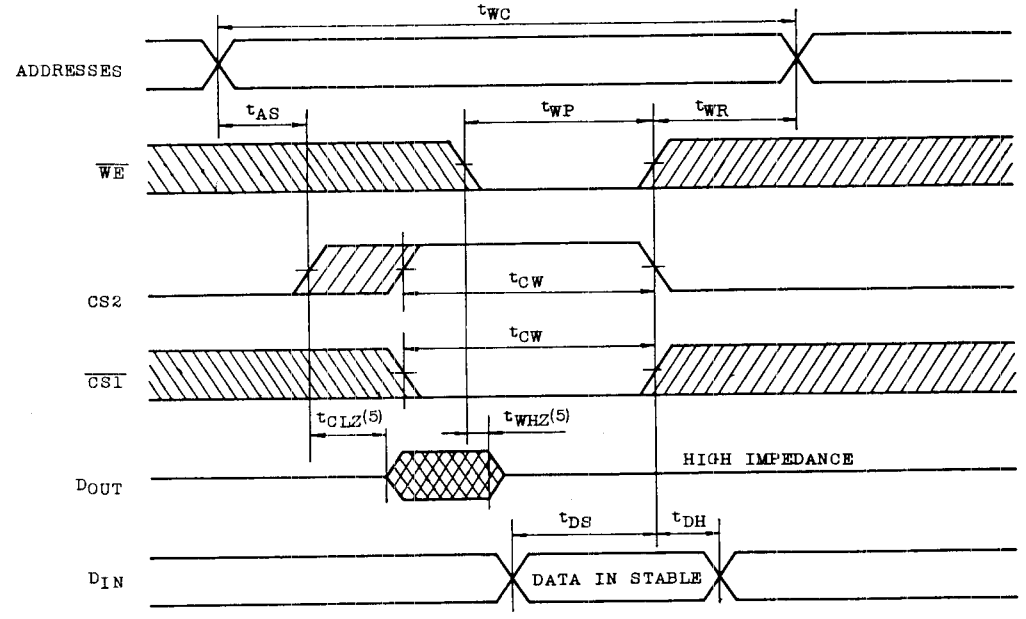
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or CS_2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or CS_2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time

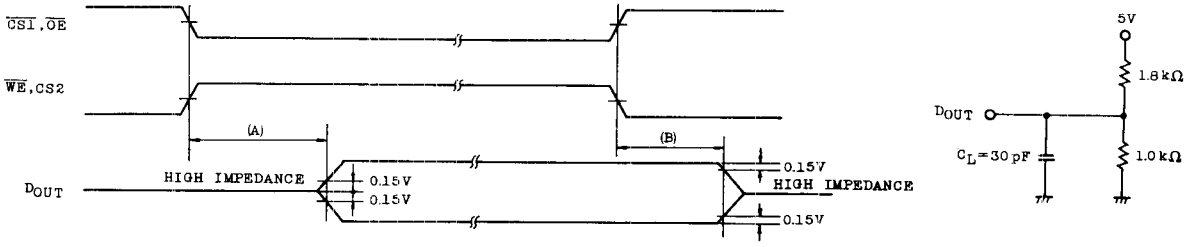
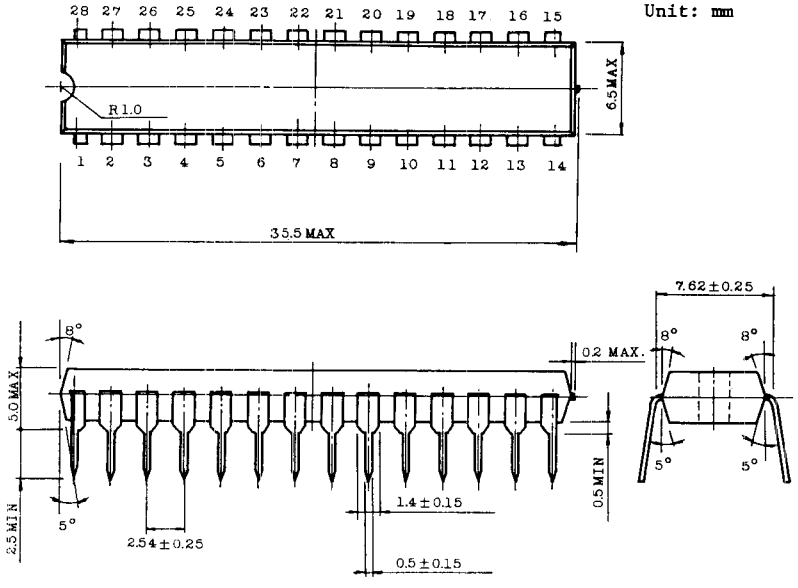


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.