8K-Word×8 bit Mask Programmable ROM

Description

The CXK3864 is a CMOS mask-programmable ROM organized as 8,192 words by 8 bits. The Chip Enable input deselects the outputs and puts the chip in a power down mode. The active level of the Output Enable is defined by the customer.

Features

- Fast access time: 200 ns Max
- Automatic power down
- Fully static operation . . . No clock or timing strobe required
- Pin compatible with EPROM i2764
- Directly TTL compatible: All inputs and outputs
- Three state output
- Single +5V supply
- Low power dissipation
  - 165 mW maximum (active, unloaded, 200 ns cycle rate)
  - 16.5 mW maximum (standby, TTL inputs)
  - 165 μW maximum (standby, full rail inputs)

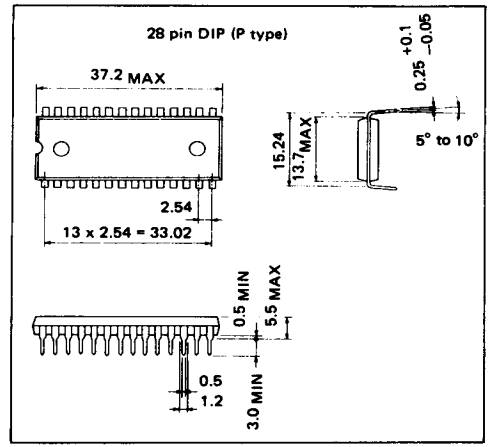
Structure

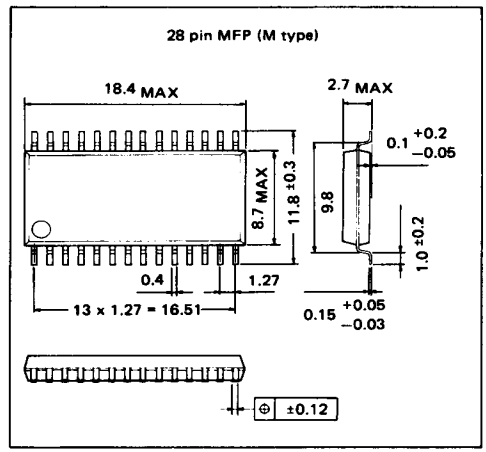
Silicon gate CMOS IC

Function

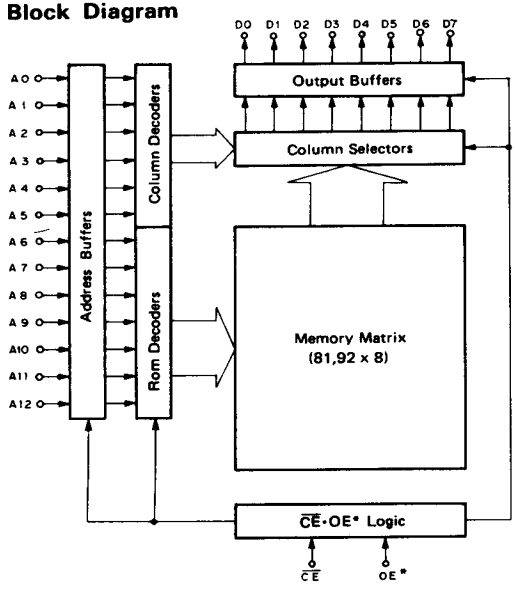
8,192-word × 8 bit mask-programmable ROM

Package Outline Unit: mm



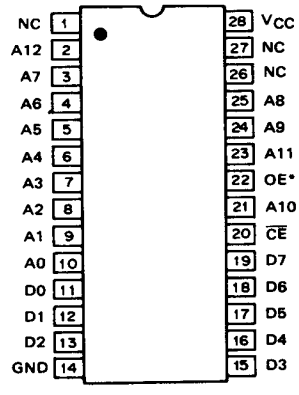


Block Diagram



* The active level defined by the customer.

Pin Configuration (Top View)



* Active level defined by customer

Pin Names

Symbol	Description
A0 to A12	Address Input
D0 to D7	Data Output
$\overline{CE}$	Chip Enable
OE*	Output Enable
Vcc	+5V Power Supply
GND	Ground
NC	Non Connection

Absolute Maximum Ratings

Ta=25°C (GND=0V)

Item	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to +7.0	V
Input Voltage	VIN	−0.5 to Vcc+0.5	V
Output Voltage	VOUT	−0.5 to Vcc+0.5	V
Allowable Power Dissipation	PD	M 0.7	W
		P 1.0	
Operating Temperature	Topr	−10 to +85	°C
Storage Temperature	Tstg	−55 to +150	°C
Soldering Temperature	Tsolder	260 • 10	°C • sec

Truth Table

$\overline{CE}$	$\overline{OE}$	Mode	Output Pin	Vcc Current
H	×	Not Selected	High Z	I_{SB1}, I_{SB2}
L	H	Not Selected	High Z	I_{CC1}, I_{CC2}
L	L	Selected	Data Output	I_{CC1}, I_{CC2}

Note: ×: H or L

DC Recommended Operating Conditions

Ta=0 to +70°C (GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

DC and Operating Characteristics (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test condition	Min.	Typ.*	Max.	Unit
Input Leakage Current	I_{LI}	$0V \leqq V_{IN} \leqq V_{CC}$	−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, or $\overline{OE}=V_{IH}$ $0V \leqq V_{OUT} \leqq V_{CC}$	−2	—	2	μA
Operating Current (DC)	I_{CC1}	$\overline{CE}=V_{IL}$ I_{OUT}=0mA	—	—	30	mA
Average Operating Current	I_{CC2}	$\overline{CE}=V_{IL}$ I_{OUT}=0mA Cycle=min, Duty=100%	—	—	30	mA
Standby Current	I_{SB1}	$\overline{CE} \geqq V_{CC}-0.2V$	—	1	30	μA
	I_{SB2}	$\overline{CE}=V_{IH}$	—	0.5	3	mA
Output High Voltage	V_{OH}	$I_{OUT}=-400\mu A$	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OUT}=2.1mA	—	—	0.4	V

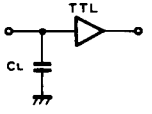
* Typical values are measured at V_{CC}=5V and Ta=25°

AC Characteristics

• AC Test conditions

(V_{CC}=5V±10%, Ta=0 to +70°)

Item	Test Condition
Input Pulse High Level	V_{IH}=2.4V
Input Pulse Low Level	V_{IL}=0.6V
Input Rise Time	t_R=10nS
Input Fall Time	t_F=10nS
Input Reference Level	V_{IL}=0.8V, V_{IH}=2.2V
Output Reference Level	V_{OL}=0.8V, V_{OH}=2.2V
Output Load	C_L*=100pF, 1TTL



* C_L includes scope and jig capacitance

AC Characteristics

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
Chip Enable Access Time	t_{CO}	—	200	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Hold from Address Change	t_{OH}	0	—	ns
Chip Enable to Output in Low Z ($\overline{CE}$)	t_{LZ}	0	—	ns
Output Enable to Output in Low Z ($\overline{OE}$)	t_{OLZ}	0	—	ns
Chip Disable to Output in High Z ($\overline{CE}$)	*t_{HZ}	—	80	ns
Output Disable to Output in Low Z ($\overline{OE}$)	*t_{OHZ}	—	80	ns

* t_{HZ} and t_{OHZ} are jadged with the time when outputs are high Z, not with output voltage level.

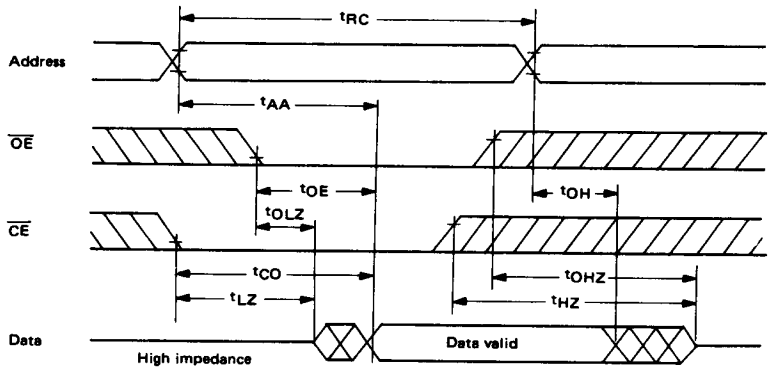
Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10	pF

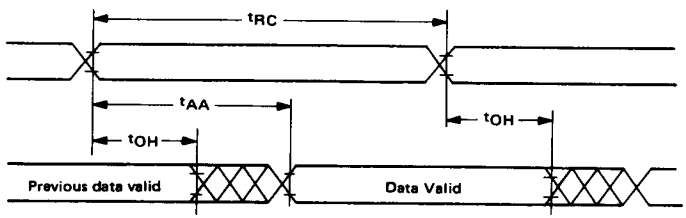
Timing Waveform

• Read cycle (1)

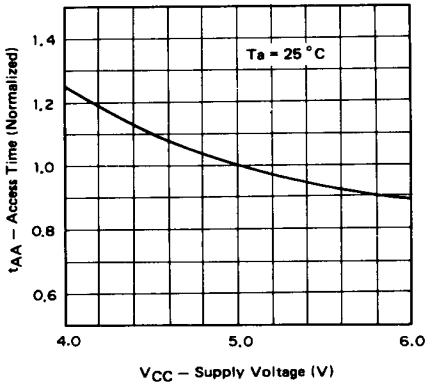


• Read cycle (2)

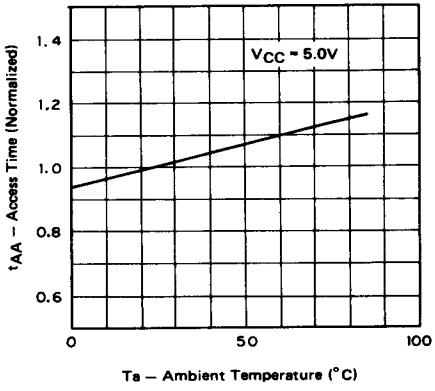
Note: 1. $\overline{CE}$=VIL
2. $\overline{OE}$=VIL



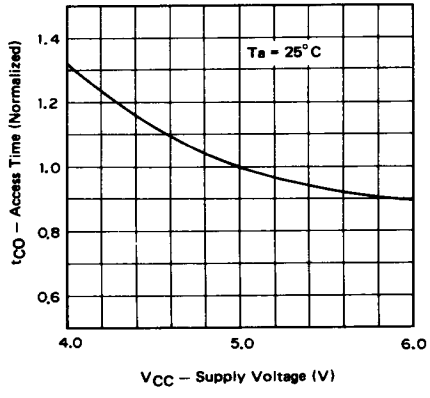
Address Access Time vs. Supply Voltage



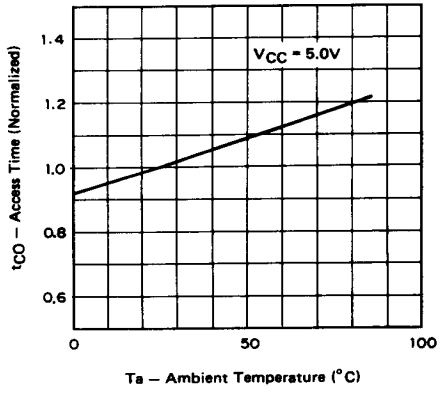
Address Access Time vs. Ambient Temperature



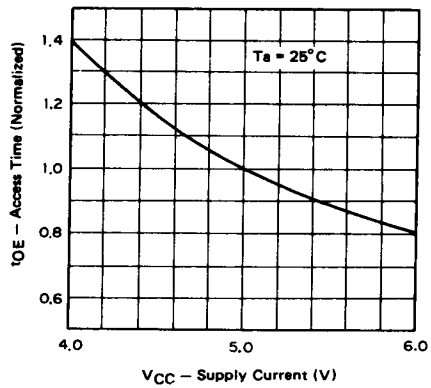
CE Access Time vs. Supply Voltage



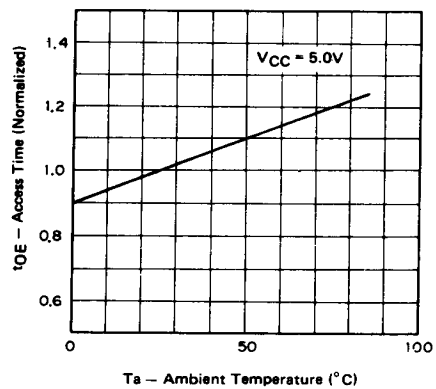
CE Access Time vs. Ambient Temperature



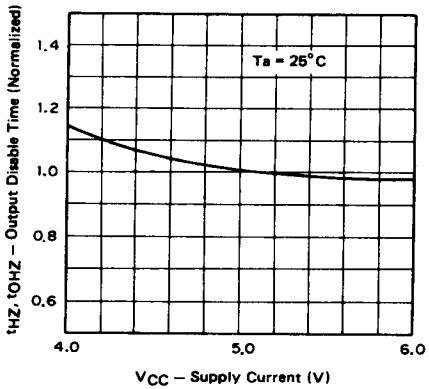
OE Access Time vs. Supply Voltage



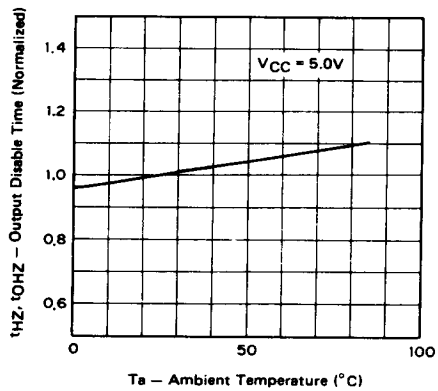
OE Access Time vs. Ambient Temperature



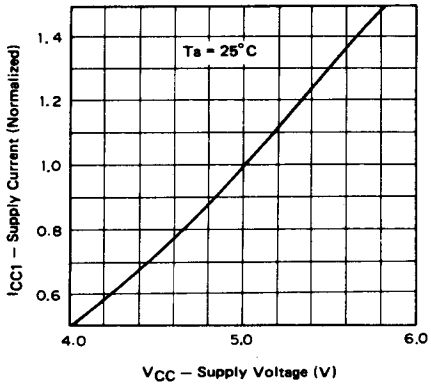
Output Disable Time vs. Supply Current



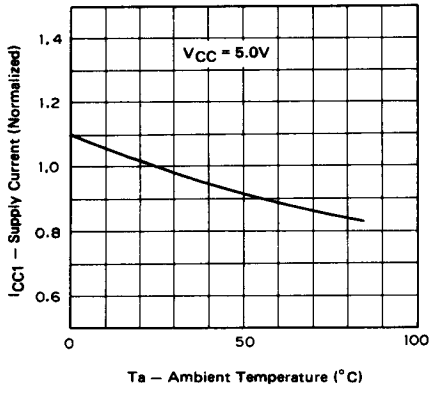
Output Disable Time vs. Ambient Temperature



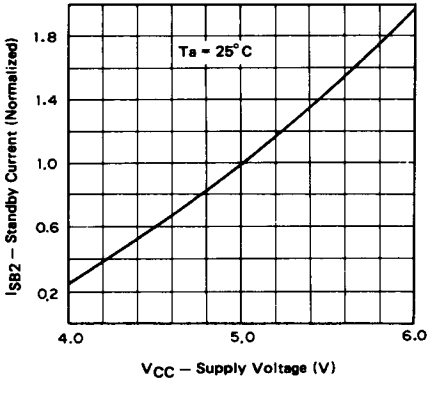
Supply Current vs. Supply Voltage



Supply Current vs. Ambient Temperature



Standby Current vs. Supply Voltage



Standby Current vs. Ambient Temperature