M5M411860TP-6,-8,-6S,-8S

FAST PAGE MODE 1179648-BIT(65536-WORD BY 18-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 65536-word by 18-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density and reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

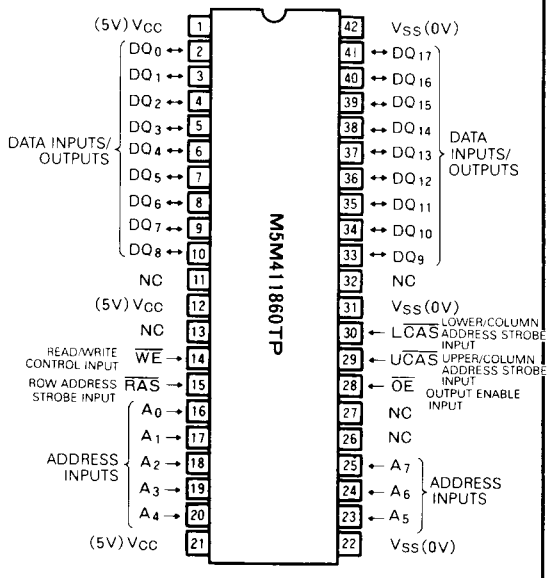
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (max. mW)
M5M411860TP-6,-6S	60	15	30	110	660
M5M411860TP-8,-8S	80	20	40	135	580

- Byte write control can be performed with 1$\overline{WE}$ and 2 $\overline{CAS}$ inputs.
- 42 pin 300 mil TSOP (TYPE II)
- Single 5V±10% supply
- Low stand-by power dissipation
  2.75mW (max) ·····(CMOS input level)
- Fast-page mode, Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, CBR Self refresh (-6S, -8S) capabilities
- Early write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 256 refresh cycles every 4 ms (A_0~A_7)
- 256 refresh cycles every 32ms (A_0~A_7) for Extended Refresh cycle (M5M411860-6S, -8S)

APPLICATION

Storage memory buffer

PIN CONFIGURATION (TOP VIEW)



Outline 42P3U-E (300mil TSOP II)

NC: NO CONNECTION

FAST PAGE MODE 1179648-BIT(65536-WORD BY 18-BIT)DYNAMIC RAM

FUNCTION

The M5M411680TP provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast-page mode, $\overline{RAS}$-only refresh and delayed-write.

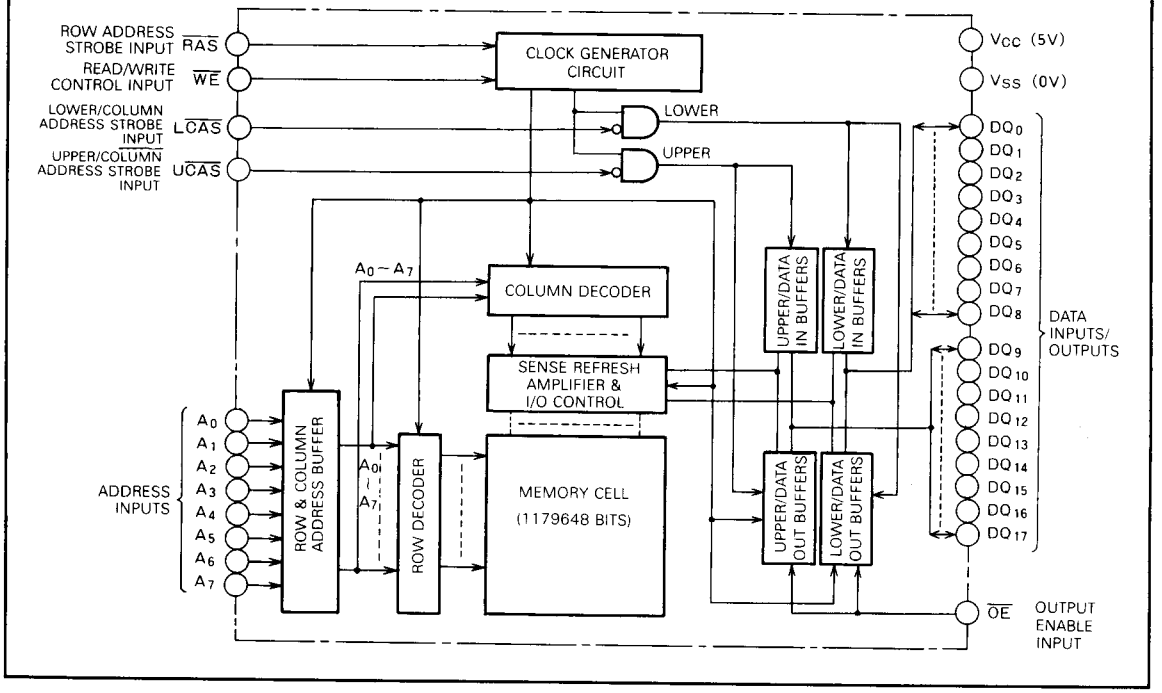
The input conditions for each are shown in Table 1.

Table 1. Input conditions for each mode

Operation	inputs							input/output				Refresh	Remark
								Lower		Upper			
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row address	Colmn address	D	Q	D	Q		
Read	ACT	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	OPN	VLD	YES	Fast-page mode identical
Upper Read	ACT	NAC	ACT	NAC	ACT	APD	APD	DNC	OPN	OPN	VLD	YES	
Lower Read	ACT	ACT	NAC	NAC	ACT	APD	APD	OPN	VLD	DNC	OPN	YES	
Early write	ACT	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper early	ACT	NAC	ACT	ACT	DNC	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower early	ACT	ACT	NAC	ACT	DNC	APD	APD	VLD	OPN	DNC	OPN	YES	
Delayed write	ACT	ACT	ACT	ACT	ACT	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper delayed	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower delayed	ACT	ACT	NAC	ACT	ACT	APD	APD	VLD	OPN	DNC	OPN	YES	
Read-modify-Write	ACT	ACT	ACT	ACT	ACT	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper RMW	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower RMW	ACT	ACT	NAC	ACT	ACT	APD	APD	VLD	OPN	DNC	OPN	YES	
$\overline{RAS}$ only-Refresh	ACT	DNC	DNC	NAC	DNC	APD	DNC	DNC	OPN	DNC	OPN	YES	
Hidden refresh	ACT	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	OPN	VLD	YES	
Upper Hidden-R	ACT	NAC	ACT	DNC	ACT	DNC	DNC	DNC	OPN	OPN	VLD	YES	
Lower Hidden-R	ACT	ACT	NAC	DNC	ACT	DNC	DNC	OPN	VLD	DNC	OPE	YES	
CBR refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPE	YES	
Upper CBR	ACT	NAC	ACT	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Lower CBR	ACT	ACT	NAC	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	NO	

Note: ACT; active, DNC; don't care, VLD; valid, IVD; invalid, APD; applied, OPN; open

BLOCK DIAGRAM



FAST PAGE MODE 1179648-BIT(65536-WORD BY 18-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25℃	1000	mW
Topr	Operating temperature		0～70	℃
Tstg	Storage temperature		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70℃ unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta＝0～70℃, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High level output voltage		I_{OH}＝−2.5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝2.1mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0≦V_{IN}≦6.5V, Other input pins＝0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M411860-6, -6S	$\overline{RAS}$, $\overline{CAS}$ cycling			120	mA
		M5M411860-8, -8S	t_{RC}＝t_{WC}＝min output open			105	
I_{CC2}	Supply current from V_{CC} Stand-by	M5M411860-6, -8	$\overline{RAS}$＝$\overline{CAS}$＝V_{IH}, output open			2	mA
		M5M411860-6S, -8S				2	
		M5M411860-6, -8	$\overline{RAS}$＝$\overline{CAS}$＝$\overline{WE}$＝$\overline{OE}$≧V_{CC}−0.5 output open			0.5	
		M5M411860-6S, -8S				0.1	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M411860-6, -6S	$\overline{RAS}$ cycling, $\overline{CAS}$＝V_{IH}, t_{RC}＝min output open			120	mA
		M5M411860-8, -8S				105	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4)	M5M411860-6, -6S	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$＝cycling, t_{PC}＝min output open			95	mA
		M5M411860-8, -8S				80	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M411860-6, -6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}＝min, output open			80	mA
		M5M411860-8, -8S				65	

ELECTRICAL CHARACTERISTICS (continued)

Self-Refresh M5M411860-6S, -8S (Ta＝0～70℃, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC8}	Average supply current from V_{CC} Buttery Back-up (Extended Refreshing)	$\overline{CAS}$＝0.2V or $\overline{CAS}$ before $\overline{RAS}$ cycling, $\overline{WE}$, $A_{0～7}$, Din＝V_{CC}−0.2V or 0.2V, Q＝OPEN, t_{RC}＝125μs, t_{RAS}＝$t_{RAS(min)}$−1μs,			200	μA
I_{CC9}	Average supply current from V_{CC}, Self-Refresh cycle	$\overline{RAS}$＝$\overline{CAS}$＝0.2V			100	μA

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1} and I_{CC4} are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta＝0～70℃, V_{CC}＝5V±10%, V_{SS}＝0V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I＝V_{SS}, f＝1MHz, V_I＝25mVrms			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/output capacitance, data ports				7	pF

MITSUBISHI ELECTRIC

FAST PAGE MODE 1179648-BIT(65536-WORD BY 18-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS (Ta=0~70℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, See notes 5, 12, 13)

Symbol	Parameter		Limits				Unit
			M5M411860-6, -6S		M5M411860-8, -8S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		60		80	ns
t_{AA}	Column address access time	(Note 6, 9)		30		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		35		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	10	0	10	ns

Note 5; An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6; Measured with a load circuit equivalent to 1TTL load and 30pF.

7; Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

8; Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceed the value shown.

9; Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$. If t_{ASC} is greater than the maximum recommended value shown in this table, t_{AA} will increase by amount that t_{ASC} exceeds the value shown.

10; Assumes that $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \leq t_{CP(max)}$. If $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$, access time (t_{CPA}) is controlled by t_{CAC}. If $t_{ASC} \leq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$ or $t_{ASC} \leq t_{ASC(max)}$ and $t_{CP}-t_{ASC} \geq 5$ns, access time (t_{CPA}) is controlled by t_{AA}.

11; $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leq 10\mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast page Cycles)

(Ta=0~70℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, See notes 11, 12)

Symbol	Parameter		Limits				Unit
			M5M411860-6, -6S		M5M411860-8, -8S		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time			4(32)*		4(32)*	ms
t_{RP}	$\overline{RAS}$ high pulse width		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low		20	45	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 14)	5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 15)	15	30	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 18)	15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 18)	10		10		ns
t_T	Transition time	(Note 19)	1	50	1	50	ns

* : t_{REF} (32ms) is for Extended Refresh cycle (M5M411860-6S, -8S)

Note 12, The timing requirements are assumed t_T=5ns.

13; $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14; $t_{RCD(max)}$ is specified as a reference point only.
If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled by t_{CAC} or t_{AA}.

15; $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled by t_{AA}.

16; $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, t_{AA} is controlled by t_{CAC}.

17; Either t_{DZC} or t_{DZO} must be satisfied.

18; Either t_{CDD} or t_{ODD} must be satisfied.

19; t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M411860-6, -6S		M5M411860-8, -8S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		110		135		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 20)	0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		10		10		ns

Note 20; Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M411860-6, -6S		M5M411860-8, -8S		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		135		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		15		ns
t_{DS}	Date setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Date hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		10		10		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M411860-6, -6S		M5M411860-8, -8S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 21)	145		175		ns
t_{RAS}	$\overline{RAS}$ low pulse width		100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		50	10000	60	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		95		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		50		60		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	30		35		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	75		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 22)	45		55		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
t_{WP}	Write pulse width		10		15		ns
t_{DS}	Date setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Date hold time after $\overline{W}$ low		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		10		10		ns

Note 21; t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$

22; t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition is satisfied (delayed write), the condition of DQ (at access time and untill $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

FAST PAGE MODE 1179648-BIT(65536-WORD BY 18-BIT)DYNAMIC RAM

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits				Unit
		M5M411860-6, -6S		M5M411860-8, -8S		
		Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	75		100		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	100	100000	130	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	10	15	10	20	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	50		60		ns

Note 23; All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24; $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed. $t_{RAS(min)}=t_{CSH(min)}\pm t_{PC(min)}$
25; $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		M5M411860-6, -6S		M5M411860-8, -8S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		ns

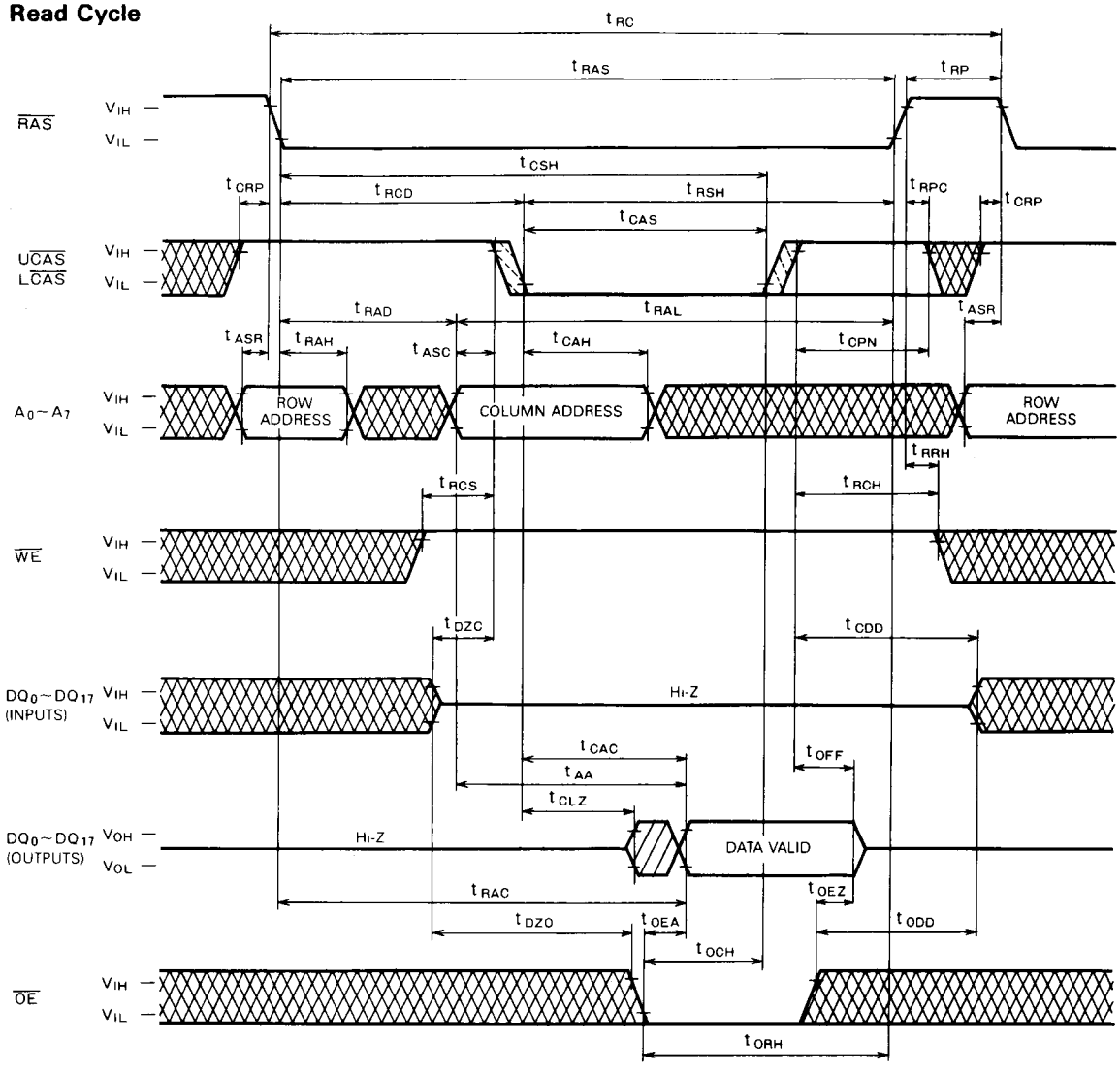
Note 26; Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

$\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle (M5M411860-6S, -8S)

Symbol	Parameter	Limits				Unit
		M5M411860-6S		M5M411860-8S		
		Min	Max	Min	Max	
t_{RASS}	$\overline{RAS}$ low pulse time	100		100		μs
t_{RPS}	$\overline{RAS}$ high precharge time	110		135		ns
t_{CHS}	$\overline{CAS}$ hold time	−50		−50		ns

Timing Diagrams (Note 27)

Read Cycle



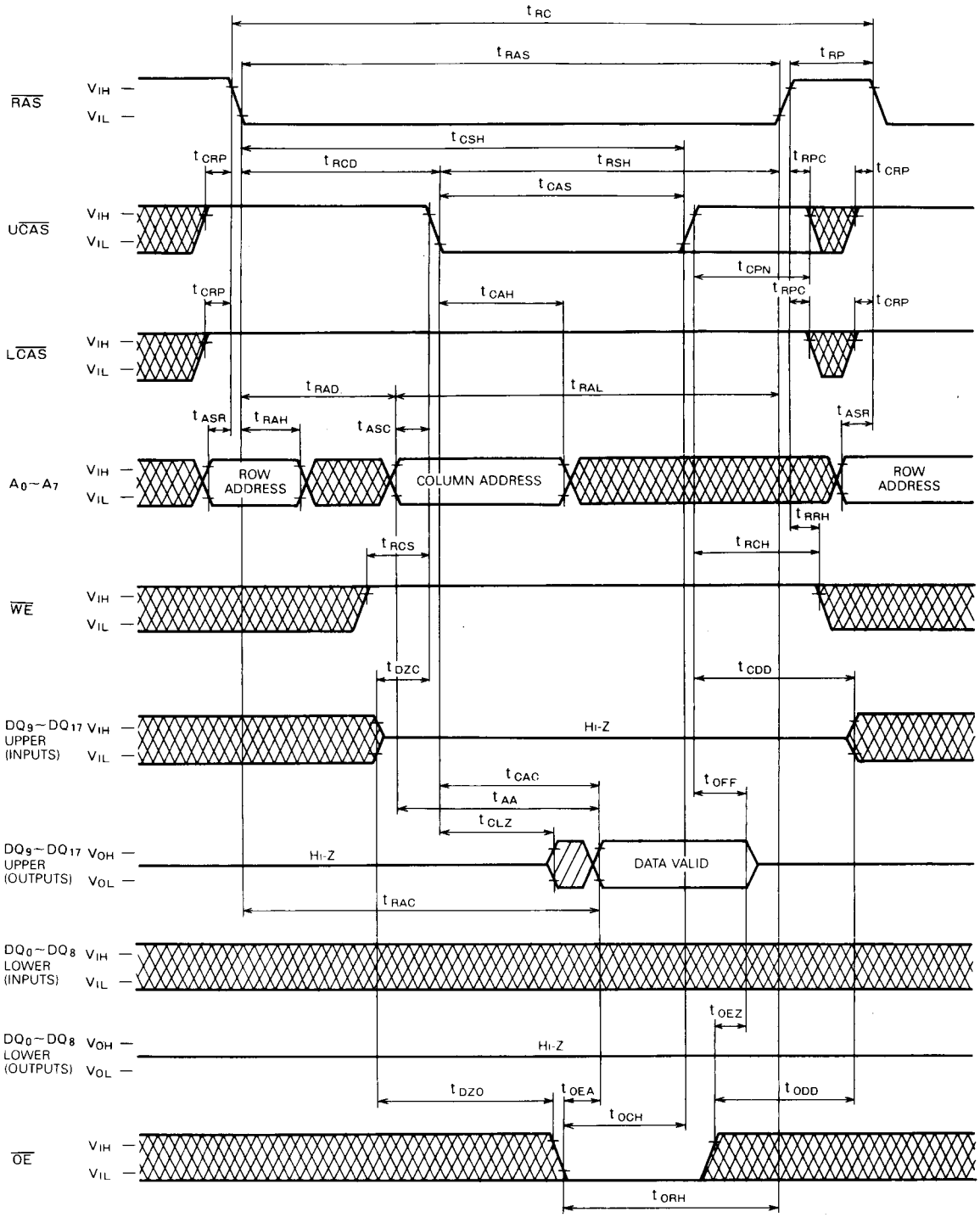
Note 27

Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$.

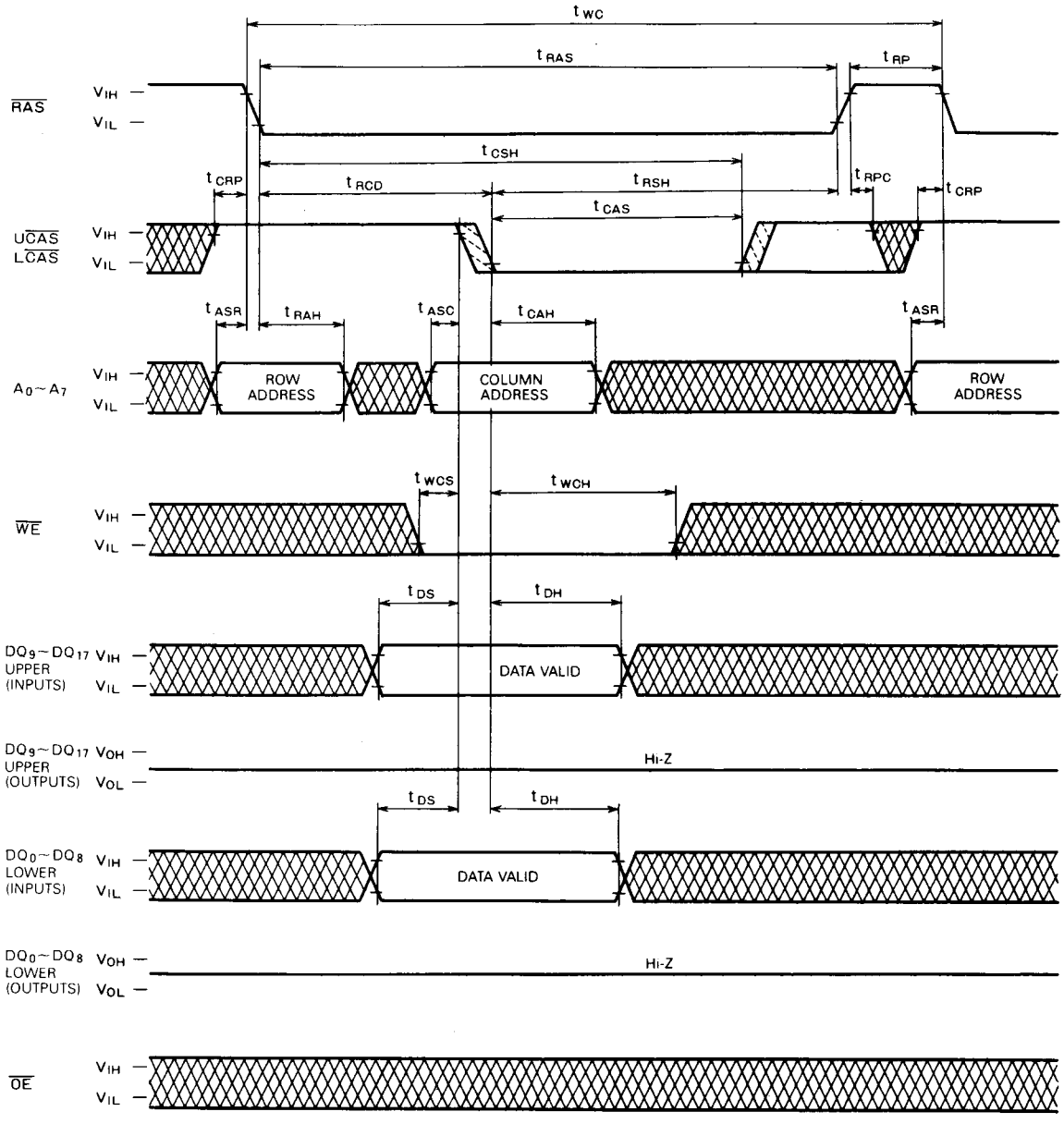
Indicates the invalid output.

Indicates inputs skew of 2 $\overline{CAS}$

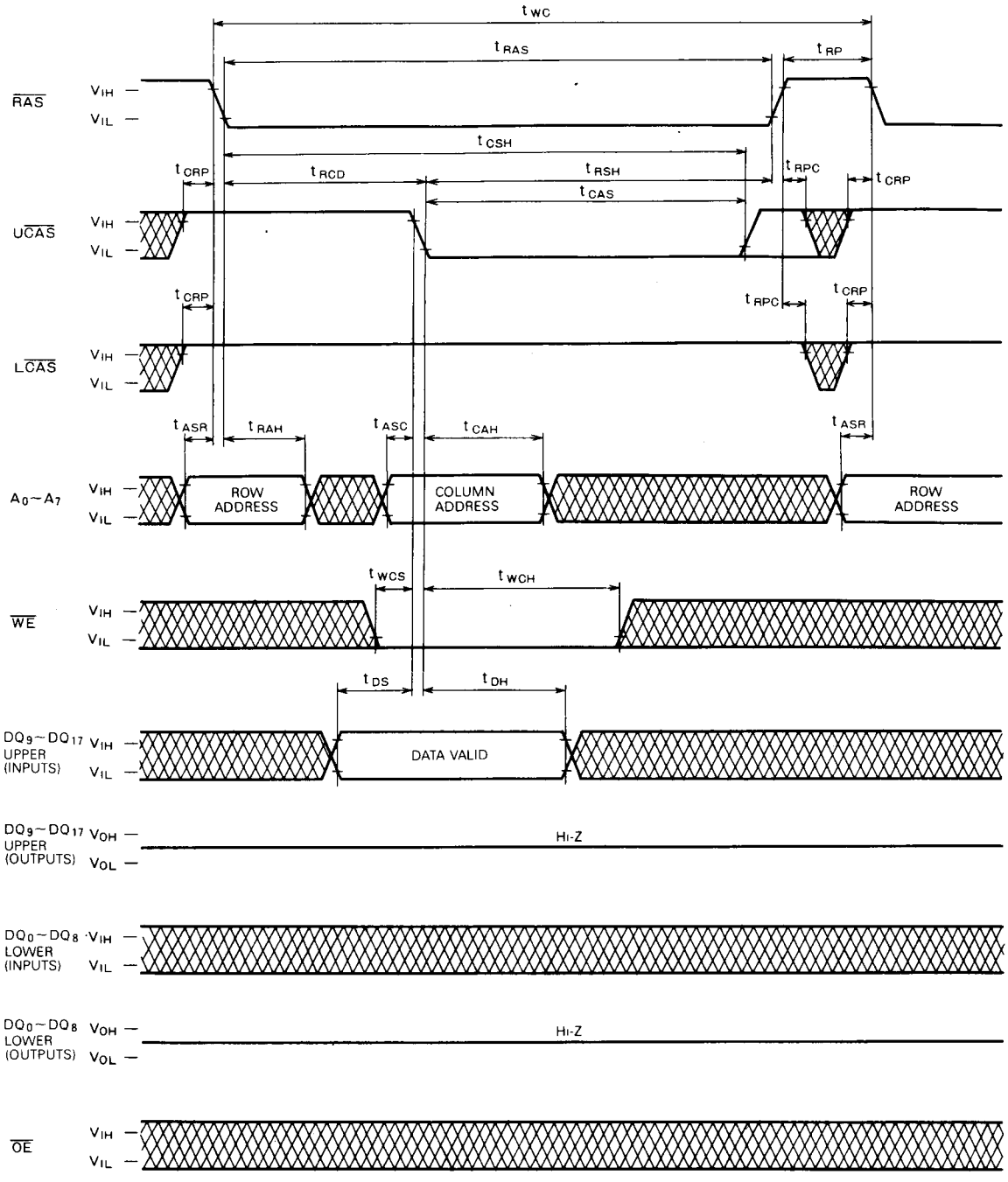
Read Upper (Lower) Byte Cycle



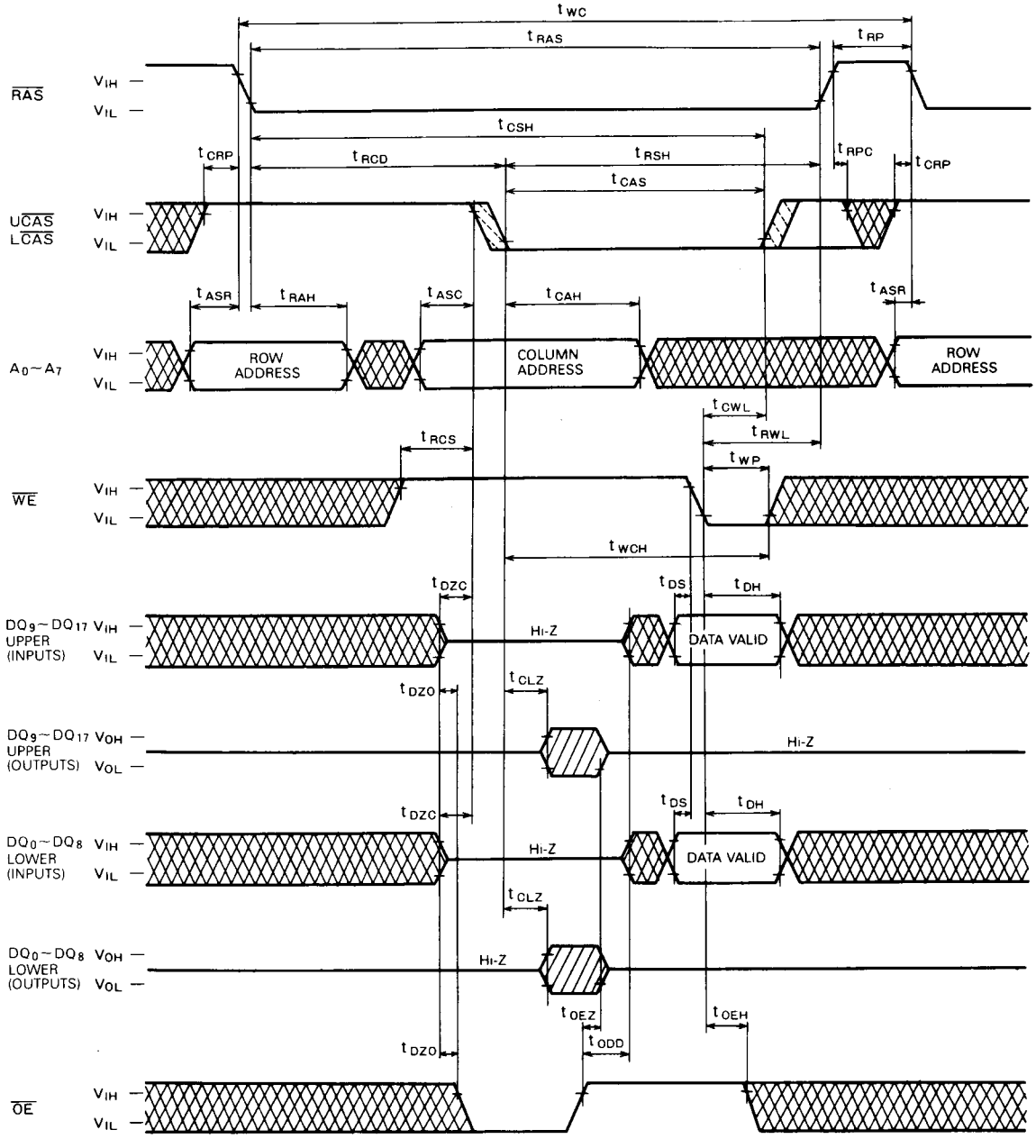
Early Write Cycle



Early Write Upper (Lower) Byte Write Cycle



Delayed Write Cycle



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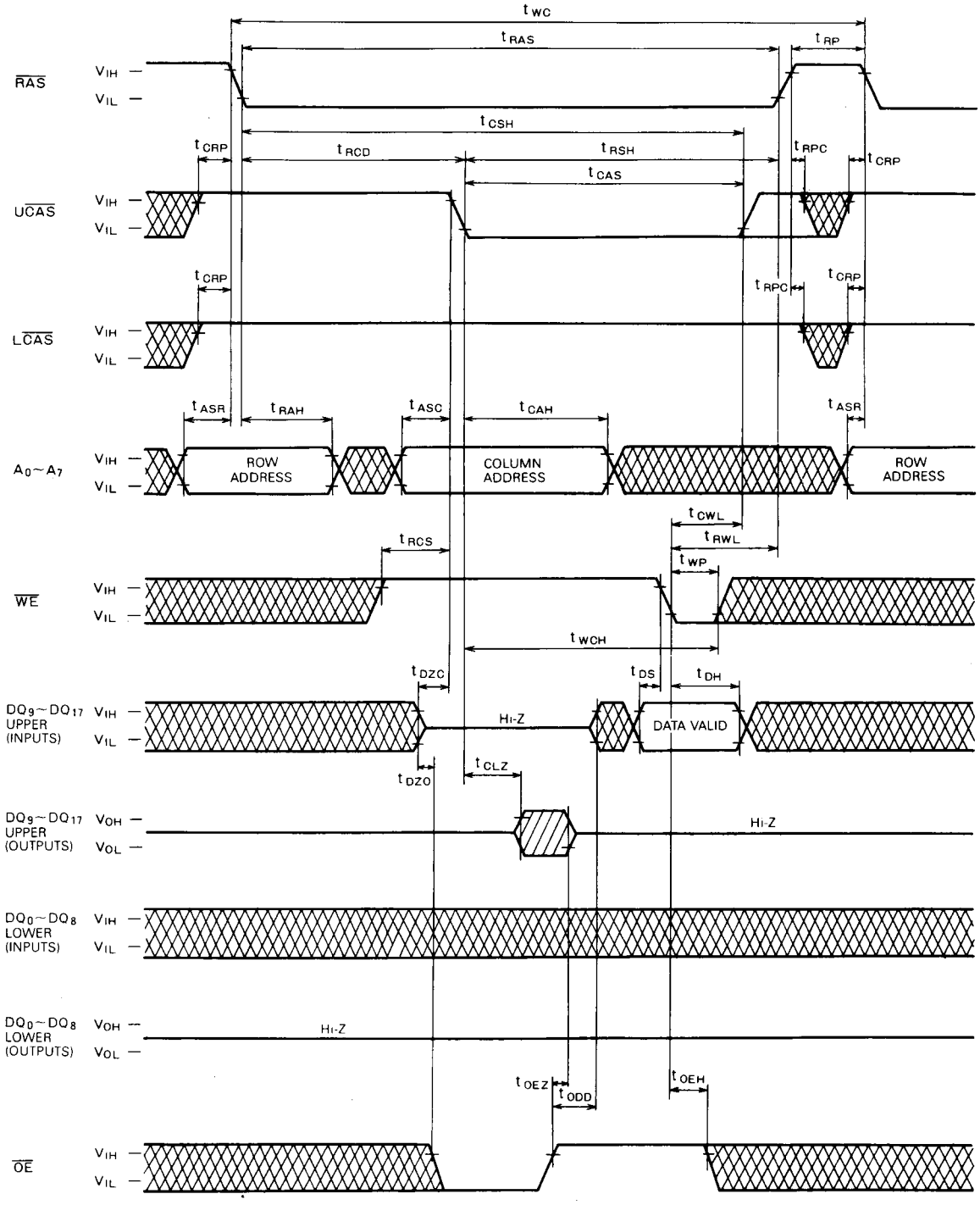
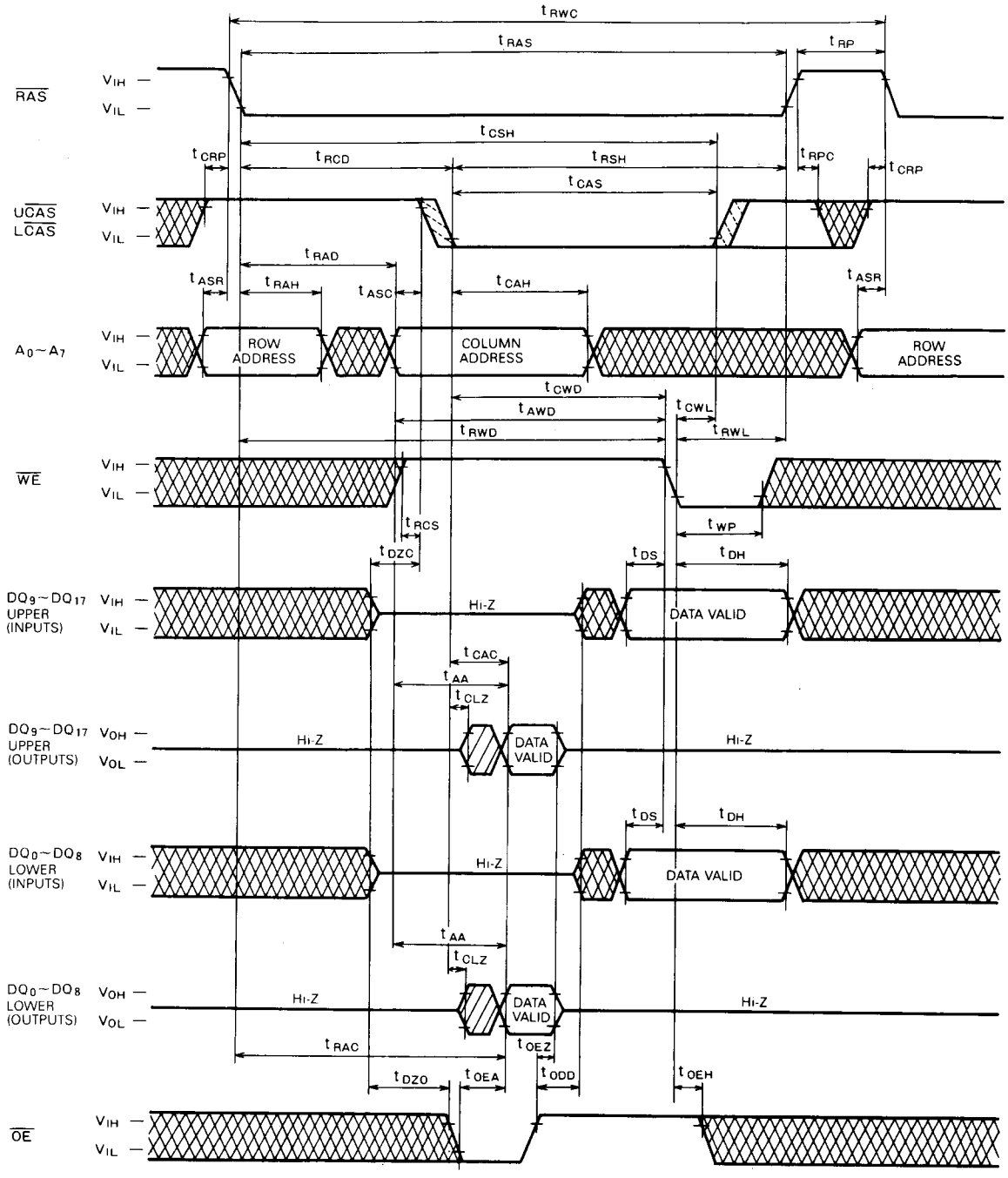
Delayed Write Upper (Lower) Byte Cycle



Read-Modify-Write Cycle



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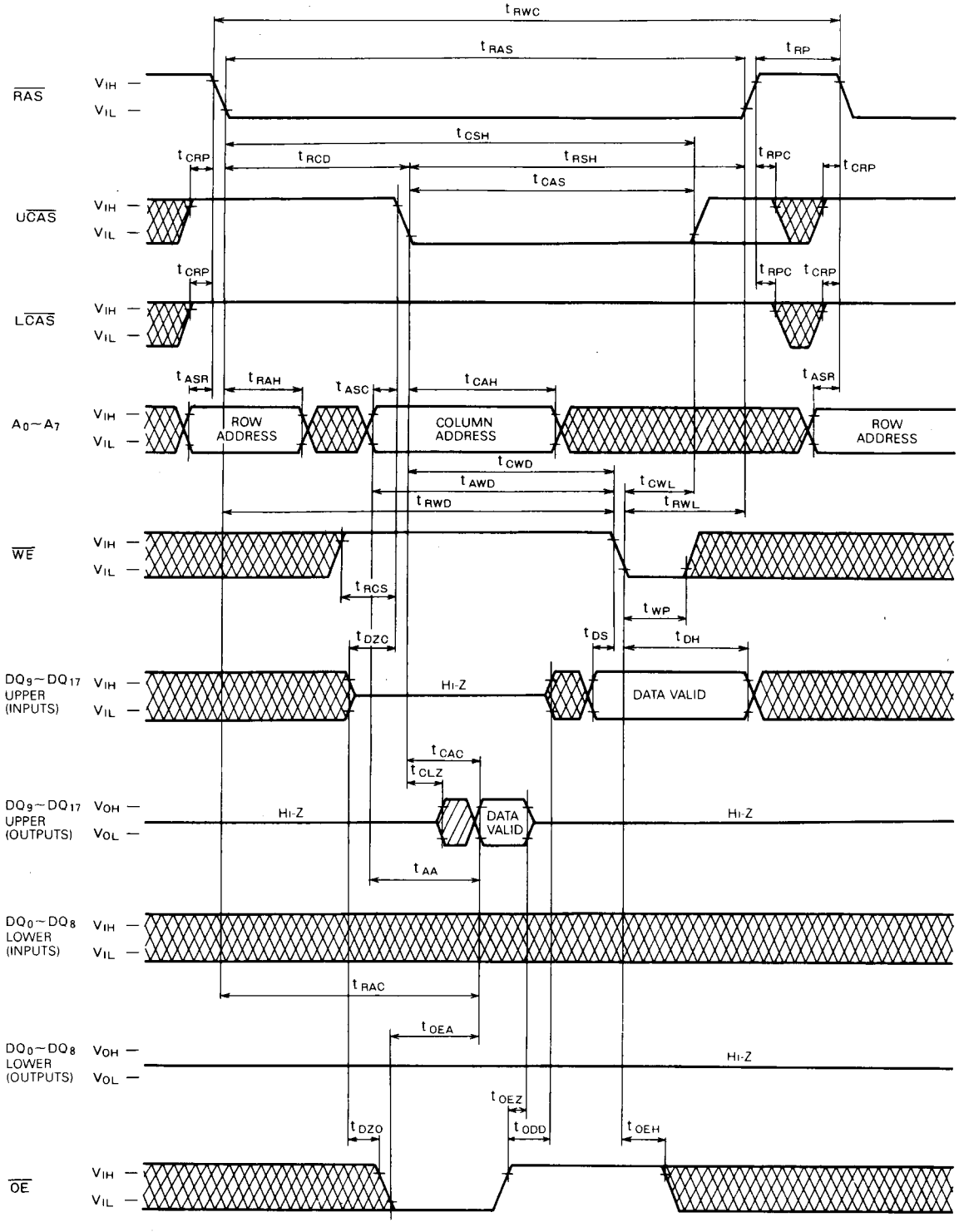
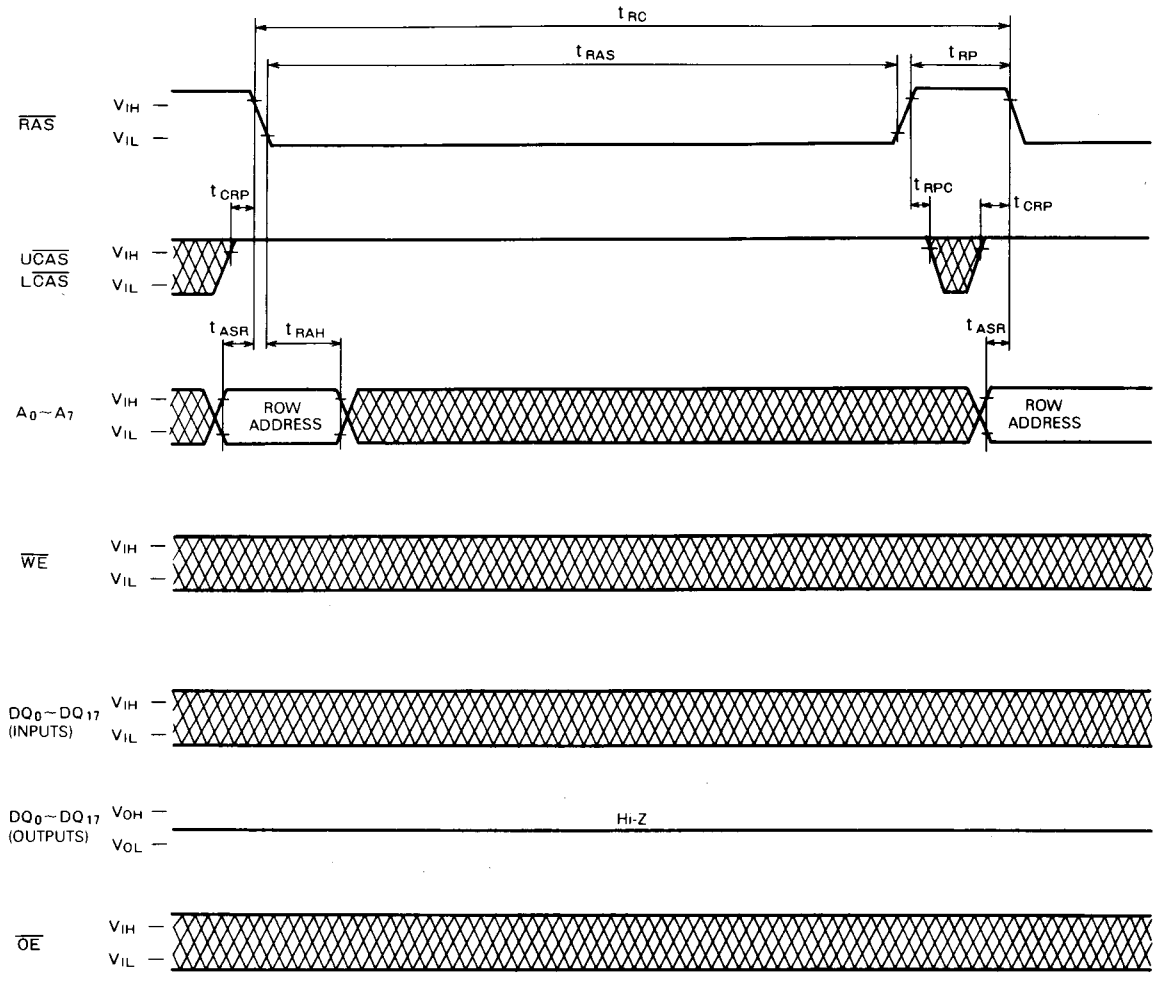
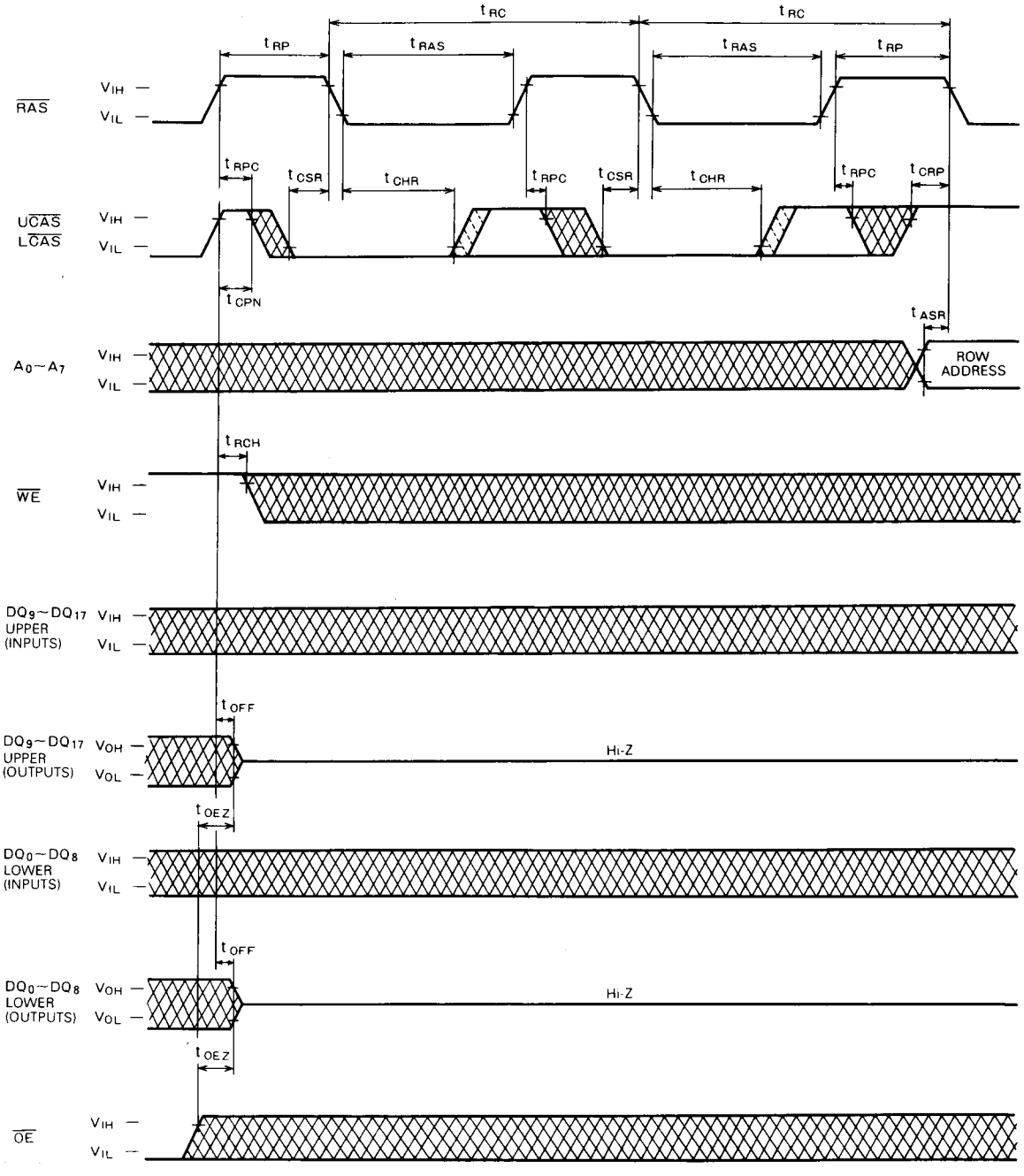
Read Modify Upper (Lower) Byte Cycle



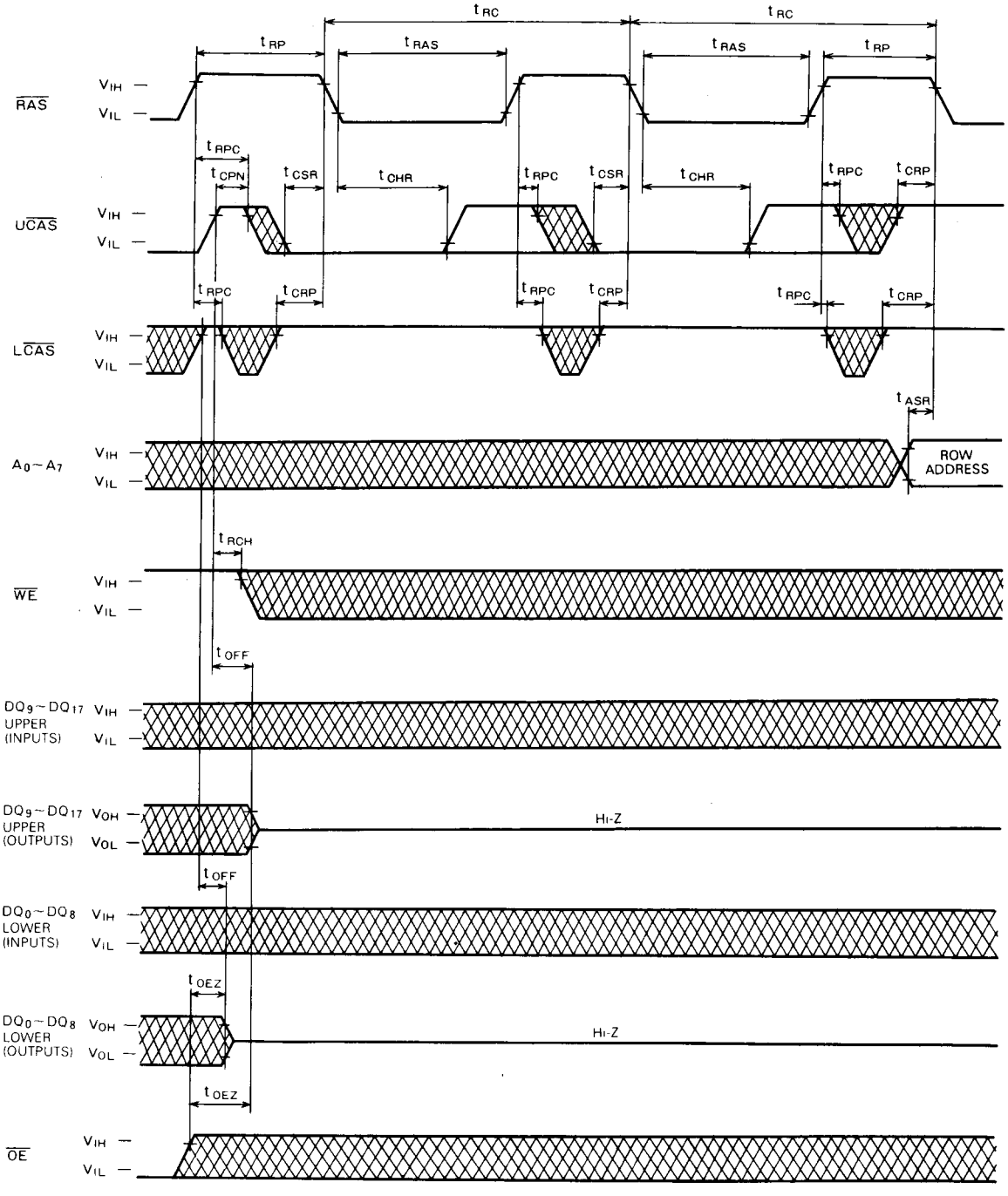
$\overline{RAS}$-only Refresh



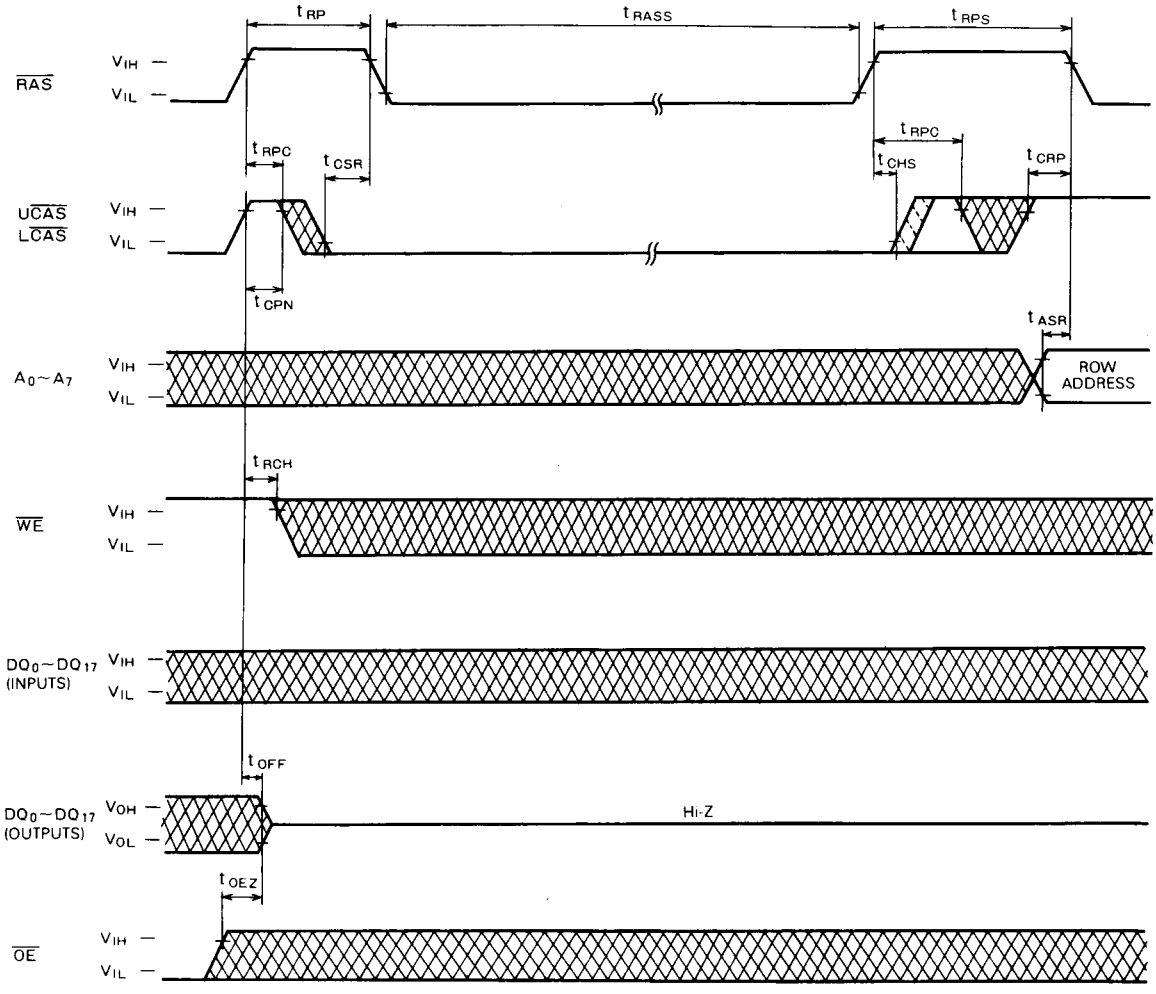
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Upper (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

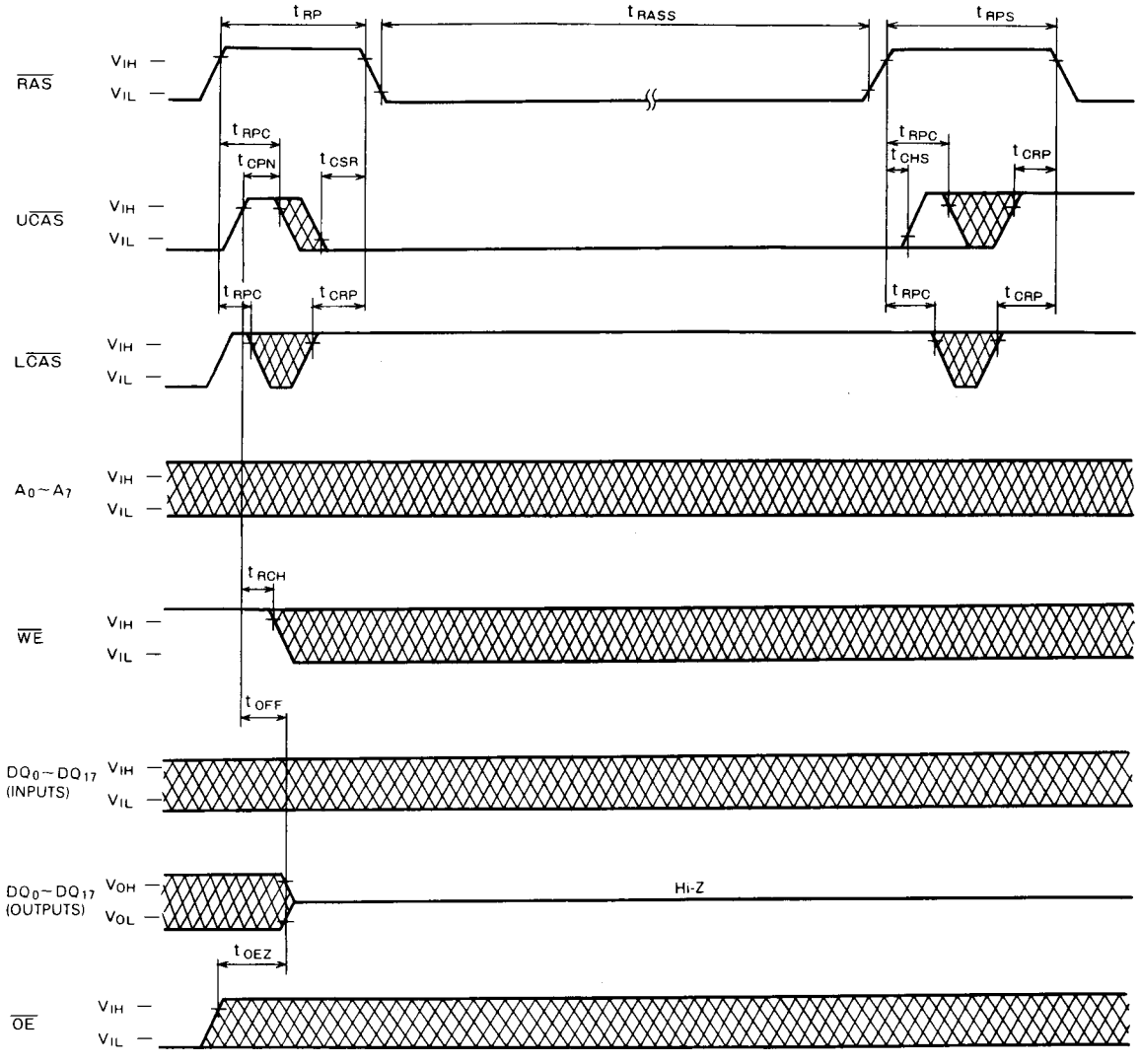


CBR Self-Refresh Cycle (Note 28)



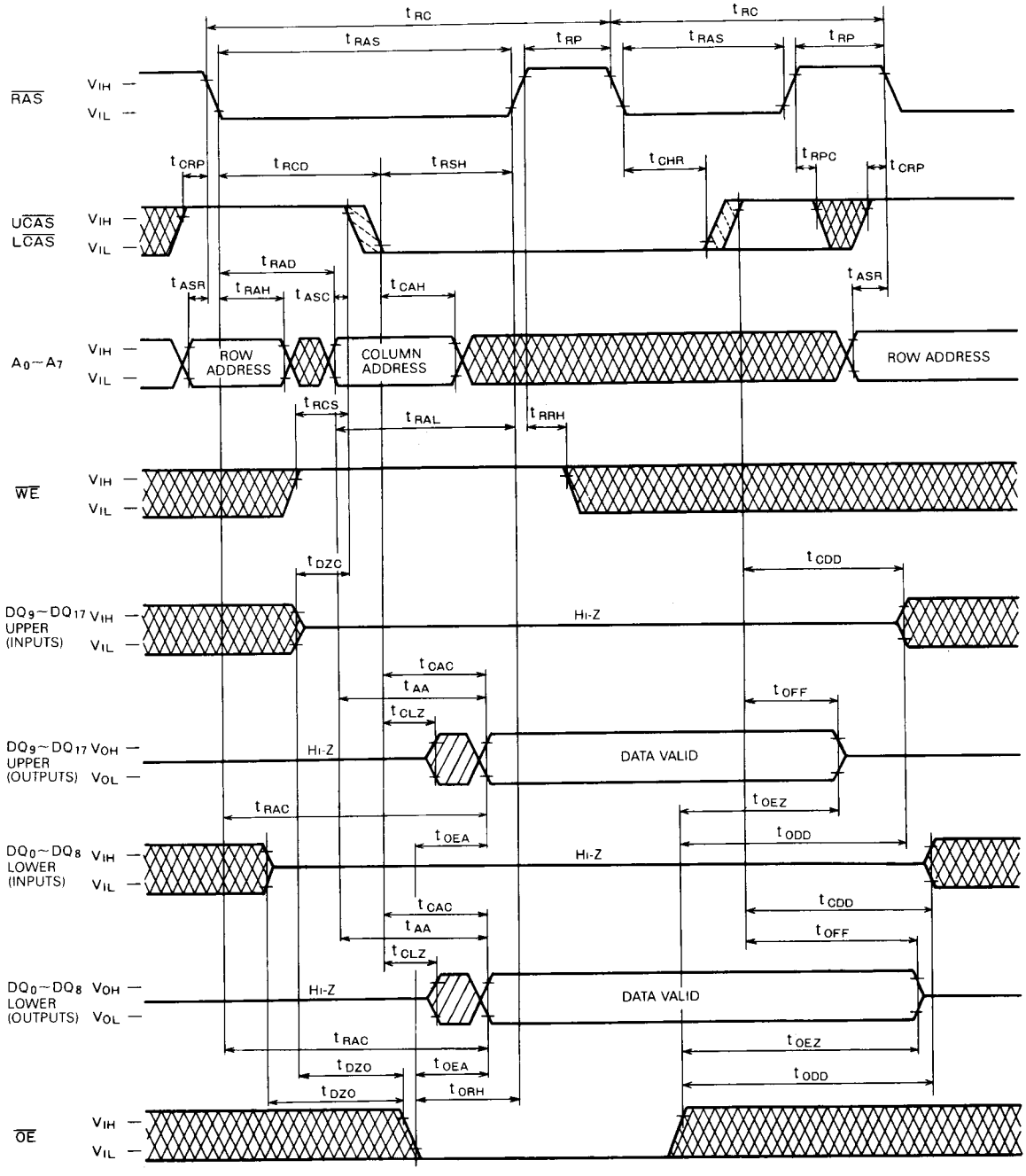
Note 28: 1. When the $\overline{RAS}$ only Refresh is used in the normal Read/Write cycle, the $\overline{RAS}$ Only Refresh cycles must be completed for all row of 256 cycles no later than 4ms after the CBR Self Refresh exit.
2. When the distributed CBR Refresh is used in the normal Read/Write cycles, the CBR Refresh cycles must start no later than 125μs after the CBR Self Refresh exit.
3. When the Burst CBR Refresh is used in the normal Read/Write cycles, the Burst CBR Refresh cycles must be completed for 256 cycles no later than 4ms after the CBR Self Refresh exit.

Upper (Lower) CBR Self Refresh Cycle (Note 29)



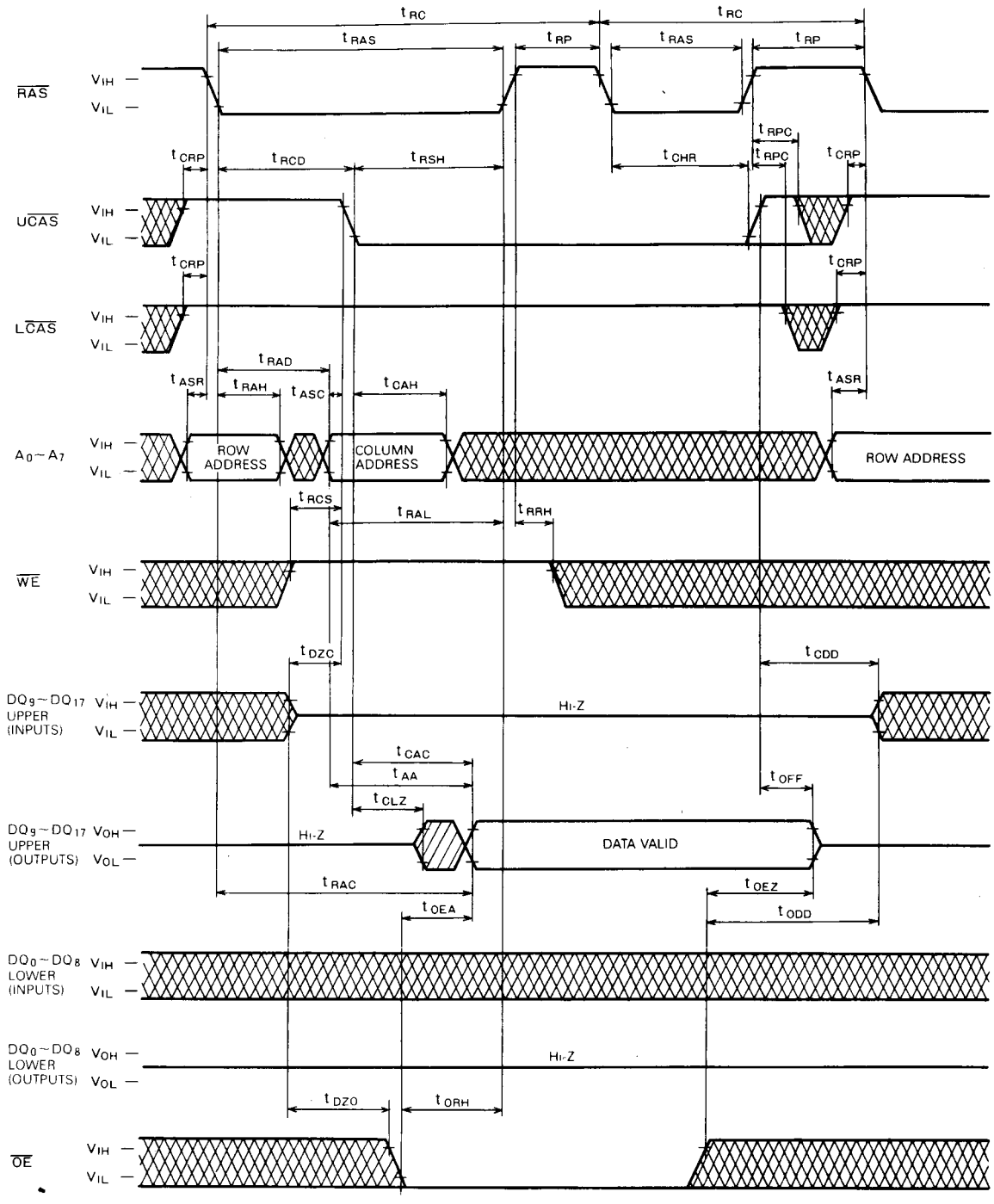
Note 29: 1. When the $\overline{RAS}$ only Refresh is used in the normal Read/Write cycle, the $\overline{RAS}$ Only Refresh cycles must be completed for all row of 256 cycles no later than 4ms after the CBR Self Refresh exit.
2. When the distributed CBR Refresh is used in the normal Read/Write cycles, the CBR Refresh cycles must start no later than 125μs after the CBR Self Refresh exit.
3. When the Burst CBR Refresh is used in the normal Read/Write cycles, the Burst CBR Refresh cycles must be completed for 256 cycles no later than 4ms after the CBR Self Refresh exit.

Hidden Refresh Cycle (Read) (Note 30)



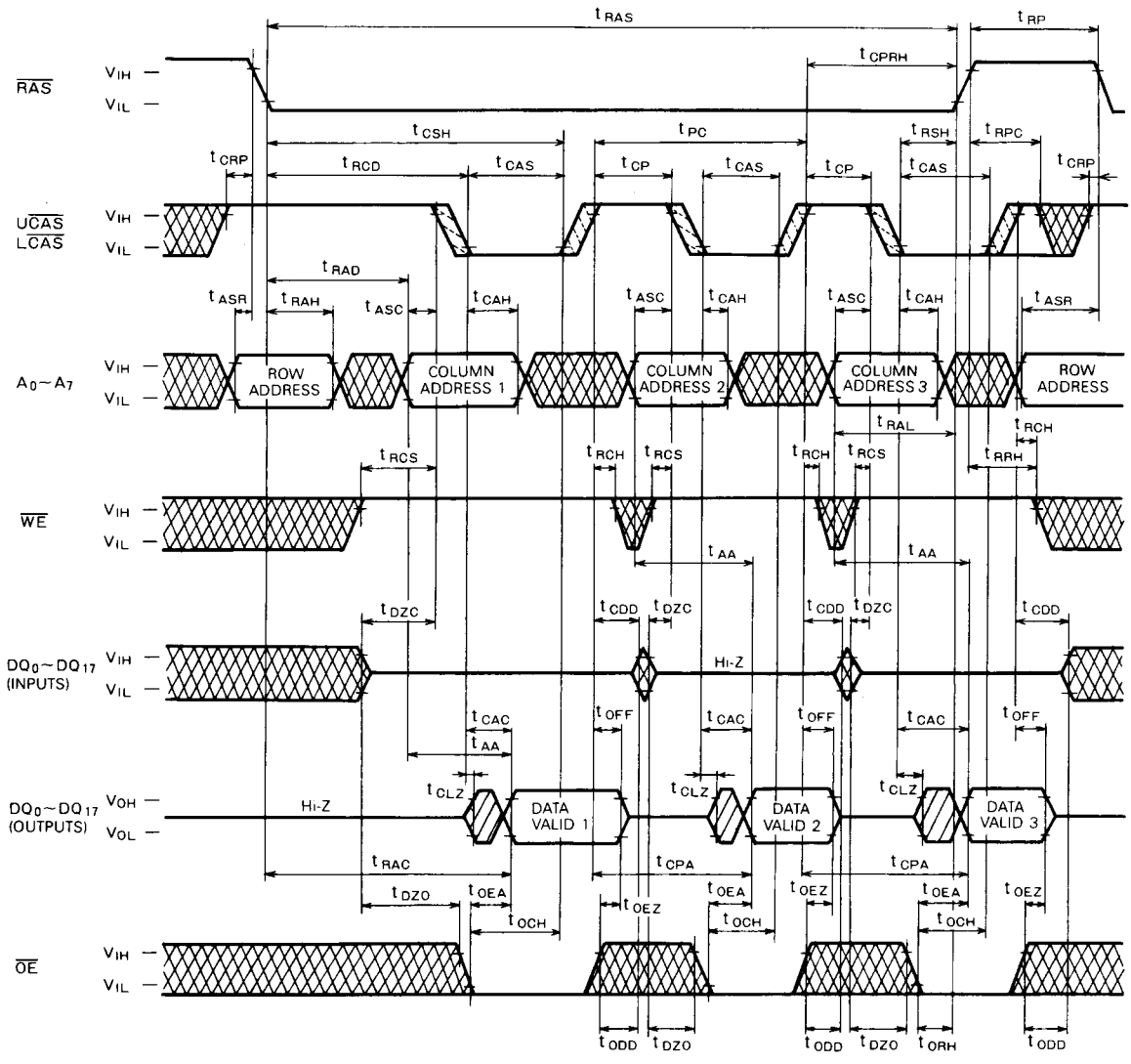
Note 30: Early write, delayed write, read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Hidden Refresh Cycle (Upper (Lower) Byte Read) (Note 31)

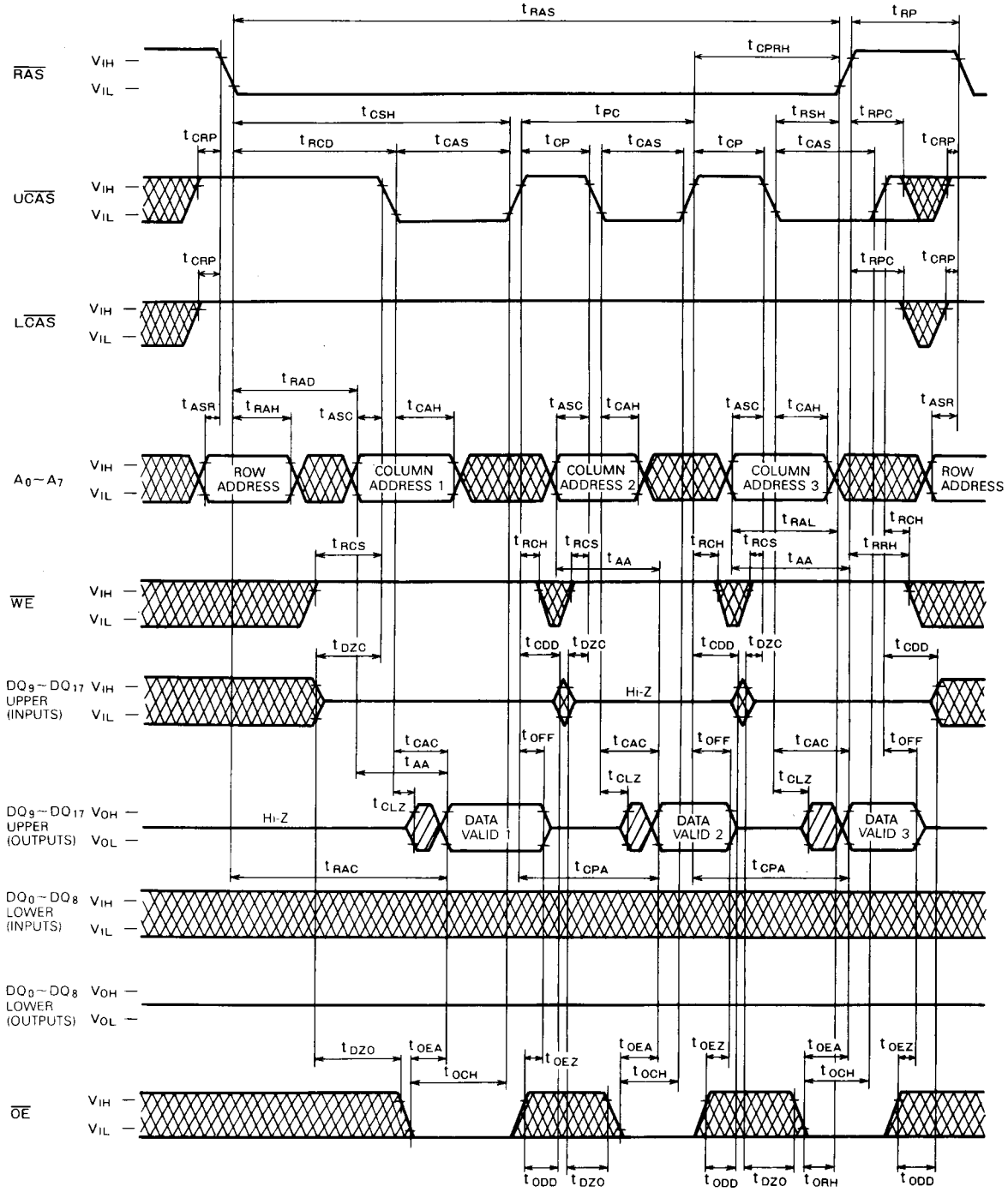


Note 31: Early write, delayed write, read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle



Fast Page Mode Upper (Lower) Read Cycle



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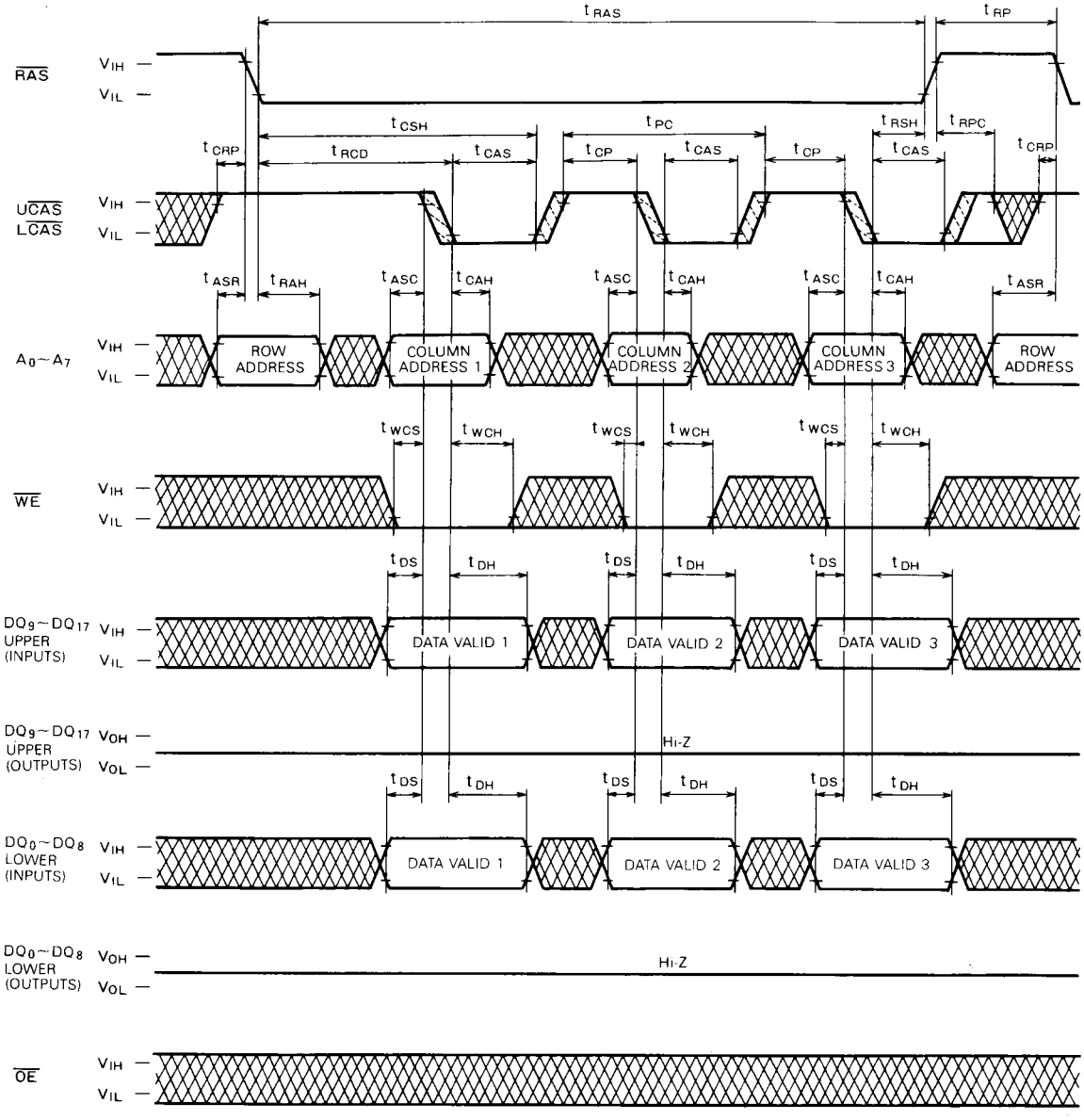
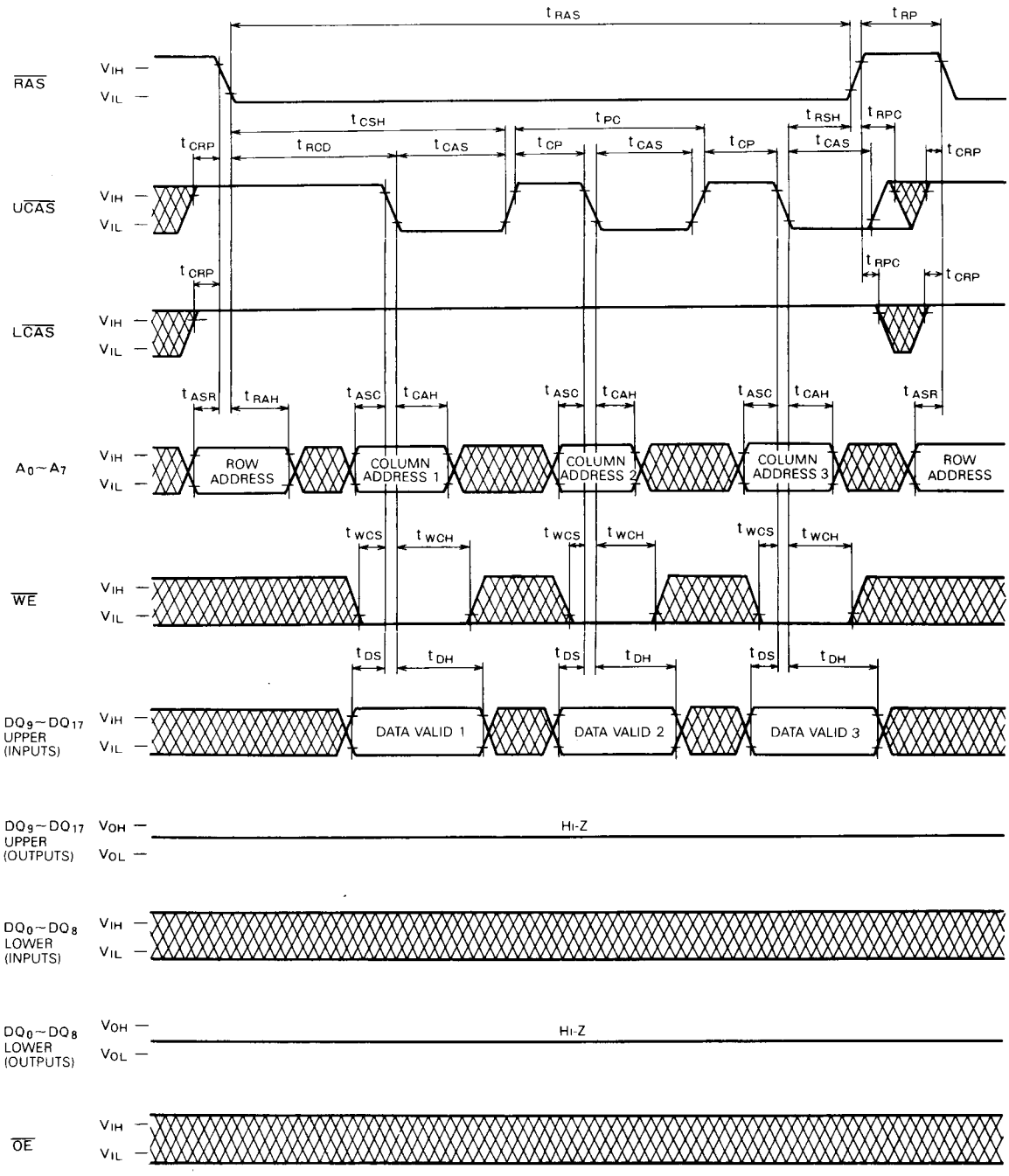
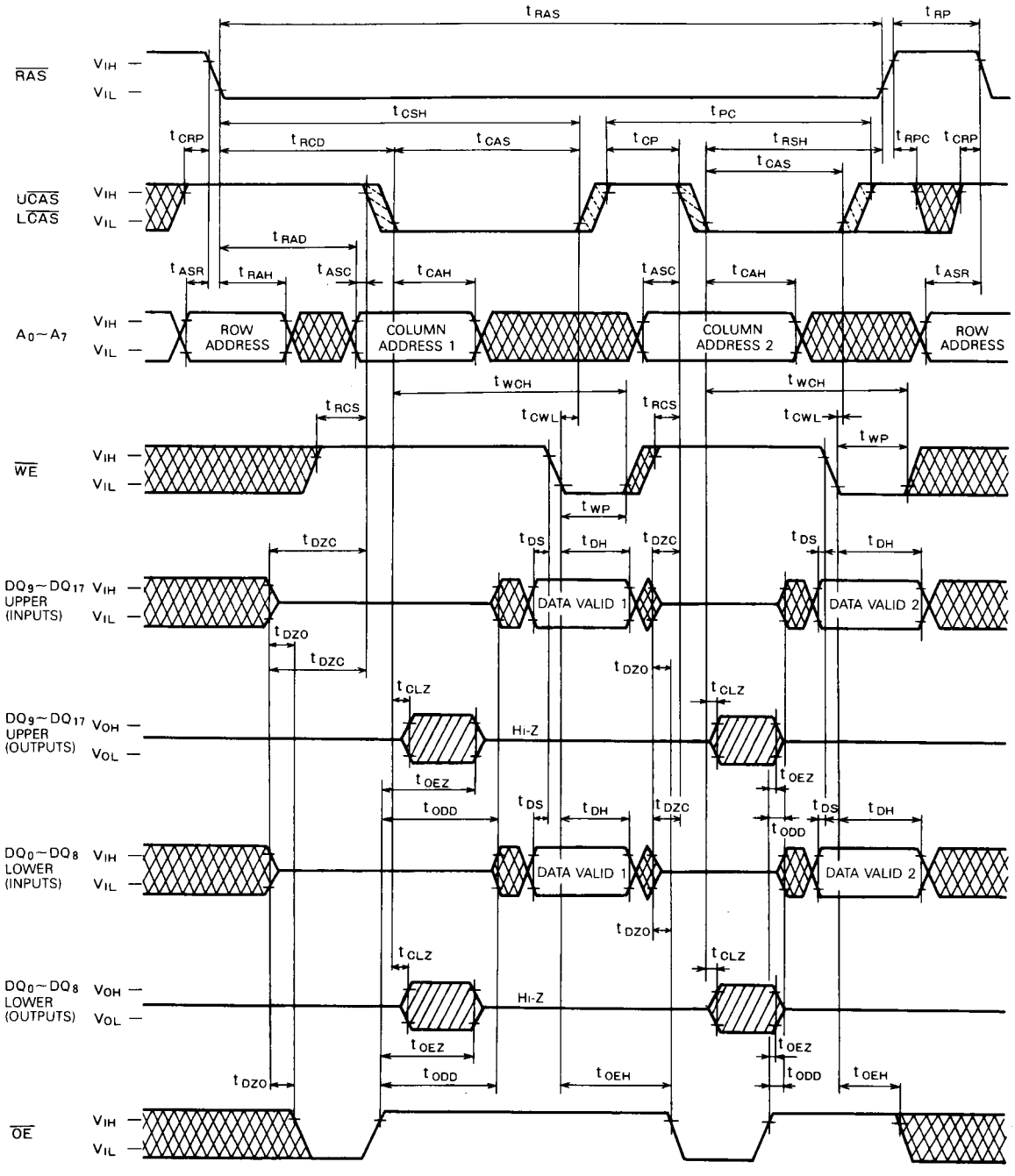
Fast Page Mode Early Write Cycle



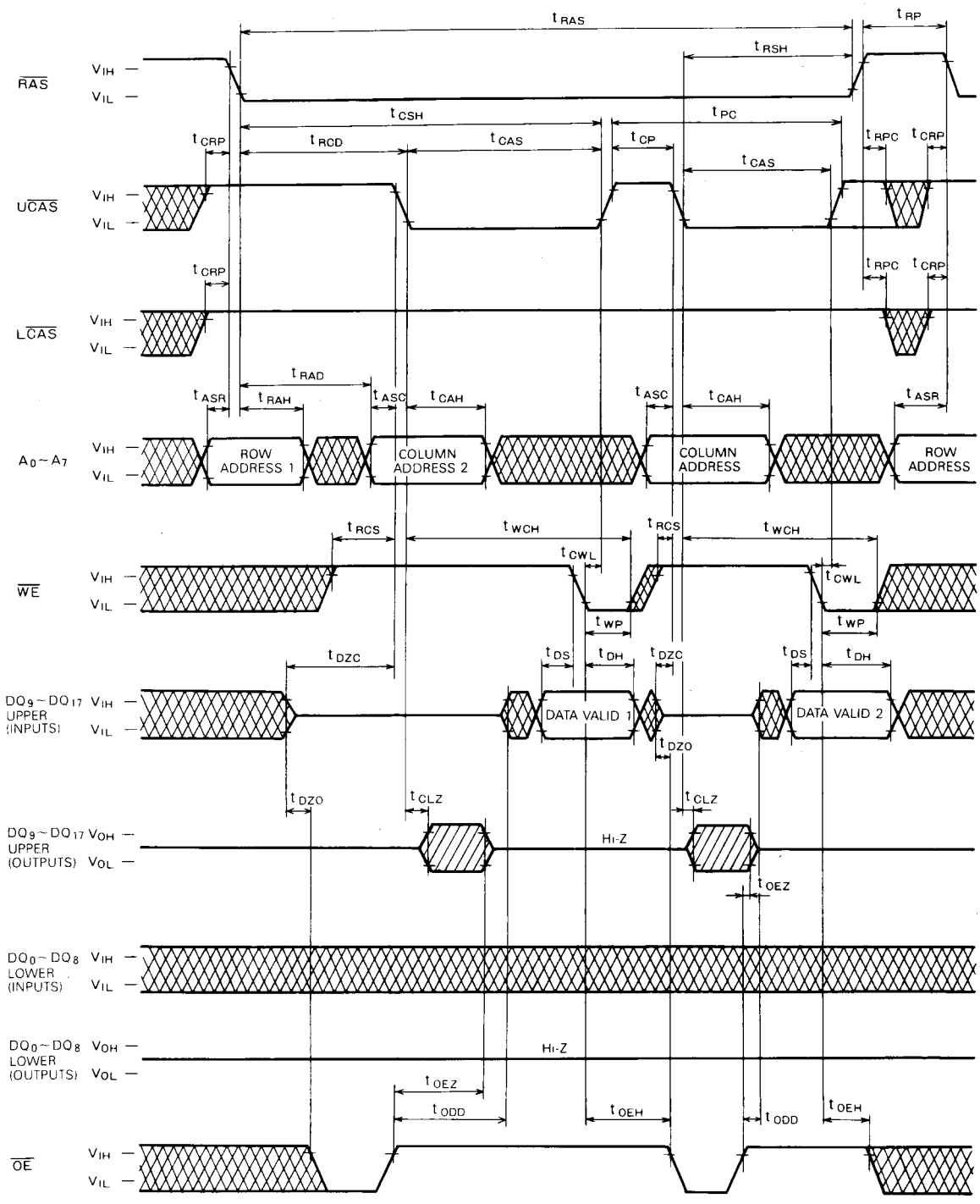
Fast Page Mode Upper (Lower) Byte Early Write Cycle



Fast page Mode Delayed Write Cycle



Fast Page Mode Upper (Lower) Byte Delayed Write Cycle



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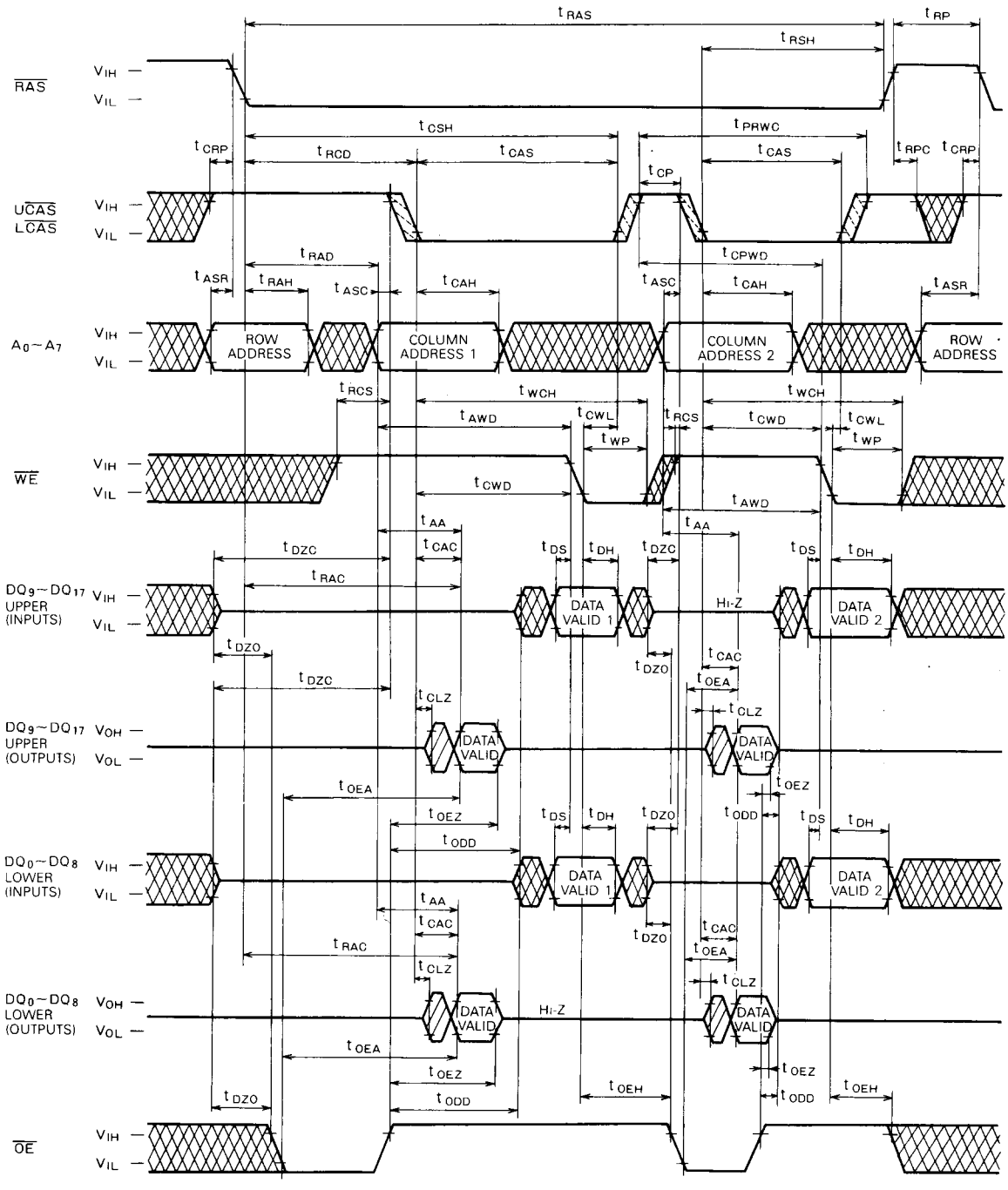
Fast Page Mode Read Modify Write Cycle



Fast Page Mode Read Modify Upper (Lower) Write Cycle