

MB838200B/BL

CMOS 8M-BIT MASK READ ONLY MEMORY

512K x 16 (1M x 8) CMOS MASK READ ONLY MEMORY

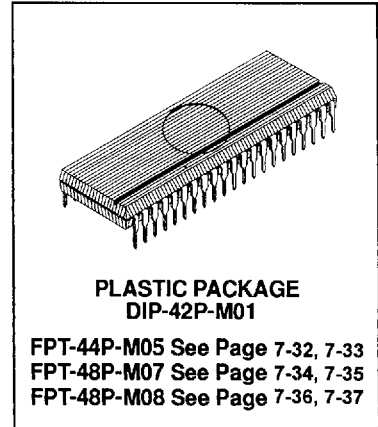
The Fujitsu MB838200B/BL is a CMOS Si-gate mask-programmable static read only memory organized as 524,288 words by 16 bits or 1,048,576 words by 8 bits.

All pins are TTL-compatible and 3-state output level. The device is full-static operatable (i.e. no need of clock signal) with a single +5V power supply. Also, the MB838200BL can be used with a single +3V power supply which is required for battery powered applications.

The MB838200B/BL is designed for applications such as character generator and program storage which require large memory capacity and high-speed/low-power operation.

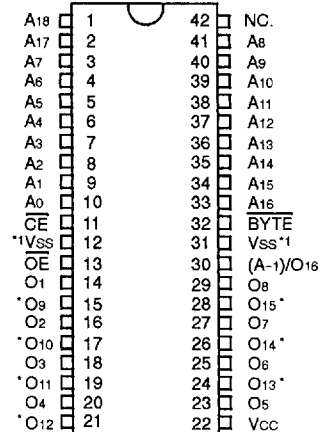
The memory organization of MB838200B/BL is configurable between 16 bits and 8 bits by BYTE pin.. (ex. The system using 8 bits CPU and 16 bits CPU can use common data on the same chip.)

- Organization: 524,288 words x 16 bits
1,048,576 words x 8 bits
- Access time: 120ns max. @V_{CC} = 5V (MB838200B)
200ns max. @V_{CC} = 3V (MB838200BL)
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5V power supply (MB838200B)
Single +3V power supply (MB838200BL)
- Power dissipation: 275mW max. (Active) @V_{CC} = 5V (MB838200B)
82.5mW max. (Active) @V_{CC} = 3V (MB838200BL)
- 42-pin Plastic DIP: Suffix: P
- 44-pin Plastic SOP: Suffix: PF
- 48-pin Plastic Thin Small Outline Package (TSOP):
Suffix: PFTN(Normal Bend)
Suffix: PFTR(Reversed Bend)



PIN ASSIGNMENT

(TOP VIEW)



This pin (*) is High-Z, the device is used 8 bits.

*1: All pins should be connected.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0 *	V
Input Voltage	V _{IN}	-0.5 to V _{CC} +0.5 *	V
Output Voltage	V _{OUT}	-0.5 to V _{CC} +0.5 *	V
Temperature Under Bias	T _{BIAS}	-10 to +85	°C
Storage Temperature Range	T _{STG}	-45 to +125	°C

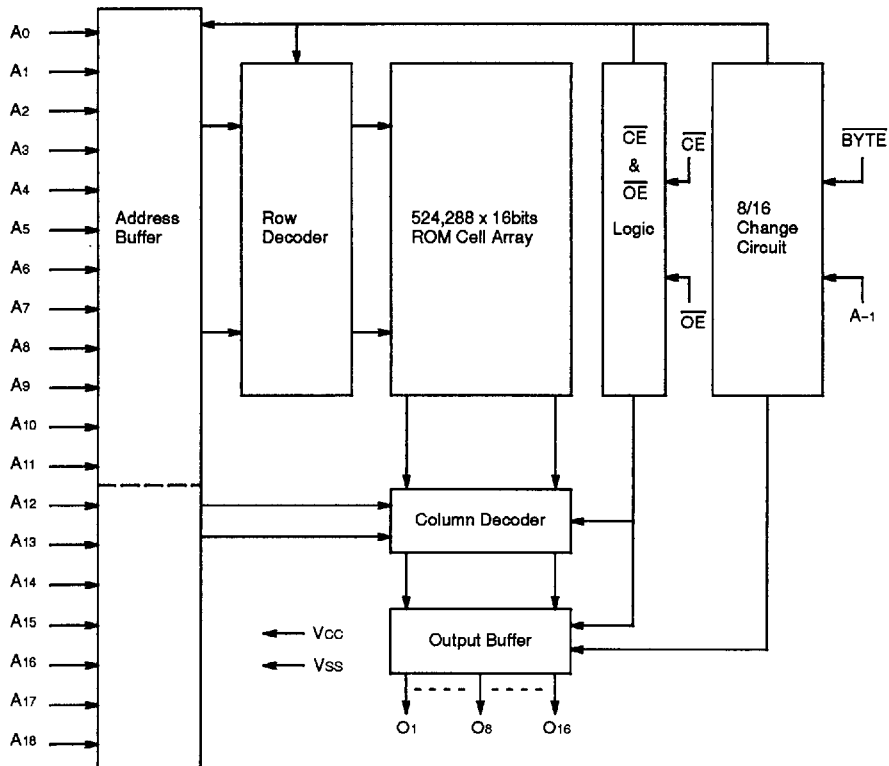
* Referenced to GND

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 — MB838200B/BL BLOCK DIAGRAM



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OUTPUT MODE SELECTION A-1 is LSB.

BYTE	O1 to O8	O9 to O15	(A-1)/O16
H	O1 to O8	O9 to O15	O16
L	O1 to O8	High-Z	A-1 ("L" INPUT)
L	O9 to O16	High-Z	A-1 ("H" INPUT)

TRUTH TABLE

\overline{CE}	\overline{OE}	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	NOT SELECTED	High-Z	STANDBY
L	H	NOT SELECTED	High-Z	ACTIVE
L	L	SELECTED	DOUT	ACTIVE

CAPACITANCE (TA=25° C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (VOUT=0V)	COUT			15	pF
Input Capacitance (VIN=0V)	CIN			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	MB838200B			MB838200BL			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	4.5	5.0	5.5	2.7	3.0	3.3	V
Input Low Voltage	V _{IL}	-0.3		0.8	-0.3		0.6	V
Input High Voltage	V _{IH}	2.2		V _{CC} +0.3	V _{CC} ×0.7		V _{CC} +0.3	V
Ambient Temperature	T _A	0		70	0		70	°C

DC CHARACTERISTICS

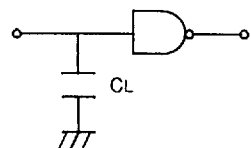
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	MB838200B			MB838200BL			Unit
			Min	Typ	Max	Min	Typ	Max	
Active Supply Current	$\overline{CE}=V_{IL}$, Minimum Cycle Output = Open	I _{CC}			50			25	mA
Standby Supply Current	$\overline{CE}=V_{IH}$	I _{SB1}			1			0.5	mA
	$\overline{CE}=V_{CC}=V_{IH}$, V _{IN} =GND or V _{CC}	I _{SB2}			10			10	μA
Input Leakage Current	V _{IN} =0 to V _{CC}	I _{LI}	-10		10	-10		10	μA
Output Leakage Current	$\overline{CE}=V_{IH}$ $\overline{OE}=V_{IH}$	I _{LKO}	-10		10	-10		10	μA
Output High Voltage	I _{OH} =-400μA	V _{OH}	2.4			2.0			V
Output Low Voltage	I _{OL} =2.1mA	V _{OL}			0.4				V
	I _{OL} =1.0mA						0.4		

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Fig.2 -- AC TEST CONDITIONS

- Input Pulse Level : 0.6 to 2.4V @V_{CC} = 5V (MB838200B)
0.4 to V_{CC}×0.8V @V_{CC} = 3V(MB838200BL)
- Input Pulse Rise and Fall Time : t_r=5ns
- Timing Reference Levels : Input: V_{IL}=0.8V, V_{IH}=2.2V / Output: V_{OL}=0.8V, V_{OH}=2.2V @V_{CC} = 5V (MB838200B)
Input: V_{IL}=0.6V, V_{IH}=V_{CC}×0.7V / Output: V_{OL}=1.2V, V_{OH}=1.8V @V_{CC} = 3V (MB838200BL)
- Output Load : 1 TTL Gate and 100pF



AC CHARACTERISTICS

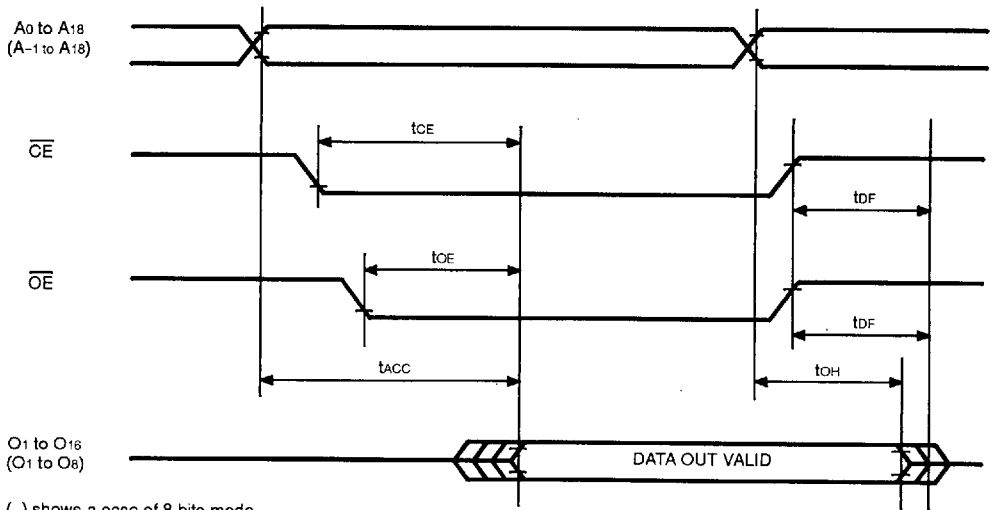
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	MB838200B		MB838200BL		Unit
			Min	Max	Min	Max	
Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	t _{ACC}		120		200	ns
Chip Enable Access Time	$\overline{OE}=V_{IL}$	t _{CE}		120		200	ns
Output Enable Access Time ^{**1}		t _{OE}		60		120	ns
Output Disable Time ^{**2}		t _{DF}		50		60	ns
Output Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	t _{OH}	0		0		ns

*1: When continuously switching between 3V operation and 5V operation, during Vcc transition the \overline{CE} should be High state (Standby mode).

*2: t_{DF} is specified by either of \overline{CE} or \overline{OE} changing to High earlier.

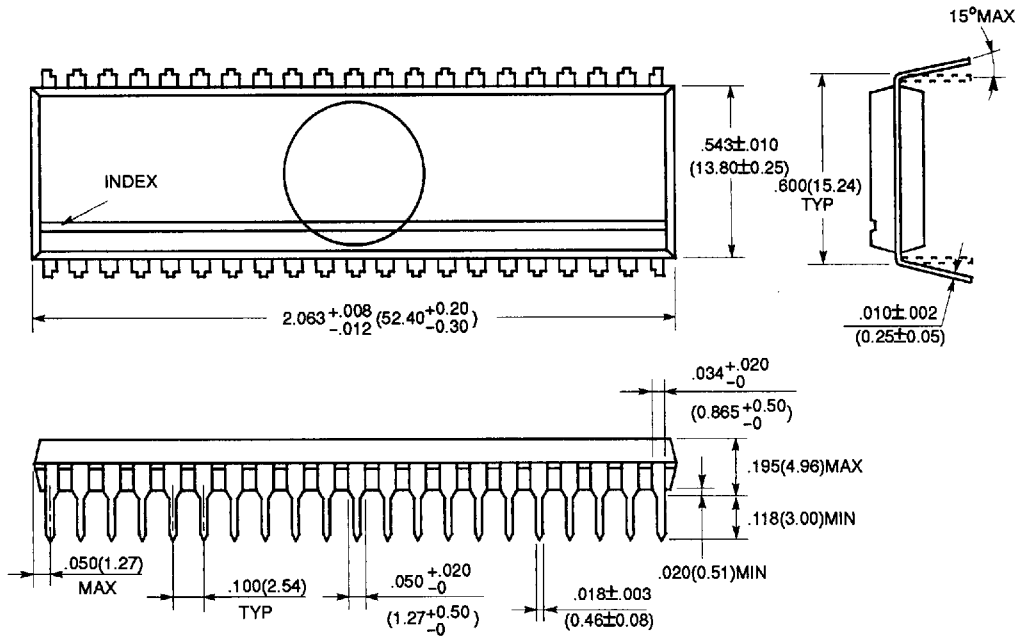
TIMING DIAGRAM



PACKAGE DIMENSIONS

(Suffix: P)

42-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42P-M01)



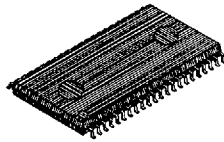
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Dimensions in
inches (millimeters)

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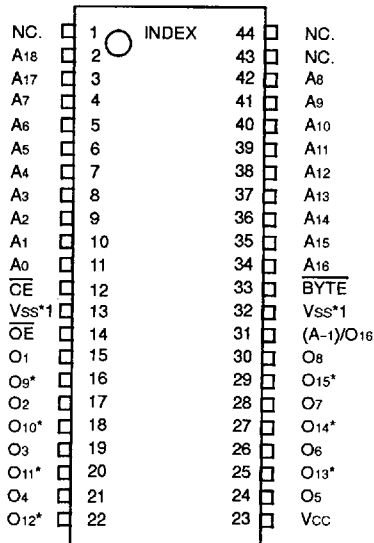
PACKAGE DIMENSIONS (Continued)

(Suffix: PF)



PLASTIC PACKAGE
FPT-44P-M05

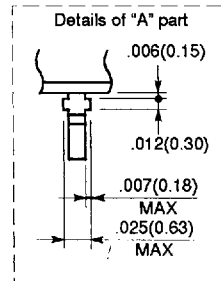
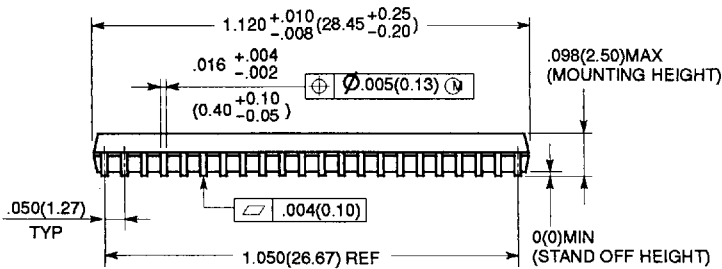
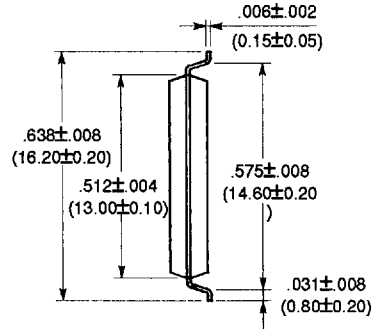
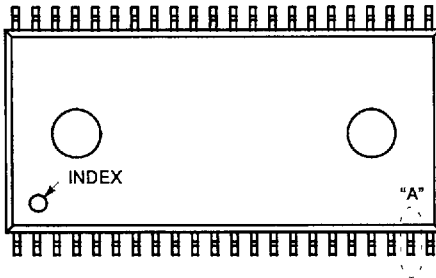
PIN ASSIGNMENT



This pin (*) is High-Z, the device is used 8 bits.
*1: All pins should be connected.

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44-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-44P-M05)

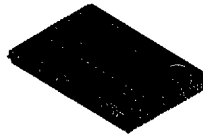


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Dimensions in
inches (millimeters)

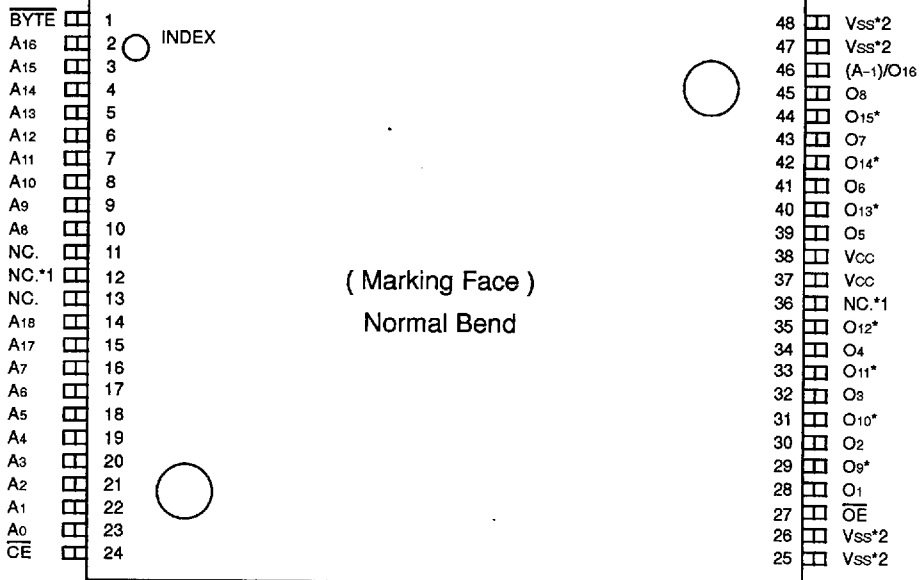
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)



PLASTIC PACKAGE
FPT-48P-M07

PIN ASSIGNMENT



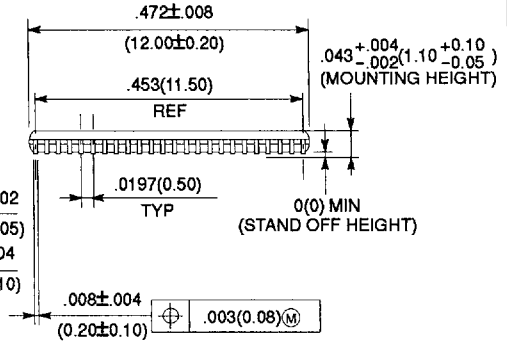
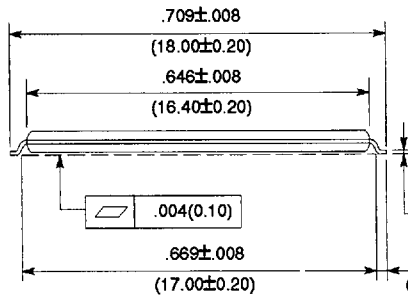
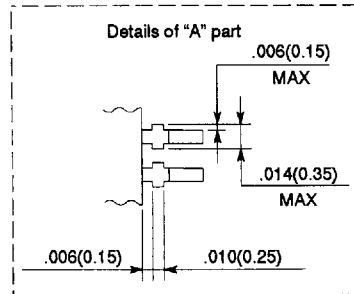
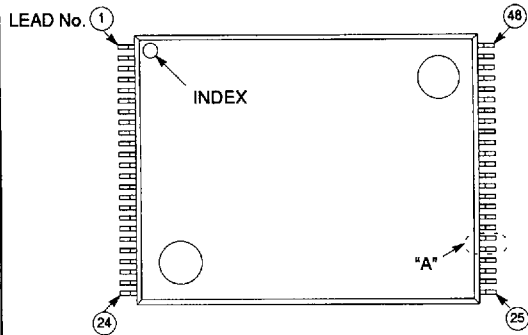
This pin (*) is High-Z, the device is used 8 bits.

*1: If the voltage is applied externally, it should be connected to Vss.

*2: All pins should be connected.

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48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M07)

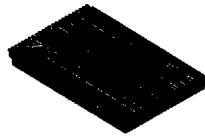


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Dimensions in inches (millimeters)

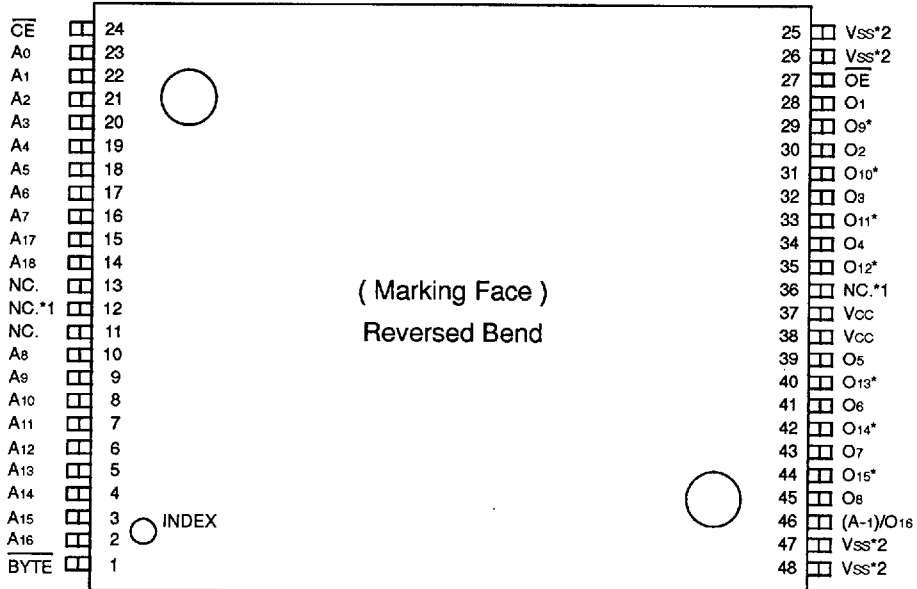
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



PLASTIC PACKAGE
FPT-48P-M08

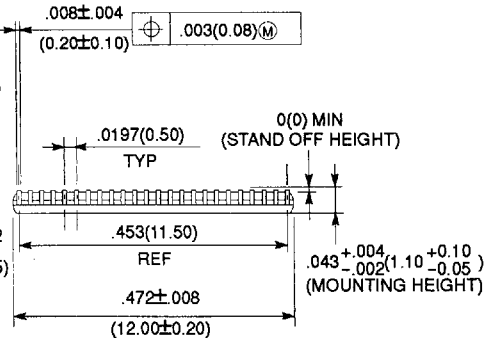
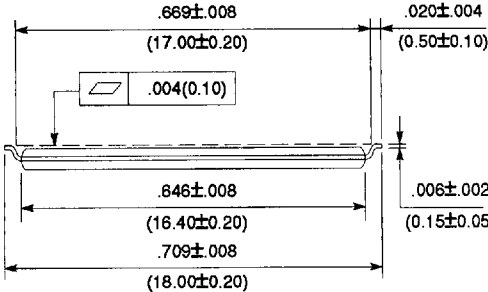
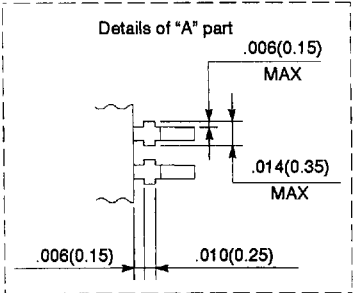
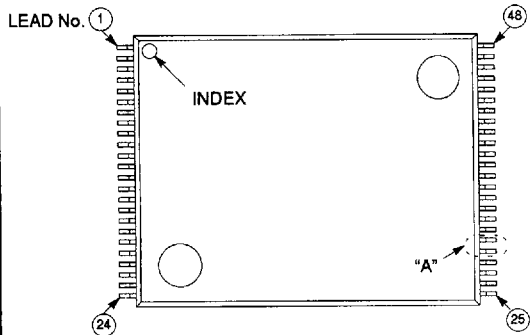
PIN ASSIGNMENT



This pin (*) is High-Z, the device is used 8 bits.
 *1: If the voltage is applied externally, it should be connected to Vss.
 *2: All pins should be connected.

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48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M08)



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Dimensions in inches (millimeters)