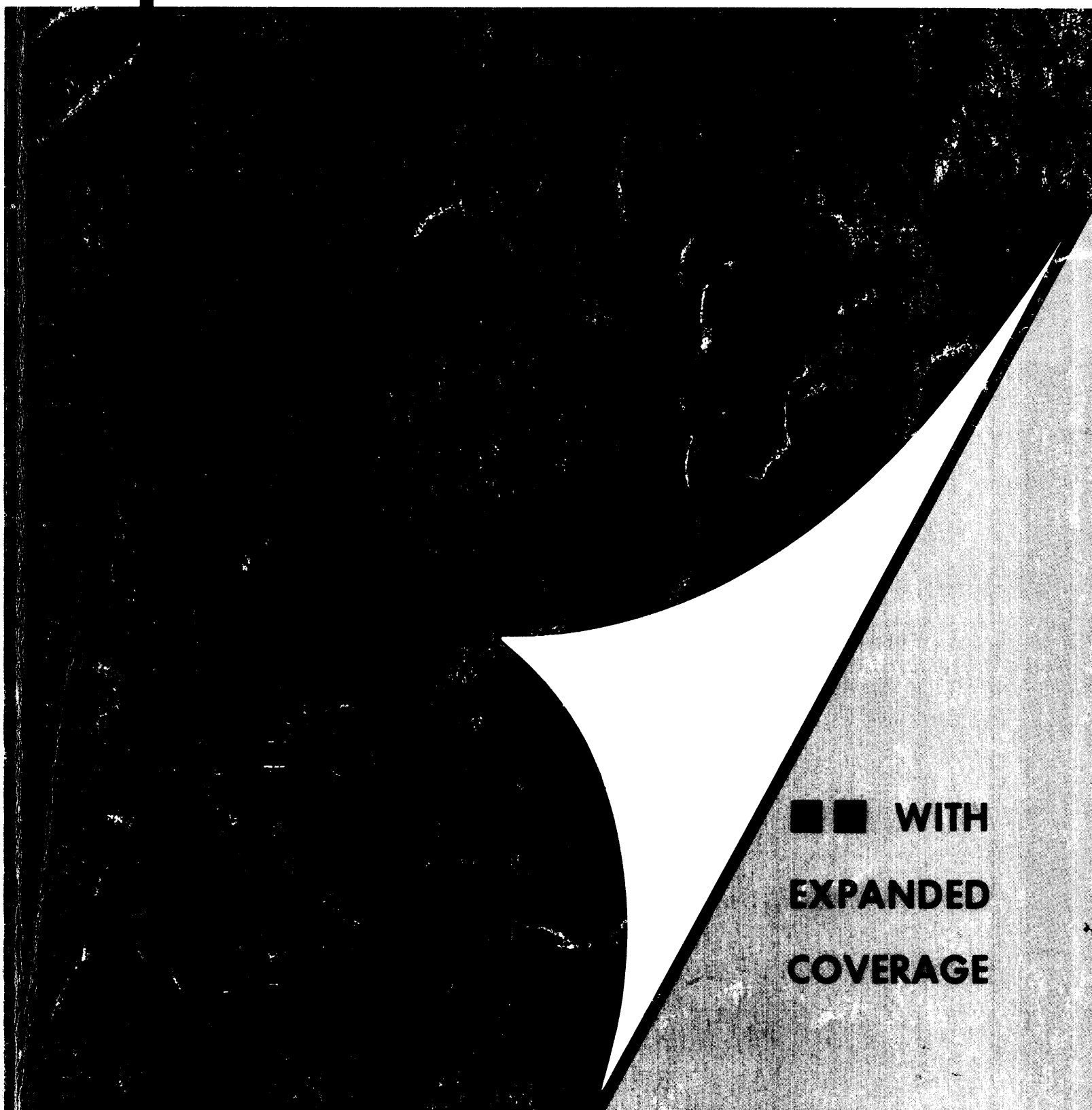
AUERBACH Guide to



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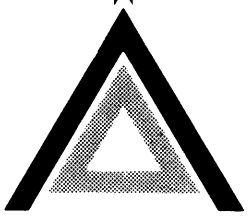
AUERBACH

Guide to Minicomputers

The material contained in this publication is included in *AUERBACH Computer Technology Reports*, an analytic reference service that provides comprehensive coverage of the information processing industry.



AUERBACH®
Publishers Inc.
philadelphia
penna. 19107

Standard Book Number 0-87769-227-0
Library of Congress Card Number 76-10108
Printed in the United States of America

First Edition April, 1975
First Revision, April, 1976

The information contained herein has been obtained from reliable sources and has been evaluated by experienced technical personnel. Due to the rapidly changing nature of the technology and equipment, however, the information cannot be guaranteed.

Published by AUERBACH Publishers Inc., Pennsauken NJ 08109

Printed in the United States of America

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PREFACE

Although "dispersal of computer power" is currently a popular phrase, minicomputers have been dispersing computer power for more than 8 years. Sophisticated users were quick to find the minicomputer an attractive alternative to waiting in line for a batch processing system. Minicomputers are not only cheaper and faster than their general-purpose cousins, but also technologically more advanced. New technology adds more power, lowers costs, and increases markets. Because they were first used in process control applications, in laboratories, and for communications, minicomputers are real-time and on-line oriented. After 8 years, the marginal manufacturers have been shaken out; only well-managed companies that produce substantial products remain.

This **AUERBACH Guide to Minicomputers** presents an introduction to minicomputers and a system overview of the major minicomputers on the market today. Some manufacturers, such as Digital Equipment, produce two or three lines of minis. Others produce only one broad line. Generally the minicomputer manufacturers call themselves "toolmakers." They produce the hardware and software tools that others use to solve problems in a particular application.

The **AUERBACH Guide to Minicomputers** presents information in several levels of detail. Special individual reports devoted to general-purpose minicomputers, microcomputers, and microprocessors and process control systems explain how to evaluate and select your own system. Each major minicomputer and some minor ones are covered in a separate analytical report.

You can look through the Table of Contents for a system which interests you. If you want a quick view of the minicomputers available on today's market, check the search chart. For more detailed information on a particular manufacturer's components, go to the individual product reports. A price list is included as part of each report. When you have evaluated the minicomputers and selected the ones that seem most likely to fulfill your needs, consult the list of suppliers for addresses and phone numbers.

This selection guide presents the following information:

- Device Reports
  - — Text: describes characteristics of various minicomputer systems. Each product report begins with a summary and then discusses configuration, software, design features, performance, maintenance and company history.
  - — Product Specifications: a chart that summarizes information on the components' performance, capacity and design.
  - — Price Data: price list of equipment supplied.
- Search Chart — provides a quick way to compare the minicomputers covered in the product reports. Lists major processor features, peripheral devices and programming languages for all minicomputers available on the market. The reports are a selection of this material.
- Suppliers: — an alphabetical directory of vendors.

PREFACE (Cont)

To use the guide effectively, it is important to know what information is contained in each product report. Separate sections discuss a device's advantages and marketing, configuration possibilities, facilities requirements, performance characteristics, and service. The company's background is also covered.

The Summary or Overview gives the name of the company marketing the system, its special capabilities or unique features, and their significance to the user, as well as the user group most likely to benefit from a particular minicomputer. The Performance section evaluates the system's competitive position, performance capabilities, special strengths and weaknesses, and its impact on other systems in the marketplace. Users are interviewed to show how effective the system is in operation. The company history is also included, telling the date the firm was established and its major business, and noting the growth of its minicomputer line.

The Configuration Guide identifies the major system components, states their performance and interface requirements, and lists available options. This section also gives information on capacities of main and auxiliary storage, data structure and speeds of input/output devices.

The Software section identifies the major software available to the minicomputer under consideration. This includes discussions of the applications software offered by the vendor.

Since maintenance is another important aspect in selecting a minicomputer, a section of each report specifies the company providing maintenance and its experience.

For selected major minicomputer systems, the **Guide to Minicomputers** includes the Detail Report that also appears in the General-Purpose Minicomputers segment of the updated **AUERBACH Computer Technology Reports** library service. The Detail Report provides expanded information in the following areas: mainframe, memory, input/output control, peripherals, data communications and software.

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OVERVIEW

Process control is the automatic handling of matter or energy, and its modification by chemical or physical means to yield the products or results desired at a profit. Process control computers are electronic digital computers functioning in a process control environment. (The term process control itself is somewhat redundant, inasmuch as process implies control; we therefore will speak of a control computer.)

Digital computers were first applied to the automatic control of industrial processes in 1958. Early applications included chemicals, steel, petroleum refining, paper, electric power, and cement. Current uses are in satellite control, missile launches, pipelines, intensive care hospital units, television networks, data acquisition-reduction systems, automatic testing, bridge and traffic control, food packaging, postal cancellation, and laboratory automation. In each instance, the introduction of the electronic digital computer began a trend away from older, more manual forms of control such as human resources, controllers, data loggers, and analog computers. As processes became more complex and instruments more numerous, human operators were inundated with information. Digital computers have had an enormous effect on such systems, primarily because they can handle large amounts of information with far greater speed, accuracy, and flexibility than has previously been possible.

Computers used in the control of industrial processes are similar to business and scientific computers in that they benefit from technological advances such as integrated circuits. Control computers differ from their siblings in that they are more compact, cost less, can accept input directly from the process, and must operate continuously in most adverse conditions. For example, a business computer usually lives in a temperature- and air-controlled, dust-free environment. A control computer must withstand extreme ranges of temperature and humidity and often must ignore vibrations caused by nearby heavy machinery.

Business and scientific computers differ from control computers in the thought and planning preceding their installation. Control computer installations depend on a great deal of advanced engineering and analysis of hardware and applications software for design, installation, and programming. In most cases, advanced mathematical models are made by system engineers to determine the exact configuration to explore the range of operations and to exploit potential operational improvements. Planning generally consumes more than two years prior to installation. Once installed, the control computer must function almost immediately in an error-free manner. Experience has shown that success in a given installation is directly proportional to the size of the user's planning team, not to the vendor's support.

Such thorough planning is not the norm in a business or scientific environment where debugging may take up to 6 months or even longer before efficient processing occurs. The primary reason for this vast difference in planning techniques is that rerun time doesn't exist for a process that is on-line 24 hours a day.

Control applications can be discrete, continuous, semicontinuous, or batch and can be serviced by a single computer or a myriad of computers linked in a plantwide system. Functions can include the allocation of tasks to and the control of lesser computers; raw material operations; inventory maintenance; materials scheduling; future orders; and utilization of equipment capacity.

The components of a control system are basically the same as those of a business or scientific computer system: a main memory unit to store programs and data; a control unit to direct computations and switching; an arithmetic unit to perform calculations; and input-output units to communicate with the computer. In business and scientific computers as well as control computers, the control unit plus the arithmetic unit is called the central processing unit.

Unlike a business or scientific computer system, however, a control computer system is connected directly to sensing devices which measure product qualities, raw material characteristics, temperatures, flows, pressures, and other process conditions. Various signal converters change the signals from these sensing devices into a digital form that is usable by the computer. The devices or positioners in the process receive signals from the computer relayed through analog controllers; or in some cases, analog controllers are omitted and the computer is connected directly to control devices or actuators for direct digital control (DDC). In a DDC system, the elimination of conventional instruments and control equipment offsets the cost of the computer equipment. A disadvantage is that manual control is harder to invoke in the event of computer malfunction.

Human intervention occurs through input-output equipment. An operator can communicate with the computer by using pushbuttons, switches, knobs, typewriter keyboards, video display screens, and punched paper tape or cards. The computer communicates with the operator through alarm buzzers, horns, lights, digital indicators, typewriter printouts, and video displays. Although the degree of difficulty varies, almost every control computer can be bypassed by the operator to take direct readings from sensors or to enter changes in the process through analog controllers or manual adjustment of control devices.

Figure 1 depicts a digital computer control system. Industrial process control developed before business and scientific computer control, and Figure 1 shows the similarities of concept in input and output. Not shown in Figure 1 are computer concepts once though to have only commercial or scientific application that are now finding their way into process control technology. For example, information storage and retrieval methods have much to

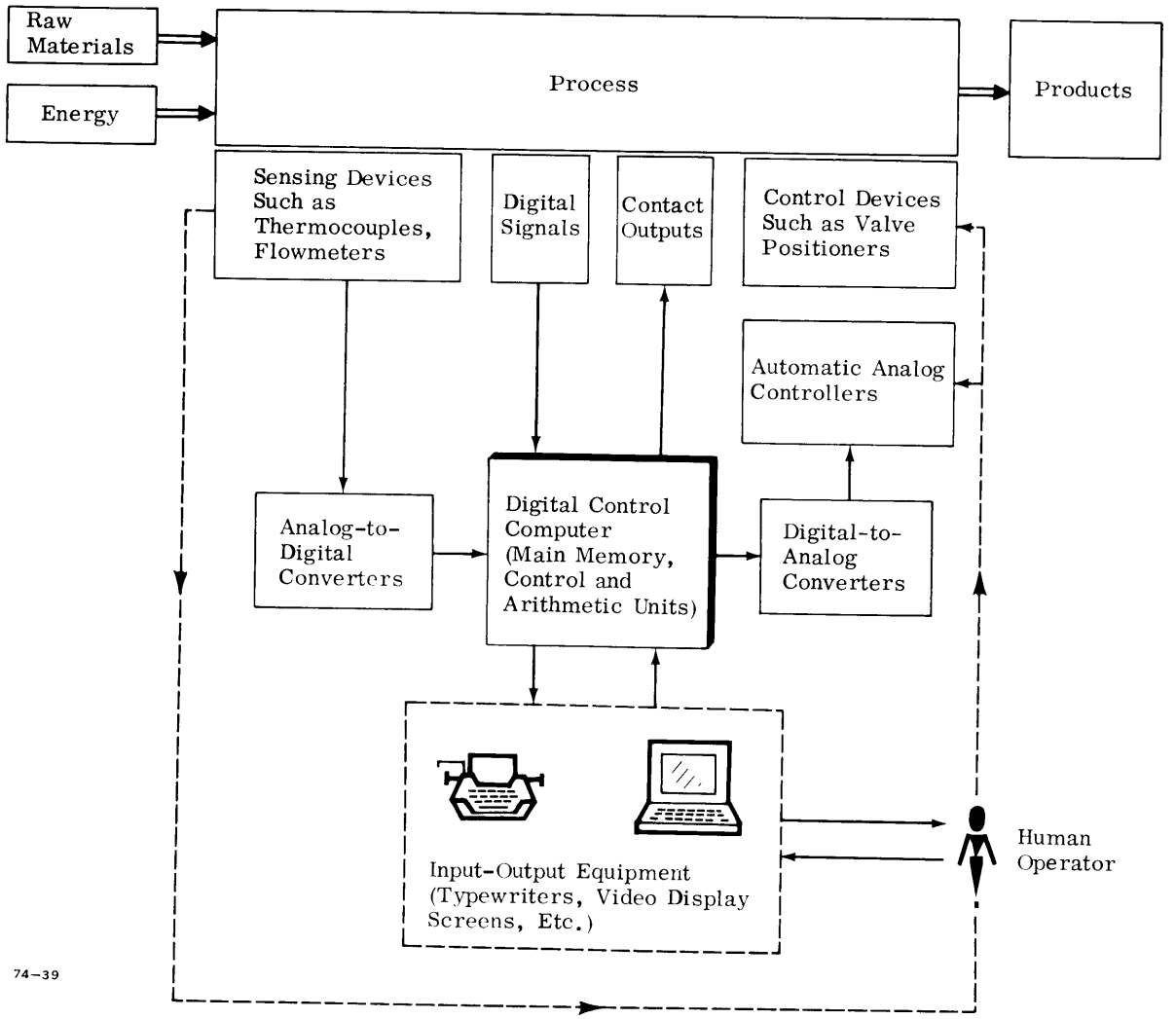


Figure 1. Digital Computer Control System

offer in the creation and maintenance of a system data base; time sharing has become commonplace; compilers, report generators, and batch processing techniques are all appearing in today's control computer systems.

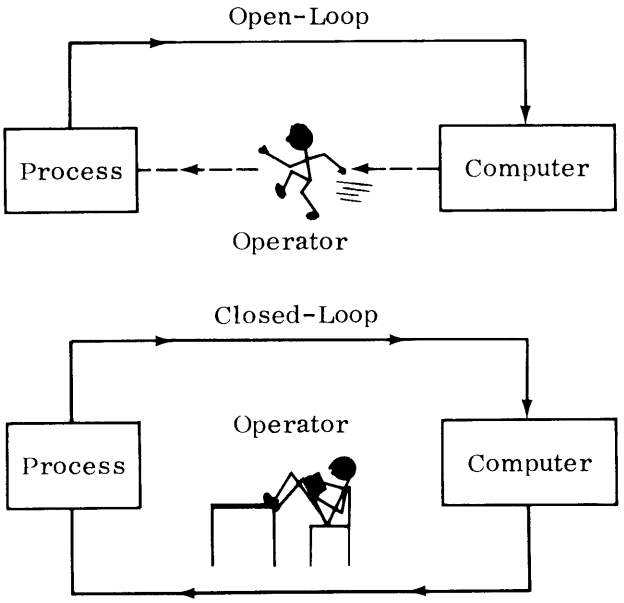
FORMS OF CONTROL

In the most elementary control applications, the computer is not connected to the process but functions as an extension of instrumentation to collect and record process data, which is entered manually and interpreted by the operator. In its more advanced functions, however, the control computer is connected directly to the process and is part of a total system of control. Advanced functions range from the output of explicit instructions for an operator to follow (open-loop system) to complete automatic control of the process (closed-loop system). The relationships in the open-loop and closed-loop system appear in Figure 2.

An advanced form of closed-loop control is optimized control. The objective of an optimized system is to achieve the best or most desirable operating conditions while also controlling ultimate goals such as production costs, yields, or efficiencies. The computer takes into consideration all significant variables, calculates the best process conditions, and applies the integrated control changes necessary to achieve the most desirable performance. This type of control is particularly appropriate for continuous processes in which many variables interact simultaneously. Optimized control, for example, can be used to achieve the most profitable product mix from a given input of raw materials.

CONTROL COMPUTER CONCEPTS

There are three main categories of tasks that a control computer can perform: supervisory functions, control



Note: Broken lines indicate manual handling of information; solid lines indicate automatic transmission.

74-40

Figure 2. Open and Closed-loop Control Systems

functions, and recording and reporting. In the supervisory role, the computer collects data and provides it in an accurate and timely form to the operators. In its control function, the computer calculates control action to be performed and either executes the control itself (closed-loop) or advises the operator of the action to be taken (open-loop). Recording and reporting is primarily used by management to promote closer control.

The tasks performed and the general information flow is depicted in Figure 3.

Supervisory Functions

Supervisory functions include process monitoring, indirect measurement, and logging and alarming.

Monitoring. Monitoring is necessary to define the conditions in the processing system. It is accomplished by determining the status of the instruments and process variables, the equipment, and the product. The status of the sensing instruments is determined by scanning on a fixed time schedule, by a signal from the process itself, or on demand either by the operator or by the control program. The frequency of scanning is commensurate with the use of the scanned data and the dynamic characteristics of the unique process. Scanning also involves the discernment of out-of-limit conditions. This can involve screening out wild or erratic readings by taking comparison readings from similar instruments in a different place.

Data from the process instruments is converted to digital form prior to its entry into the computer; the computer software is responsible for transforming the data

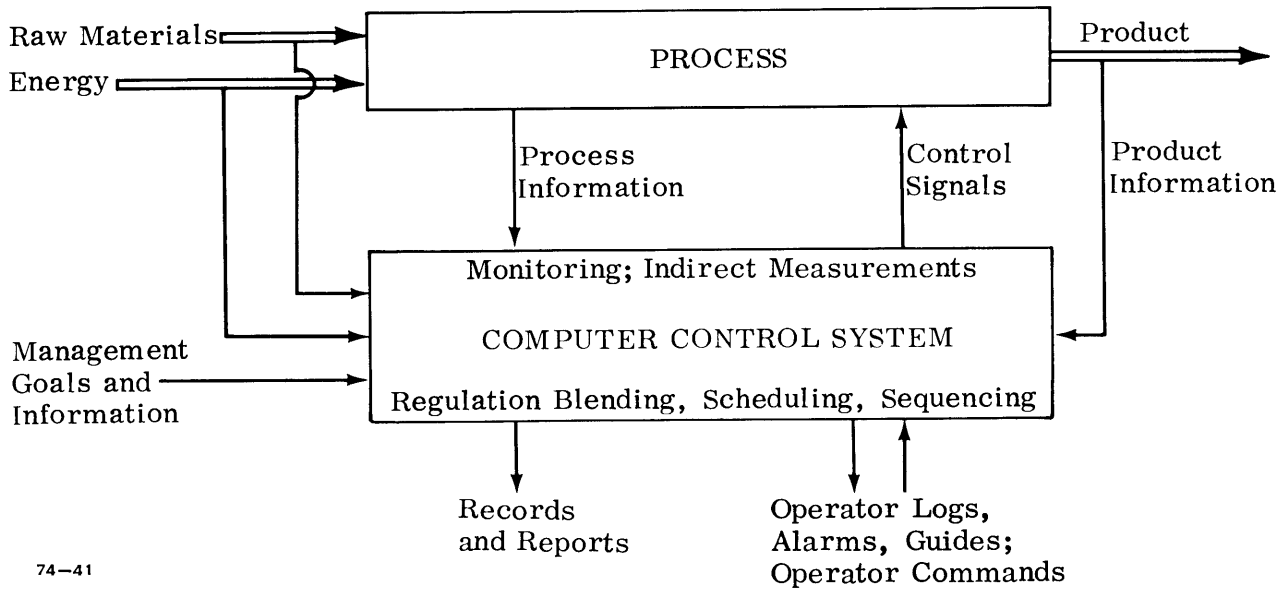


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Figure 3. Information Flow in a Control Process

into meaningful units such as gallons per minute or degrees centigrade. Such conversions are accomplished either by conversion tables stored in main memory or by calculation through use of a suitable routine. Modification required by a change of instruments, instrument rescaling, or correction of various factors is accomplished by reprogramming rather than equipment modification of the control system. This versatility is a significant characteristic of the control computer.

Data from the process instruments can be further refined by data substitution, correction, calibration, compensation, smoothing, curve fitting, integration, and differentiation. Techniques such as these are generally performed by software routines.

The monitoring of equipment status prevents mistakes that could result in injury, severe equipment damage, or material losses by preventing (closed-loop) or guarding against (open-loop) forbidden combinations of valve settings, motor conditions, and so forth. Equipment monitoring of this type is standard in most control computer environments.

To determine the status of the products, the computer receives information on product quantity and quality either from the on-line process or from data entered manually by way of input devices such as the video display.

Indirect Measurement. Another major function of a control computer is to indirectly determine unmeasurable quantities by computation from other variables which are measured. Variables may be unmeasurable because the cost of sensing instruments is prohibitively high, relevant on-line sensing instruments are unavailable, the process noise at the desired measurement points is excessive, or the variable is a quantity that cannot be directly measured. Efficiency is an example of such a variable. Calculated variables are valuable as data for further calculations associated with the control functions of the computer and as necessary input to process-analysis studies.

Logging and alarming. The control computer can present information gathered through the monitoring and indirect measurement of the process through logging and alarming functions. (These are different from reporting and recording, which are discussed later.)

Logging is a data acquisition function that can be periodic (continuous analog signals) or non-periodic (chromatographs operating asynchronously with the control system). Information that is logged can be output on a fixed schedule, in a response to an operator inquiry, as an exception report, or as a result of an event in the process. The form and content of the report are established and modified by software. Generally logs are of two varieties: One presents information directly needed for the operation of the process whereas the other provides selected data for supervisory personnel. Averages or exceptions, for example, have meaning for planning but not for direct control of the process. Logged information is communicated by means of typewriters, video display units, and plotters.

An alarm system immediately communicates to an operator that an out-of-limit condition has occurred in either a process variable or a piece of equipment. An alarm can be a light, a typed red warning message, a buzzer, a horn, or a video display. Predetermined emergency situations can be immediately and automatically handled by corrective action by the control computer if it is configured with the appropriate devices.

Control Functions

Computer control can regulate process variables at a desired value, carry out a schedule or a sequence of predetermined process actions, and optimize processes.

Regulation. Regulatory control adjusts set points of local analog subsystems. The control can be feedback, feedforward, or multivariable. Feedback control can regulate an output variable that is measured indirectly. Feedforward control gathers information, anticipates, and counteracts possible upsets to the system. Multivariable control simultaneously manipulates several input variables to produce a desired output value without violating process limits. Raw material blending is an example of multivariable control.

Standard procedures for regulatory control include the solution of conversion equations for feedback control, validation for high-low limits on variables and outputs (including recognition of reverse reaction response), output status checks and dynamic adjustment features. The control computer does not handle all of these procedures; some are handled by sophisticated process equipment such as multi-variable controllers and other instrument units that include integrated computing circuits. The special purpose process equipment is not only generally less expensive but also less flexible than the control computer.

Scheduling and Sequence Control. Scheduling and sequencing control supervises the flow of materials through a plant and the events that operate on it. Successful operating conditions must be reproduced consistently and uniformly. Scheduling control is limited in its use because it assumes that other factors are always equal and that the same action produces the same results. Because of its limitations, scheduling control is often presented to an operator as an open-loop suggestion.

Sequencing control handles the coordination and serial-control problems of a process. It is used when a series of predetermined control actions must be carried out and considerable monitoring and checking must be done before proceeding from one step to the next in the sequence. An example of such control is the starting and stopping of a steam-boiler and turbine-generator unit.

Recording and Reporting

Documentation of process information is generally business-oriented and is part of a management information system. Reports include material usage, production, cost accounting, inventory management, lost-time analysis, maintenance required, equipment performance, quality control, process analysis, legal records, and information retrieval. The most traditionally business-oriented function is information retrieval, which requires a large data base usually stored on a magnetic disc.

Other business-related tasks that can be performed by a control computer include accounting and clerical jobs, production planning, and inventory control. These functions are normally executed in a batch environment although occasionally they are done in a time-shared environment.

CONTROL COMPUTER HARDWARE

Basic to determining the capabilities of a control system are the interrelationships and characteristics of its input and output, arithmetic and control units, main memory, and priority-interrupt features. Both process and non-process devices are relevant to a control computer.

Non-process devices such as magnetic disc, drum, tape, and operator's console are needed for operator communication and for storing and retrieving information. These devices can attach to the system through a direct memory access (DMA) channel or through a programmed I/O (PIO) channel; high speed devices (disc, drum) connect to DMA and slow-speed devices to PIO. The best results occur when all devices are buffered. Processor arithmetic speeds, storage access times, instruction execution times, and maximum data transfer rates are less relevant for control computers than for business and scientific computers. Although these characteristics are important, they do not indicate true on-line process control capabilities. Other factors such as reliability are far more important.

Central Processor

The processor, through programs stored internally in main memory, directs the operation of the entire system. A control system has one or more processors. Multiprocessor control systems generally function in a clearly defined hierarchy of control or one processor operates as a backup for the other in case of failure.

Important features of processor design include word-size, instruction set, addressing methods, information transfer rate, and priority interrupt system. These influence programming, effective computing speeds, and storage utilization.

Another important feature is the interval timer and clock. Because this circuitry is often handled by pulse-counting on input channels, the discussion of the timer appears later under DIGITAL INPUT CHANNELS.

Information Transfer. The rates for information transfers between the processor and main memory and between the input and output channels and devices are extremely important because they affect the performance of the overall control computer system. If input-output facilities are limited it is difficult to use a digital computer efficiently. Some older systems, for example, cannot perform parrallel computation with data transfers. Others do not have a DMA facility. These limitations are rare for newer systems, however.

There are three main ways to enter information into the system: programmed entry, buffered entry, and direct entry. Programmed entry in its pure implementation is the worse possible means of entering data into a control computer. Input and output cannot be overlapped with computations because every piece of information passed into or out of the processor's storage proceeds under direct control of program commands, which of course use processor cycles. Programmed entry is best used for non-critical data that can be relegated to a low priority.

Buffered entry is a step above programmed entry. Buffers are storage registers functioning as "way stations"; they hold information temporarily until the processor is ready to receive it or the peripheral devices and channels have time to operate on it. Buffers allow the processor to proceed with computations after initiating a command to peripheral units, which then complete the commands or actions independently of the processor.

The number and size of buffers vary, but the minimum requirement for a control system is a one-character or one-word data register plus an input-output addressing and control register. Buffer registers for each type of input-output (analog, digital, or logging) provide complete overlapping of processing, input, and output.

Direct entry is by far the most straightforward means of data entry because it allows essentially simultaneous computations and input-output functions. Direct entry has specific main memory locations associated with the input and output variables. Transducers or converters transform inputs to or outputs from digital form. These functions are performed independently of the control programs and require external control circuitry for switching and timing.

Information flow within the control computer in its optimum case is depicted in Figure 4.

Word Size. The word is the basic primary unit of data. Words are generally a sequentially numbered group of bits, data bits as well as check bits or parity bits.

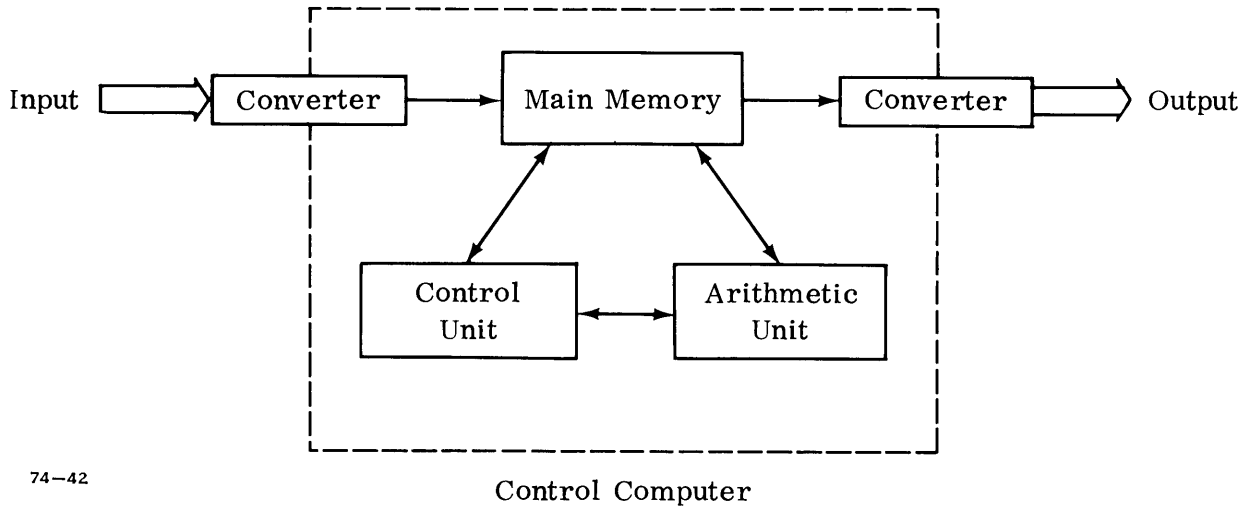


Figure 4. Optimum Information Flow in Control Computer

(Parity bits are not always used). Words can be fixed-length or variable-length. Variable-length words are the most flexible and offer the most efficient means for specifying adequate precision in calculations. Fixed-length words often require double word calculations for adequate precision.

Instruction Set. The control computer's instruction set can reduce the number of "housekeeping" functions necessary by providing the right kind of instructions. Instructions to transfer large variable length blocks of data between storage units or between memory locations should be provided. Instructions should perform more than one operation in a single command. They should allow direct, indirect, indexed, and immediate addressing. The most powerful and precise instruction sets for process control allow variable length word manipulation at any desired bit level. Such instructions, however, are usually bulky and time-consuming to code.

Priority Interrupt. The interrupt system is the primary vehicle for handling emergencies, accepting intermittent data, and interleaving diversified on-line and off-line tasks. It allows the processor, upon receipt of an interrupt signal, to suspend work on the program in progress, to transfer control to another program, and to return control to the original program automatically when the routine is finished. An example of an emergency interrupt is a power-failure interrupt. Important considerations in a power failure situation are safety to humans, equipment, and data.

Interrupt signals are caused by electrical impulses or by switches. Electrical impulses can come from either the computer system or external devices. Switches can be set manually or by alarm devices or process events.

In the complex control environment, interrupts must be serviced according to a clearly defined hierarchy of priority levels. This can be provided both by equipment and programming; most systems use a combination of hardware and software interrupt priority scheme.

Main Memory and Auxiliary Storage

Main memory stores the data, programs and results currently being used. The most important characteristics of main memory are its size, addressing capability, and sensitivity to power fluctuations. The size of main memory required for a system depends on the definition of the process and the tasks to be performed. Memory size is measured in terms of the smallest addressable unit, for example, 16K 16-bit words or 16K bytes.

Most main memory components used today (semiconductor, plated wire, core) are sensitive to power fluctuations. Power-failure protection is therefore provided by circuitry that prevents storage accesses when power-supply voltages are below safe limits.

Main memory protection is also essential in a control computer to prevent interference to the process while another program is being "debugged" or run. Protection at the hardware level is provided by logic circuits that inhibit the execution of any instructions that attempt to write in a protected portion of main memory. At the software level, protection is accomplished by the operating system's assignment of protection keys to individual program areas. A comparision of protection keys precedes a program's access of memory.

Auxiliary storage is usually a magnetic disc or drum; it stores data or programs not immediately required by the

control computer. Disc or drum access times are significantly slower than non-rotating memory access time; moving head discs are the slowest. Because it is too slow, magnetic tape is rarely used as auxiliary storage in a control environment.

Input and Output

Programmers and engineering personnel, the computer, and the process communicate with each other by way of input-output channels. Channels are characterized by their ability to operate simultaneously with processing, their transfer rate, and their transfer mode. Maximum flexibility of I/O structure is one of the strictest requirements in a control system; most systems can transfer data by way of programmed I/O, buffered I/O, and direct memory access.

The types of input/output devices, logging devices, and displays cover a wide range. Control computer systems offer input/output expansion in small increments: up to over 2000 analog and digital inputs, several hundred analog and digital outputs, and multiple logging and display devices. Furthermore the process environment dictates that the channels and devices can be added or deleted as required.

Input-output channels often perform some integrated computing and control functions such as "compare" and "add". This unburdens the processor of highly repetitive functions such as those involved in comparing a measurement with a standard value to detect random or out-of-limit events. Intelligent channels simplify programming, reduce interrupt operations, provide more efficient memory utilization, and improve the overall capabilities of the control computer system.

Types of Channels. Channels in a control environment are defined in terms of their functions and the equipment they service. Two basic types of channels handle analog input and output and digital input and output.

Analog input channels contain control registers and data registers that receive instructions from the processor. General functions the channel provides are termination points for process analog signals, the conditioning and normalization of the signals to required levels for amplifiers or analog-to-digital converters, analog-to-digital conversion, and data transfer to the processor's storage. Specific functions might be the selection of the exact process point to be read, the generation of proper timing signals, initialization of analog-to-digital conversion, and generation of an interrupt to the processor if necessary. A termination unit, signal conditioner, multiplexer, amplifier, ADC, limit comparator, or calibrator (including thermocouples) can be attached to an analog input channel.

Analog output channels are required for closed-loop systems and basically are a special form of the digital output channel that converts digital data to analog form. Outputs are voltage or current, pulse train, or pulse duration signals.

Digital input channels scan, assemble, and accumulate discrete digital inputs into a suitable input format such as bytes or words. Digital input channels may or may not be intelligent. Those unintelligent channels can seriously degrade processing throughput because they require program (processor) time to perform their process functions. Intelligent channels perform status sensing and pulse counting and can provide effective input rates of 100,000 to 1,000,000 bits per second without requiring any processor time.

For status sensing, digital inputs are scanned sequentially. Changes are sensed by comparing present-status with last-status values held in registers. If necessary, the channel generates an interrupt. In pulse counting, pulses generated by process devices are integrated or accumulated. Pulses represent a unit of measurement such as time, volume, length, and so forth. Time integration is an extremely important function of a pulse-counter because elapsed time and real time are required by the control computer to determine when to initiate control actions, logs or updates.

Digital output channels provide transfer paths for digital signals from the computer to the process or process operators. Output can be contact operate, pulse output, pulse duration, display drivers, or printer output.

Instrumentation

Instruments in a process can be divided into two broad classifications: measurement and control.

Measurement. Measuring instruments are sensing, indicating, or recording units. Ranges vary from 3 to 15 pounds per square inch for pneumatic instruments or 1 to 5 milliamperes, 4 to 20 milliamperes, 10 to 50 milliamperes, and −25 DC to +25 DC volts for signals.

Factors measured include temperature, pressure, flow and liquid level. Temperature is measured by thermocouples, resistance thermometers, and gas-filled or liquid-filled thermometers. Pressure is measured by pressure gauges; flow by flowmeters; and liquid level by a displacement-type level meter.

Measurements or factors in measurements can be further analyzed by instruments such as mass, infrared, ultraviolet, and nuclear magnetic resonance spectrometers, gas chromatographs, and infrared analyzers.

Control. Controllers generally control a single variable. Cascade and ratio control systems, however, relate two or more variables. Controllers sense and compare; they also correct in a closed-loop feedback control

system. Controllers can be of the on-off, floating, proportional, ratio, or cascade type. Controllers often contain analog computing elements that can multiply, divide, or take the square root. At most, they handle three variables.

RELIABILITY AND PERFORMANCE

Down time cannot exist in a process that is on-line 24 hours a day. Therefore, business and scientific computers' down times—which range from 5 to 15 percent—cannot be tolerated in a control computer.

Reliability

Reliability is a function of components, design, manufacturing, and overall system performance. Components must be long lived and have predictable characteristics, which can usually be determined by qualification tests. The most useful measure of reliability is the mean time between failures (MTBF).

MTBF is calculated either by actual experience or by combining the reliability of the component parts. Because there are so many components in a digital computer, the best design minimizes their number by organizing components to avoid duplication of function. (Duplication is used, however, for system backup.) Strict quality control in manufacturing components is a necessity.

Reliability is no guarantee of perfection so preventive maintenance is a critical factor. Possible equipment failures must be detected. This can be done by diagnostic programs, test points and indicators, and/or modularity of circuit design. Diagnostic tests and internal parity checking can detect and pinpoint marginal conditions and impending failures. Test points and indicators can be set to generate an interrupt if they are not reset after a specific time. Since modularity allows for substitution of defective parts, they can be repaired off-line.

Even more important than reliability and maintenance is making the system fail-safe — designing the system so that failures, if they occur, will not result in uneconomical or hazardous operation. System fail-safe measures can include an operator alarm system to warn of unsafe or out-of-limit events; a means to transfer control to completely manual operation; the establishment of predetermined set-points for all control devices in the event of system-failure; and the duplication of the control computer for backup.

The nature of a given application determines the method used for making the system fail-safe. System failures can also occur external to the control computer. For example, a measuring device can provide incorrect readings. Programmed checks aid in detecting and correcting such external failures.

Performance

Performance in a control computer environment is not necessarily determined by the sum of the performance of the parts; rather, it is determined by unique interrelationships between components, hardware, software, and so forth.

Primary considerations for determining the performance of a control computer include the following factors.

- The speed with which the system can scan input data (the number of inputs acceptable), convert it to machine language, check it for reliability, and store it in working storage for processing.
- The amount of processing time required to solve the control algorithm.
- The time the processor requires to execute control programs.
- The number of logs and printed records the system can produce while controlling the process.

A control computer that uses a relatively slow processor but extensive buffering and direct entry I/O channels may perform better than a high-speed processor that uses only programmed I/O and minimal buffering. Thus, a detailed analysis of each system must be performed before a system is selected for a particular application.

CONTROL COMPUTER SOFTWARE

The biggest difference between a control computer's software and that of a business or scientific machine is the way it implements the interrupt scheme. The control computer must operate on actual time (clock time) and must operate in relationship to other events external to the computer. A control computer also receives information directly from instruments and must respond instantly to priority signals from the process.

Throughout this report we have assumed the primary importance of process mostly because its failure can be hazardous and costly. There are environments, however, where the control of a process is a secondary application on a computer intended primarily for batch or time-shared processing. The power and complexity of the control routines required by a given application cover a wide spectrum. For example, an application can require a highly complicated executive and little or no time is available for time-sharing or batch processing operations. In other cases, the on-line process is relatively straightforward, but involved preparations are necessary in other areas.

Software for a control computer consists of two types: operating system software and application software. Both are indispensable to an efficient control environment.

Operating System

The operating system is the most essential part of a computer control system. Besides coordinating the on-line programs, which is its primary duty, it must also coordinate other processing activity such as time-shared applications and/or batch processing.

Time sharing is the primary means of compiling or assembling additional programs, running test data, analyzing plant data, and executing unrelated off-line work. The batch mode generally performs off-line reporting and runs non-process related programs such as accounting or inventory control.

Time sharing is a risky business in an on-line control computer; therefore, the executive must have means, usually storage protection, to protect the process application from unwitting destruction and to protect the executive itself against tampering with its interrupt scheme.

A control computer operating system must schedule the execution of the various process programs, coordinate the servicing of priority interrupts, supervise input-output, analyze and correct computer malfunctions, and handle large storage transfers.

The core program in a control computer's operating system is the monitor, executive, or supervisor. All other programs report to the executive, which schedules and controls all program execution. The following routines report to the executive.

- The system error monitor receives input from the error detection hardware and initiates the requests for error analysis and correction programs.
- The scan control monitor services the interface between the process instruments (the analog-digital equipment) and the computer system.
- The input-output monitor handles operator communications, logging typewriters, and programmed input-output requests.

Because the primary responsibility of a control computer is the process, all process interrupts or service requests must be handled before any other programs are executed. Only the idle or unused time can be allocated to time-sharing or batch operations, and, if necessary, these operations must be immediately interruptable by the process. The interrupt monitor is of equal importance with the executive, but it is usually subservient to it. The interrupt monitor responds to external interrupts from the process, timer interrupts, and internal interrupts from the processing programs (system interrupts). Timer interrupts are generally considered system interrupts.

Process interrupts can be initiated manually or automatically. They denote process conditions that require attention; they may also serve as an alarm. System interrupts promote efficiency of the control computer and prevent possible malfunctions. Clock interrupts indicate the passing of discrete periods of time and can be used to start a scheduled operation.

Interrupts are also described in terms of their relationship to the control computer. An interrupt system can be single or multilevel, and it can be priority- and/or nonpriority-oriented. An interrupt level denotes its degree of susceptibility to being interrupted. For example, there is always a non-interruptible level for critical processing. Additionally, there can be one or more interruptible levels. When there is more than one interrupt level, interrupts are assigned levels according to the interrupt function and its time constraints. The differences between single-level and multilevel priority interrupt systems appear in Figure 5. Figure 5 assumes three interrupt conditions with priorities in reverse order to the order of receipt of the interrupts. That is, interrupt

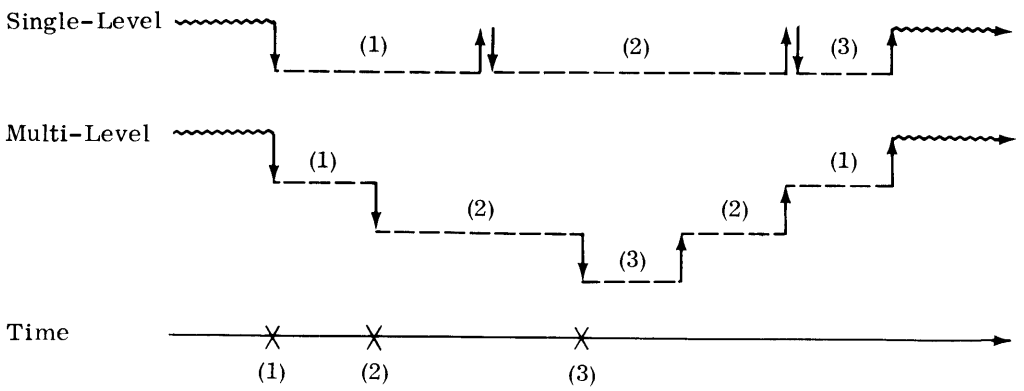


Figure 5. Single-level and Multilevel Priority Interrupt Systems

one has the lowest priority but is received first. The figure shows that multilevel priority interrupt systems are more efficient in responding to priority interrupts, but there is little or no saving in overall elapsed time.

Applications Programs

For business and scientific computers, applications are coded in computer programming languages, either higher level languages or assembly language. It is the same for control computers. Historically, higher level languages are easier to program; code is easier to document or it is self-documenting; software is easier to maintain; and the capability for extremely complex arithmetic and logical operations is provided. High level language compilers, however, run slower; use more system resources, particularly time and space; and do not provide the level of detail usually required in a control process.

Assembly languages are harder to program than higher level languages; codes are harder to modify; and programs are harder and more time consuming to document. Assembly languages are weak where higher level languages are strong. Also, assemblers run faster and provide a level of detail equivalent to the addressing level of the control computer. Assemblers are generally preferred for control applications; in particular they allow an application program to attain a very close relationship to the executive routines, notably the interrupt monitor.

A concept originally conceived for the scientific environment but heavily used for applications programs on control computers is code optimization. Depending on the needs of the application either time or space can be optimized. If the amount of information to be handled threatens to exceed the storage capacity of the computer, space must be optimized. On the other hand, if the time required to complete a calculation or processing phase exceeds the time prescribed, timing must be optimized.

Assembler programs are generally optimized by the programmer; higher level language programs are optimized either by the programmer or by an optimizing compiler. Optimizing compilers generally consume large amounts of resources but generally produce tighter, faster code.

CONTROL COMPUTER APPLICATIONS

Control computer installations are unique because the processes to which they are applied are as diverse as industry itself. Selected applications are presented here in order to give the reader an opportunity to relate typical applications to his own industry and his own problem.

Chemical Industry

The chemical industry processes ethylene, ammonia and methanol, and other chemicals.

Ethylene. The most valuable function of computer control in an ethylene plant is the optimization of operating profit, which is subject to all the process restraints and market limits that exist. In fact, the cracking furnace is generally the primary target of an optimizing program. The control computer also regulates the distillation portion of the plant to make products of specified purity and to carry out the specifications called for by the optimizer in terms of product splits and losses.

Typical plants can have five to 20 cracking furnaces with an assigned feed type. Although many feed types exist, most plants use either light hydrocarbons such as ethane or propane or heavier feeds generally described as napthas. Ethylene is the primary product, but other byproducts are also generated. All must be passed through compression and distillation equipment.

There are at least three independent variables for each cracking furnace: feed rate, diluent steam rate, and heat input. Each furnace can have a number of operating constraints, such as the cracking coil skin temperature, the furnace temperature, and independent variable limits.

Additional variables and constraints follow the cracking process, such as loading limits in the process gas compressors and each distillation column. The limits are a function of the products produced.

Ammonia and methanol plants. The primary function of computer control in ammonia and methanol plants is to increase throughput where market limits do not affect the production level. Neither process produces very useful byproducts. Because the equipment costs tend to discourage oversizing, the invariable bottleneck in any ammonia plant is in compression. Therefore, control computers are mainly concerned with getting as much synthesis gas through the compressors as possible at any given time. This throughput is dependent on ambient conditions and compressor availability. Maximum amount of conversion-per-pass at the synthesis converters is also important, and the conditions to achieve this target change as catalyst activity changes. There is an important tradeoff in this respect; conversion efficiency increases as pressure increases. Compressor throughputs must be restrained in order to increase compression ratios.

A control computer also regulates tasks. It maintains the proper hydrogen/nitrogen ratio at the shift converter, determines fuel to air ratios as well as outlet temperature control at the primary reformer, and regulates the methane content to the secondary reformer.

Rolling Mills

The production of steel was among the first applications of control computers because many parameters affect the product and decisions must be made very rapidly. Two important applications in the steel industry are hot-strip rolling and cold rolling.

Hot-Strip Rolling. The control computer allows improved productivity, more flexible scheduling, better gauge and width control, and less edge damage. Basically, the computer uses parameters such as slab temperature, composition, and dimensions to calculate and set side-guard positions, edger positions, edger speeds, table speeds, and main-roll screw positions. Constraints such as maximum allowable roll force, main-drive-motor load, and maximum roll bite are also taken into account. Because several slabs are usually handled at a time, the computer must keep track of all of them. When the slab is out of the roughing train, the computer determines the desired reduction schedule and optimizes the power distribution among the multiple finishing stands for maximum production. Supervisory functions include monitoring temperatures of the roll bearings and motor windings, voltage and current of each mill motor, strip tensions, and strip thickness. Other functions include automatic production reports and mill pacing to achieve maximum throughput.

Cold-rolling. Cold rolling is done with an incoming strip made from several hot-strip mill products welded together. The control computer calculates the reduction schedule that will minimize the number of passes. It also controls coil deceleration, mill reversing, and acceleration. It must also determine when the end of the roll is being reached. Thickness measurements allow the computer to preclude strip tension exceeding the yield point of the metal.

Cement Plants

The production of cement involves blending and grinding raw materials, which are fed into kilns to make cement clinker. The clinker is then ground to make cement.

An important consideration is the amount of free lime in the clinker because it cannot exceed a prescribed amount. Heat input is another variable which can be controlled in several ways varying in complexity. Most use an off-line model for optimization in conjunction with an on-line regulation scheme. Optimization is for either a market-limited or production-limited situation. Multivariable control loops are usually employed for regulation. Other control functions include detecting upset condition detection, automatic start-up and shutdown, and control of blending raw material to smooth out fluctuations in the feed.

Some variables are controlled in the cooler section: secondary air temperature, undergrate pressure, overgrate pressure differential, and exhaust fan temperature. Manipulated variables are cooler drive speeds and cooler fan throughputs.

Controlled variables in the kilns are: burning zone temperature, fuel to air ratio, before chains gas temperature, and before chains solids temperature. Manipulated variables in the kiln are fuel rate, exhaust fan speed, kiln speed, and kiln feed rate.

Petroleum Industry

Some functions of the control computer in the petroleum industry include oil refining (crude oil distillation, catalytic cracking) and pipeline and terminal operations.

Crude Oil Distillation. The primary function of a computer in a crude oil unit is regulation. Specifically, regulation involves computing the flows of all products to satisfy production requirements and still keep each product in specification. A model is required to predict cut-point temperatures as a function of draw rates. Adjustments in reflux and bottoms temperature must be made to compensate for effects of changes in product rates on tops and bottoms. Distillation usually requires a large-capacity control computer because there are many interactions and long dynamic lags in the various columns of a crude unit.

Fluid Catalytic Cracking. Fluid crackers, like crude units, are large and complex. The main goal of computer control is optimization of product yield, distribution, and throughput. Optimixation is on-line because a fluid catalytic cracker is never in a steady-state condition.

The chief controlled variables are recycle ratio, reactor temperature, and catalyst/oil ratio. Others are air rate, stripping stream to the reactor, fresh feed rate, and system pressure. Most of the variables are dependent.

Pipelining and Production. In both applications, the computer acts in a supervisory capacity. In pipelining, it handles automatic dispatching, inventory monitoring, batch tracking, and supervision of remote compressor and pumping stations. In production, it handles automatic well-testing and data acquisition for oil, water, and gas production; well start-up and shutdown; pump control; and inventory monitoring.

Oil field applications often use satellite data acquisition stations because there are many scattered, remote wells, and state requirements and multi-owner relations in unitized fields make frequent status evaluation necessary. Also, off-shore sites have peculiar problems such as automatic shut-in.

Pulp and Paper Industries

One critical area for a paper mill is raw material variation as determined by the pulp characteristics. Other operating variables are additive flows, temperature, head box level, slice position, wire speed, vacuum, press roll pressures, dryer environment, and intersection tension.

Many of the variables in the paper product industry, especially for the finished product, are not measurable on-line. Examples are basis weight, thickness, tensile strength, color, and moisture content. Feedback control is difficult because of the noise factor. Variables, therefore,

are measured either by beta-gauge measurements or occasionally by programmed histories. Often a statistical approach is used to reduce the standard deviation of the basis weight significantly.

Power Generation and Distribution

One of the primary considerations of computer control in this industry is the avoidance of catastrophes. Many computer installations are dedicated to monitoring and surveillance. Certainly, monitoring and alarming functions are performed in all power plant computer installations. Some are also fully automated including cold start and shutdown.

Direct digital control is often used because it is required by such operations as sequencing the start-up of a boiler-turbine-generator system. The computer supervises the feedwater, firing rate, and level controls, allowing the boiler to produce constant enthalpy steam. Steam supply initially is tightly regulated; later, the values are handled automatically. Start-up of a cold turbine requires coordination of high-pressure and low-pressure sections; initial check-out; acceleration to operating speed; synchronization with the electrical network; and finally, loading to the specified level. Metal thermal shock, excessive vibration, and over acceleration must be avoided.

Power dispatch is another area regulated and controlled by computers.

Nuclear power plants require approximately the same functions as conventional power installations. In place of a boiler fired by fossil fuel, the heat source is a nuclear reactor which is susceptible to rapid and wide-ranging transients that can cause catastrophic damage. Monitoring these transients and detecting deterioration of operation before a real hazard exists is an important role for a control computer.

Food Industries

The computer's role in food industries usually is that of a high-level supervisor which examines the accuracy of each step of various subsystem operations and requests adjustment or signals an advancement to the next step. Food industries often use open-loop control system or mixtures of open-and closed-loop systems. Hundreds of variables are required for computer control. They include sensor measurements such as temperatures, humidities, flow, pressure, level, and quantity. Other functions include requesting and adjusting the liquid and dry ingredients added to batching equipment; monitoring bulk storage of ingredients; control of batch blending and mixing from stored recipes; monitoring time cycles, oven temperatures, and speeds; recording of production leaving the lines; direction of storage and retrieval of products in holding areas; and recording and outputting inventory and available-space data.

Another function in food industries (and others) is automatic warehousing. Stacker cranes must be used in the most efficient manner; plus a real-time inventory often must be maintained.

General Automation LSI 12/16 Processor Clip

INTRODUCTION

Change in the computer industry has always occurred at a high rate. Since the introduction of computers for commercial use, generation has followed generation in rapid succession. A change in basic circuit technology — always tending toward smaller size, higher speed, more reliability, and, especially, lower cost—produces changes in software architecture, data handling and storage methods, and even types of peripherals used, because the ultimate goal is to reduce the cost of the total system.

Changing the cost of one large system component alters the cost relationships among the other system components, leading to new types of system architecture. If memory is more expensive than labor, then programmers spend long hours devising ingenious algorithms to save the memory required by a program. If memory is cheap relative to manpower costs, then high-level languages are used to save programmers time at the expense of efficient utilization of memory. If memory becomes very, very cheap — who needs discs? Exit virtual storage.

Thus, a change in circuit technology quickly snowballs into a series of other changes and a new generation is born. The advent of large-scale integrated circuitry using semiconductor technology was the beginning of such a change. The miniature, high-density semiconductor "chips" of various kinds lent themselves to mass production; and they attacked existing computer technology on two fronts. On one hand, they could replace the magnetic cores used for working memory; on the other hand, they could replace the small and medium-scale integrated circuitry used in the CPU itself.

Success on both fronts is linked to three factors. First, larger and larger numbers of bits can be packed on a single chip, which increases total reliability (fewer interconnections to malfunction), reduces power consumption, and reduces total size. Second, mass production methods have been developed for high volume and low cost without sacrificing reliability. Third, the product has been marketed successfully.

Core memories were first impacted by semiconductor technologies; it is clear that the changeover from core to semiconductor memory is now well under way. The change-over in CPU circuitry is just beginning, slower in coming because CPU circuitry is complex and engineering the CPU functions onto semiconductor chips at their existing densities is difficult. As a result, the first semiconductor CPU chips, called microprocessors, were "simplified" in a number of ways that did not prevent them from becoming cost-effective in certain types of applications, with their most notable success as the basic component of calculators.

As technological and engineering problems were solved, a second generation of faster, denser CPU chips was born. These chips are called microcomputers because they can compete at the low end of the minicomputer market when memory, I/O circuitry, and programs are added. The ability to produce CPU chips equal in power to the fastest minicomputers and general-purpose computers is a matter of increasing speed and bit density to specifications, and that may well be within the range of these new semiconductor technologies. The semiconductor CPU's "third generation" (macro microcomputer?) is probably already on someone's drawing boards.

Meanwhile, what will the impact of these new microprocessors and microcomputers be on today's minicomputer markets? To answer this question, the successes and failures of microprocessors and the resulting developments in microcomputers must be examined. To understand some of the microprocessor's early problems, however, requires a brief examination of the semiconductor technologies currently used for microprocessor and microcomputer production.

SEMICONDUCTOR TECHNOLOGY

All existing semiconductor technologies base their circuitry on combinations of "solid solutions." The prevailing MOS (metal oxide semiconductor) technology uses silicon (valence of 4) as the "solvent" and another element with a valence of 3 (such as boron) or 5 (such as phosphorus) as the "solute" to yield semiconductor wafers with regular areas of either positive or negative charge, respectively. Typically, a thin insulating layer of silicon dioxide is grown over the substrate wafer, channels are etched through the insulation, and these channels are doped with the oppositely charged "solute"; i.e., phosphorus is used to create n-channels in a positively charged boron-silicon wafer or, conversely, boron is used to create p-channels in a negatively charged phosphorus-silicon wafer.

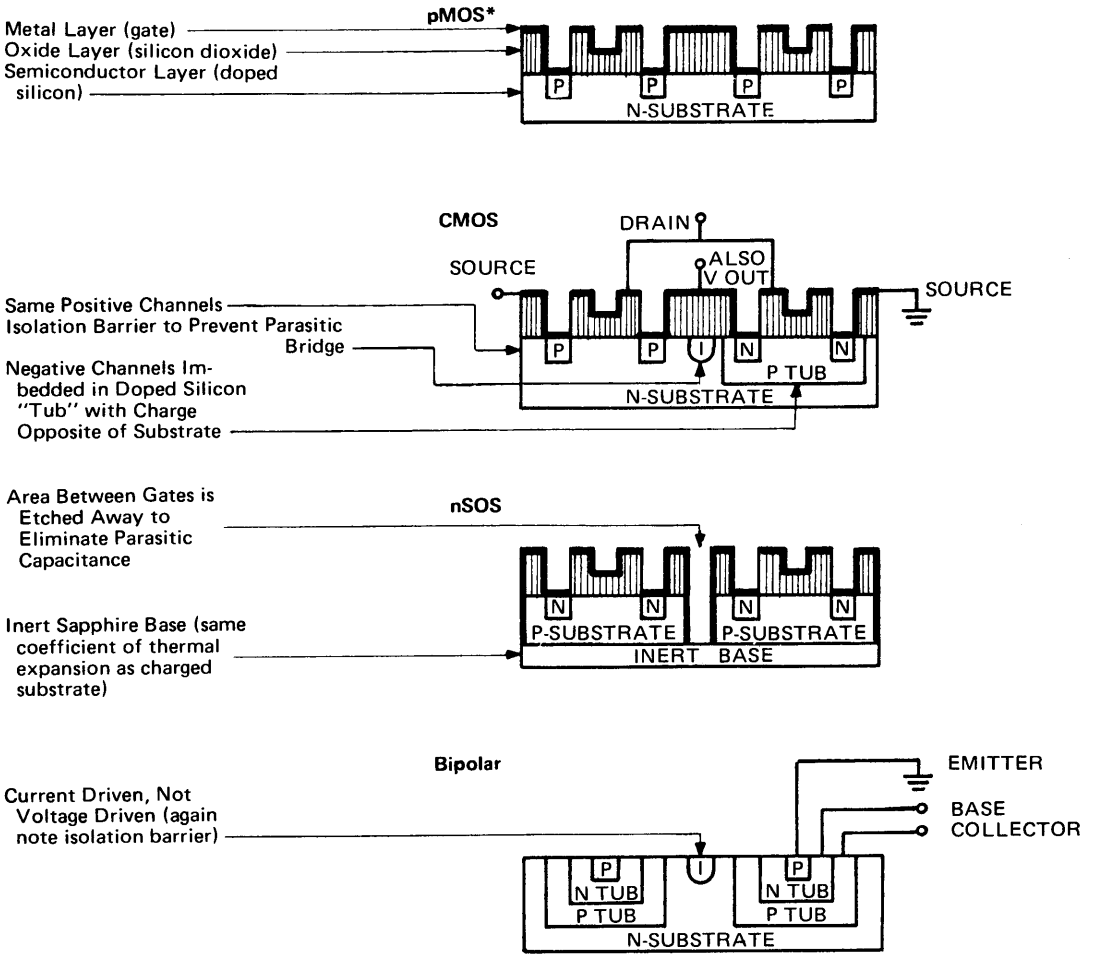
After several steps to build up the insulation layers and gates, while leaving the charged channels exposed, a metal is deposited over the entire surface. Gates and contacts are etched away; the surface is glassed in; and windows are

etched for external connections. The result is an n-channel or p-channel MOS chip, abbreviated nMOS and pMOS, respectively. (See Figure 1.)

Both pMOS and nMOS gate settling times are slowed by the parasitic capacitance presented by the thin insulating oxide layer sandwiched between two conducting layers. Some manufacturers have reduced this problem by developing CMOS (complementary MOS) wafers; Intersil and RCA, for example, are working on CMOS. Sets of p-channels are alternated with n-channels etched into an extra large p-channel called a "tub." This requires extra fabrication steps to make the p-tub and the n-channels within the p-tub; in addition, extra steps are usually required to create isolation barriers to prevent accidental "parasitic bridges" between the p-channels and the p-tubs. Again, see Figure 1 for an illustration.

Another method to make nMOS and pMOS faster is used by General Automation in conjunction with Rockwell, in their nSOS (sapphire on silicon) technology. In this technology, the whole MOS sandwich is superimposed on an inert sapphire substrate, and all surplus base material is etched away to cut down on parasitic incapacitance. The result is faster than CMOS. The manufacturers point out that nSOS is the low end of this technology, and that CSOS could achieve even higher performance. SOS could also be combined with bipolar circuitry.

Bipolar devices are faster than even CMOS and SOS devices. Each bipolar channel can be conceptualized as a channel in two nested tubs (again separated from other channels by isolation barriers) as shown in Figure 1. This creates a current-driven not a voltage-driven device, however; and it dissipates more power because an input current must be continually applied to the metal gate to maintain its "on" state. Bipolar circuits, moreover, require many more fabrication steps; consequently, they are more expensive. Typically nMOS and pMOS circuits require five masking steps and one diffusion step; bipolar circuit fabrication requires 12 masking steps and four diffusion



**nMOS is not shown, because it has the same basic pattern as pMOS except the substrate is positive and the channel is negative. Silicon gates also not shown (these achieve higher speeds on both pMOS and nMOS).*

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Figure 1. Microprocessors and Microcomputers: Semiconductor Transistors

steps; CMOS and SOS circuits are intermediate, they require two or three more steps than nMOS.

MICROPROCESSOR ARCHITECTURE

As might be expected, the earliest successful microprocessors used pMOS and nMOS technologies, with their less elaborate fabrication processes. The first CPUs had to be cut down to their barest essentials in order to fit on a small number of MOS chips.

The first manufacturer to mass produce and market MOS microprocessors successfully was Intel, a company formed in 1968 by former employees of Fairchild Semiconductor. Before introducing the 4004 microprocessor, Intel had earned a name for itself with its semiconductor memories, capturing a dominant share of the market in competition with such memory makers as Texas Instruments, Fairchild, National Semiconductor, and Mostek.

The 4004 is a 4-bit machine; the data bus and data handling registers are four bits wide, but the instruction register is eight bits wide, the address register 12 bits wide. Like most full-blown minicomputers, the 4004 has an arithmetic logic unit (ALU) and a program counter, in addition to its address and instruction registers. It also has 16 index registers, which can be addressed individually or in pairs.

Addresses, data, and instructions are all transferred over the 4-bit wide bidirectional bus. This means that the three segments of the address and the two segments of the instruction must be transferred using five machine cycles before the instruction can be decoded and executed. Because the CPU chip has only 16 pins for transfer of data, addresses, and control bits to and from memory, ROM and RAM memories are masked to "recognize" the proper location in the broadcasted addresses and to respond with an input or output operation. ROM modules contain words of memory, while RAM contains 320 4-bit words; up to a total of 4K words of ROM and RAM can be added to a system. A 4004 CPU can control 64 to 128 I/O devices.

Price and size have dictated the 4004's spare CPU architecture, with its 4-bit wide multifunction bus, small number of pins, limited instruction set, few registers, and so on. Consequently, programming a 4004 (in machine or assembly language) involves a number of maneuvers required by the limitations of the machine. A simple 4-instruction minicomputer program (Load, Add, Store, Stop) for adding two numbers takes 20 instructions with the 4004, because a 5-instruction routine is needed to assemble the address and the instruction for the operation performed by the sixth instruction. Then, because the 4004 has no Halt instruction, a conditional jump dependent on the state of the external test line is used to stop the program.

The 4-bit Intel chip sets are extremely low in cost; and, in spite of limited capabilities in comparison with minicomputers, they have found a wide variety of applications in addition to their original calculator market. The 4-bit word is ideal for decimal-number handling, so the 4004 is useful for cash registers, weighing machines, credit and point-of-sale terminals, and simple billing and accounting machines, particularly when these devices are interactive with (slow) human beings. Besides these applications, a large number of machine control applications are amenable to 4-bit microprocessor control. In the automotive industry, for example, applications include control of engine parameters, instrument displays, automatic locks, alarms, safety procedures, and burglar alarms, to name only a few. Intel says the 4004 can be a cost-effective replacement for any board with 30 to 100 packages of TTL logic.

Intel's major competitor for the large, general-purpose, 4-bit microprocessor market is Rockwell International with its PPS-4. Fairchild's PPS-25 is also competitive, particularly for the calculator market. These two systems have architectures that differ from each other and from Intel; but, like the Intel machine, they are extremely low-cost systems and very small. Consequently, they require clever programming to get around architectural idiosyncrasies.

The Rockwell PPS-4 has a slower clock time than the Intel MCS-4, but it is faster. PPS-4 uses Rockwell's proprietary 42-pin package, so it can implement separate 12-bit address and 8-bit data buses, making memory references easy and fast. Also, it allows fetch and execute portions of instructions to overlap. The CPU, including six registers and two control flip-flops, is contained on one chip; a minimum system consists of a CPU chip plus a memory chip. The CPU chip can handle 16 I/O chips, 30 memory chips, or a total of 30 mixed memory and I/O chips. Although the PPS-4 is faster and more flexible than the 4004 for handling BCD arithmetic, the Intel machine can handle more I/O, giving it a competitive edge in control-type applications.

The Fairchild PPS-25 is less suited than the Rockwell and Intel machines for general-purpose applications; but it is well suited for calculator functions, as well as for similar devices requiring numeric calculations, such as navigation instruments. The standard RAM module is organized as three 25-digit registers, allowing numbers up to 25 digits long to be processed serially by the CPU using a 4-bit data bus like Intel's. Although the 62.5-microsecond cycle seems slow, it is broken up into 25 time slots (versus eight for Intel and eight for Rockwell), allowing an instruction, for instance, to send to memory for another instruction and to receive it back. Registers can also be masked so that part of a register can be operated on by an instruction. The PPS-25 can attach up to 6,656 bytes of memory.

It is clear that the processing, memory, and I/O limitations of these three devices present no threat to the established minicomputer market. Instead, they are finding an enormous market as replacements for hardwired logic,

simultaneously achieving lower costs and greater flexibility. Costs depend on quantity, of course, but prices average less than $50 for chip sets.

The biggest problem faced by the new user in evaluating the suitability of microprocessors for an application is estimating the cost of programming them. Although all three devices have cross assemblers, assemblers, instruction simulators, and prototype board software support available, the programming is still somewhat intricate, especially for engineers unused to programming. The resounding success of all three devices, however, points to the fact that while programming is a stumbling block, it does not prevent microprocessor-based devices from being highly cost effective.

The second big cost involved with microprocessors is that of adding I/O logic, timing and control circuitry, memory modules, and I/O drivers to the microprocessor; assembling them into a system; and interfacing them to the product. Intel and Rockwell sell board-level systems, with CPU and related components assembled into a circuit board(s) that has simpler interfacing problems, similar to those encountered with stripped down minicomputers. These standardized boards are easier to use but are more expensive. A full-blown, tabletop, minicomputer-type device costs under $2,000 in most cases; but a minimum chip set usually is less than $50. In moderate quantities, the Intel 4004 costs around $15.

The cost of external circuitry and design work in building a system is enough to allow several manufacturers to buy Intel microprocessors OEM and assemble their own systems. Prolog, for instance, sells systems aimed at design engineers. The new 2 x 2-inch Teledyne TDY-52A is an Intel-based system, as is the DEC MPS Series. The tiny Intel-based TDY-52A sells for approximately $1,500 with 4K words of memory, while the DEC MPS sells for around $476 (with 1K memory).

It has been estimated that the huge market for the extremely low-cost, 4-bit processors has hardly been tapped. It is interesting, therefore, that new companies don't want to compete for the low end of the market. One reason for this lack of activity may be the relationship between R&D cost outlays and the long recovery time. The R&D costs are very large; the time gap between anticipated and actual delivery has frequently been large. More than one industry observer has noted that the most important specification for a microprocessor is its availability.

The larger, more expensive 8-bit and 16-bit microprocessors, which can overlap the lower end of the minicomputer market in many cases, have an average of 8 to 10 memory modules (256 words each) associated with each CPU, whereas 4-bit system applications usually require very little memory. A number of Intel users feel that the 4004 (MCP-4) is impractical when more than four RAM chips are needed. The upshot is that it is much easier for a semiconductor manufacturer to recover the R&D costs for a larger processor of eight or more bits because it increases sales of existing memory products which do not have to be redesigned.

From Microprocessor to Microcomputer — The First Generation

It was not until the first rumblings of the 8-bit microprocessors were heard that minicomputer manufacturers started to worry about the threat of microprocessors to existing minicomputer markets. A glance at the specifications for the slow first-generation 8-bit pMOS systems was temporarily reassuring; but R&D developments toward faster systems and the increasing miniaturization with greater CPU power told the more farsighted mini manufacturers that the days for small- and medium-scale integrated circuits were numbered. General Automation, for instance, began serious design efforts to produce a microprocessor-based mini.

The first 8-bit pMOS processors were not really microcomputers although they packed the CPU on a single chip and managed standard bytes of data; the slow speed and architectural limitations imposed by the scarcity of chip "real estate" kept performance down. Intel 8008 CPU (MCS-8 system), for example, added only three instructions to the 4004 instruction set (one of these is Halt, reducing the addition program discussed earlier to 19 steps on the 8008), added two pins to the chip, and reduced the number of registers to eight. Cycle time was reduced to 7.5 microseconds; DMA and interrupt capability were added; but the maximum number of I/O devices that could be handled was reduced to 24. Memory capacity was increased to 16K words, as opposed to 4K on the 4-bit system. The composite data/instruction/address bus architecture is retained, and each chip requires about 20 external TTL packages to implement. Performance is improved, however, because the bus is eight bits wide, and only five steps are required per machine cycle.

Another first-generation 8-bit pMOS CPU, called IMP-8 is marketed by National Semiconductor. Actually the IMP-8 is created from two 4-bit, 40-pin chips, operating in parallel with a microprogrammed control ROM (CROM). National semiconductor also markets a 16-bit system (4-bit chips operating in parallel); actually the 4-bit chips are all 4-bit CPU slices, so a user could configure a 32-bit word computer if he liked. The chip sets require a number of SSI (small-scale integration) and MSI (medium-scale integration) circuits to implement, thus the price is pushed up along with the word size. The IMP-8 has a 16-bit address scheme and can address up to 64K words of memory or devices, or both.

Although Intel's 8008 has many constraints, its low price and availability have made it a highly successful system. The market for 8-bit systems includes all types of communications gear (which deals mostly in 8-bit EBCDIC and ASCII characters), the new word processor

market, and many types of control systems. Intel's strategy has been to hold down the processor price by sticking to an 18-pin chip, small enough for good processing yields.

Both National Semiconductor and Intel supply their systems at the board level as well as at the chip-set component level. A user can buy the chips and do all the control and interfacing logic himself, or he can buy a microcomputer-on-a-board, with many of the control and interfacing chores already done. If he wants card reader input, though, he may have to design the card reader interface because microcomputer boards still fall somewhat short of minicomputer boards as far as ease of use is concerned.

Software support has increased to include a PL/M compiler for a high-level language similar to PL/1.

An interesting system, using four of National Semiconductor's 4-bit CPU slices to create a 16-bit processor, has been developed by Teledyne of California. Instead of using TTL, SSI, and MSI circuitry for external logic, I/O interfacing, and so on, Teledyne uses LSI throughout on 41 chips. It is housed in a tiny 2 x 2-inch, 120-pin package. A separate 2 x 2-inch package houses 8K words of memory. Teledyne also produces an 8-bit system based on an Intel processor; it packs the CPU, all logic, and 4K bytes of memory (50 chips total) in one 2 x 2-inch package. Teledyne has begun deliveries; the first applications take advantage of the extremely small size and have been for noncommercial aviation and navigation fields.

The Second Generation — Microcomputers Arrive

Although the delivered first-generation systems proved successful, most manufacturers concentrated on technologies other than pMOS for microprocessors with performance closer to minicomputer speeds, without sacrificing much size. The nMOS technology, in spite of its similarity to pMOS, doubles the speed of pMOS; the carriers of the charge are the extra electrons in the silicon lattice (resulting in negative charge) rather than the positive lattice "holes" (missing electrons). Electron carrying speeds are twice as fast, while threshold voltages are lower. The n-channels also require less space, so output buffers can be smaller, allowing more buffers and more I/O devices per chip. Manufacturers also learned how to make registers more compact, so more of them can be fitted on one chip.

One of the biggest problems in chip real estate is the bus structure, which needs to be twice the data word width to be efficient. Each interconnecting wire for the bus channel is around 1 mil wide, for a total of 16 mils on an 8-bit system. Manufacturers contemplating 16-bit processors are faced with a 32-mil wide bus, which takes quite a chunk out of a 200-mil wide chip. Using doped silicon for interconnections in the silicon-on-sapphire process allows narrower bus channels, but bus size is still one of the big problems for manufacturers trying to fit powerful 16-bit systems on a single chip.

The recent rash of second-generation microcomputer announcements signifies the state of the art in semiconductor technology. Three basic technologies obtain performance benefits over pMOS systems: nMOS (Intel, General Instruments, Signetics), SOS (General Automation, Rockwell), and CMOS (RCA, Intersil). Only two of these new systems, the Intel 8080 and the General Automation LSI 12/16, have been delivered, however. New microprocessors take about two years to develop, and they are prone to unexpected design problems requiring several chip prototypes.

The successful entry of General Automation into the market is significant in a number of ways. It marks the first line of defense against the impending encroachment of microprocessor manufacturers on minicomputer markets — if you can't beat 'em, join 'em. The fact that DEC has rapidly designed the MPS Series microcomputers, using the Intel 8008 in order to get large volumes of the product on the market quickly, underscores the threat to minicomputers. The 8080, although delivered, is not yet in high-volume production.

Industry observers note that about 10% of installed minicomputers are underutilized. It is these types of installations, using stripped down minis like Computer Automation's erstwhile Naked Mini or older systems like the PDP-8, which will be captured by the microcomputers first. Minicomputer manufacturers that produce microcomputers compatible with minicomputer lines, such as Computer Automation and General Automation have done, will remain competitive because of the body of software to which the systems fall heir. Undoubtedly, minicomputer manufacturers competing at the low end of the market will either have to develop their own microprocessors or OEM them from a semiconductor manufacturer in order to remain competitive.

Intel has taken advantage of existing 8008 software in the development of the 8080. The 8080 instruction set is a superset of the 8008 (78 instructions as opposed to 46). Users adapting 8008 programs to the second-generation processor have had some problems, but often they find the increased power of the new microcomputer well worth the reprogramming efforts.

The 40-pin 8080 is more like a normal mini; it has a 16-bit address structure, 64K-word memory capacity, and 10 registers; and it can address up to 256 I/O devices. The processor cycle time is 8.2 microseconds, faster than that of the 8008 but not up to current minicomputer speeds. Nevertheless, the flexibility and power of the microprocessor as a whole has led many manufacturers of terminals, word processors, and the like to feel they can make microcomputer-based systems competitive with minicomputers; processing speeds do not have to be high for these applications.

Most manufacturers working on second-generation microcomputer systems are, predictably, semiconductor manufacturers, such as General Instruments, Motorola, Signetics, AMI, Intersil, and RCA. Some manufacturers, Texas Instruments, for example, make both semiconductors and minicomputers; they are logical candidates to make microprocessors. Burroughs has used microprocessors to control its own peripheral devices for years. Honeywell uses its own "Big Blue" internally. Anxious minicomputer manufacturers, perhaps already into the calculator as well as the minicomputer market, are experimenting with semiconductor technology.

The lead time from introduction to first deliveries to high-volume production of a new processor is at least as long as for any new class of computers. In view of the number of manufacturers experiencing difficulties with the new technologies, however, the marketing move by DEC, choosing a design based on a first-generation processor in high-volume production, seems like good strategy. DEC delivered the first MPS in the second quarter 1974, high-volume production should follow shortly thereafter. As a result it will have a sizable installed base by the time a large number of second-generation microcomputers are available—which DEC estimates to be at least two years hence. DEC also plans to utilize the 8080 in its line as well, when production volumes are high enough.

The Third Generation

The basic trends in microcomputer technology are clear — greater miniaturization and higher speeds in order to place the maximum amount of processing power on a single chip. Semiconductor technology is still young, but the solution to many space and speed problems already seems within reach of those experimenting with SOS. It appears that future generations of microcomputers will replace the CPU not only of minicomputers but also, eventually, of the larger general-purpose systems. Conceivably, even some of the CPU memory, control, and I/O logic now external to the microprocessor chip will be fitted on it, shrinking the computer-on-a-board as well as the full-blown enclosed computer system. Meanwhile, the smaller, slower, cheaper processor chips will be used as components for new applications not yet thought of. Given DEC's estimate of two years before second-generation chips begin to impact the minicomputer business seriously, it is reasonable to assume that the third-generation revolution will be under way by 1980.

THE CURRENT MARKET

The characteristics of the microprocessors and microcomputers currently being marketed are listed in the Specification Charts.

INTRODUCTION TO MINICOMPUTERS

OVERVIEW

The revolution is over. Long live the revolution. The impact of the minicomputer has indeed been revolutionary. As problem-solving tools, their impact has been dramatic. But the torrent has matured to a broad, sweeping river. Indeed, so varied are the options facing the designer today that the very term "minicomputer" is in danger of losing its meaning.

While the range of solutions now spans a complete spectrum — from smallest microprocessor to the grandest minicomputer facility, the fundamental truth remains. The minicomputer represents the fruitful, joyful conjunction of technician and user. The technician can achieve perceptible goals within perceptible time; the user acquires a viable mechanism at reasonable cost.

This paper describes the early days, the frenetic growth, coming finally to a review of present technology. It describes applications that are well suited to this technology, and, by example, the advantages and disadvantages of using a particular technology. Some notes and methodology are presented to help the potential user survive the hazards of selecting a vendor. In applying technology, the problem is to choose from gradations of performance and variations in types of technology delivery: service bureau vs system supplier vs computer vendor.

Finally, in the last section, the broad trends that have influenced small-machine development in the past are cataloged and extrapolated into the future.

The word "minicomputer" became popular in 1968, to categorize a growing number of small, general-purpose computers. These machines were introduced initially to bring software solutions for the limited processing tasks of data acquisition and communications. These vintage machines, many from new vendors, generally conformed to the following descriptions:[1]

- Basic system configurations cost $25,000 or less.
- 4,096- or 8,192-word core memory.
- Programmed in Assembly language(and less often in FORTRAN).
- Computer peripherals often restricted to Teletype and paper tape.
- Usually supported customer hardware (sensors, communications lines, and control lines).

The scope of this report, however, is more than just "those processors that cost less than $25,000." Today, minicomputer is less a description of a black box than a philosophic approach to problem solving:

> "Give me just the right amount of hardware and software to solve my problem."

The technology today is broad. It is bounded by the $1,500 "system" based on the Intel computer-on-a-chip (or three chips), and a vast PDP 11/45 network from Digital worth a quarter million dollars including terminals, peripherals, and discs. With such scope it is clear why the application environment is boundless.

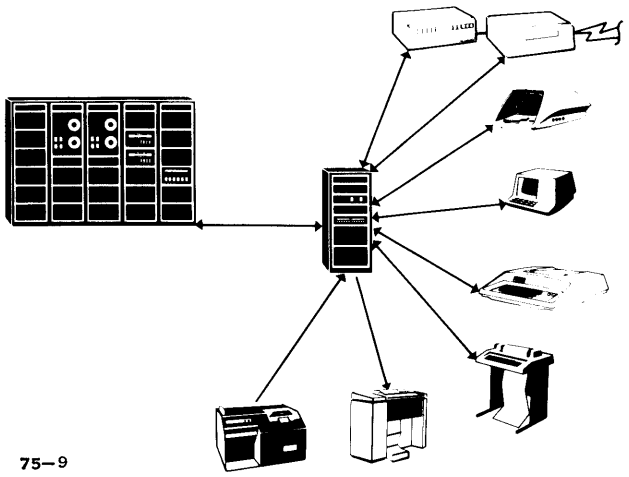

Figure A. Digital Equipment TC/D (Terminal Control Enhancement): up to 80 devices can connect to four such secondary TC/D processors; the secondary connects to the host processor at left

HISTORY

The computer industry dates from about 1954. Only then did the number of machines extant warrant the name "industry." In the first decade the trade boomed. Initially, reliability was obtained only at great expense, but transistor logic solved the problem of costs. As business organizations became acquainted with computing, configuration sizes grew, and the process was still very expensive. Operating systems were invented to harness the larger number of hardware units, and languages were put in the field to speed problem solution. Both caused operation inefficiencies, so faster, larger machines were required. The computing resource became centralized and vital to the organization, so time had to be scheduled. Batch operations were the standard, and closed shops the rule. If a task could not be made to conform to this mold, only two alternatives were available: do the job manually or design special hardware to do it.

Upon this scene, in 1962, came Computer Control Corporation[2] and Digital Equipment Corporation with small machines for laboratory applications. Digital opted for a 12-bit word machine that balanced the high cost of memory (a function of word size) against popular transducer resolution (1 part in 1,000, sometimes with a sign). Digital has prospered from that time to now, but development of this avenue of computing has always been servant to hardware advances. The introduction of transistor logic in the early 60's made small computers possible, but the use of integrated circuits in 1968 opened the flood gates of small machine activity.

The hands-on scientist with ill-conditioned data, the small user with limited budget, the executive with untimely reports, all found a new alternative for centralized

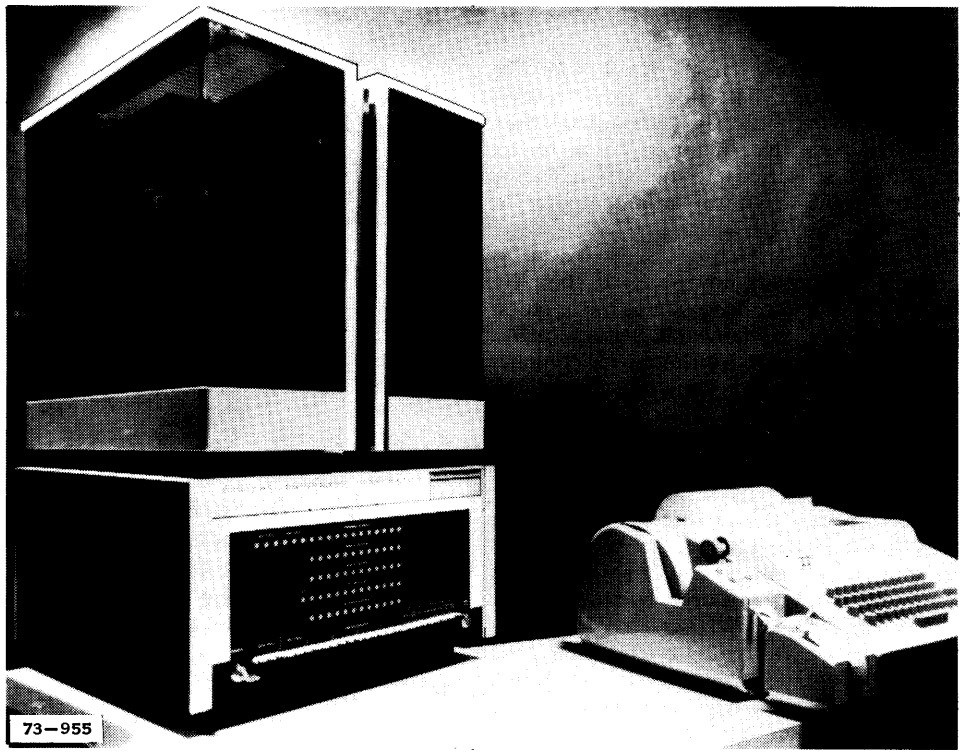

Figure B. First Tabletop Digital PDP-8 Computer System

computing. New minicomputer manufacturers entered the lists monthly until 1970, when the number of vendors stabilized to between 40 and 50 and new product emphasis shifted to low-cost, modest-performance peripherals. Also during this period a large number of small systems houses sprang up. They took the very modular, low-cost components and welded them into systems with software. It took only a modest bankroll to become a minicomputer manufacturer and even less to become a hardware-software shop providing turnkey service.[3]

More recently, other developments have accelerated the production and use of small computers:

- Availability of economical peripherals.
- Large-Scale Integration (LSI) of logic functions.
- Dramatic decline in memory costs (1973-74).
- Accumulation of system software.
- Advances in packaging techniques.

The improved hardware and software have significantly increased speed and reliability. The net effect is a better product at a lower price. With each quantum step of improvement, "minis" have gained wider acceptance and a broader range of applications.

The following table shows how two models of the Nova minicomputer from Data General Corporation compare with Univac 1[4] ,the first electronic commercial processor.

Date	CPU	Add Time (μ sec)	Memory (words x bits)	Cost
1952	Univac 1	4	1,000x48	$750,000
1972	Nova 1200	1.2	4,096x16	$5,200
1975	Nova 2/10	0.8	4,096x16	$3,800

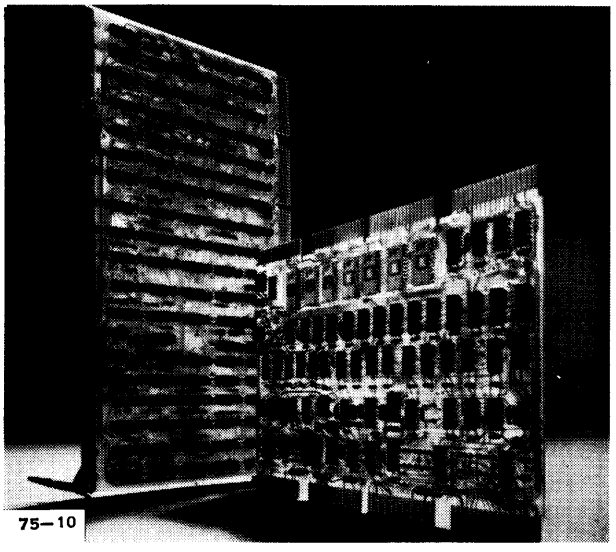

Figure C. The PDP-8/A, Digital's Smallest PDP-8: made up of two modules

Figure D. Alpha/LSI and Naked Mini/LSI

In the early 70's, the path of development was to extend the market upward by offering "bundled" operating systems and language processors. FORTRAN was available from practically all vendors. ALGOL and COBOL derivatives came later — but they came. Disc-based operating system software was so pervasive by 1974 that Computer Automation — ever an OEM supplier — provided one. Entering the last half of the decade, vendors were supplying machines that spoke ENGLISH[5] and employed some of the optimizing features of the very large systems:

- From IBM 360/85, circa 1968, comes the "cache" memory now on the Data General ECLIPSE.
- From the B5000, circa 1962, comes the "stack" architecture of the HP3000.
- From the IBM-360, circa 1963, comes the "dynamic control store" of the Varian V70 Series and Hewlett Packard 2100MX.

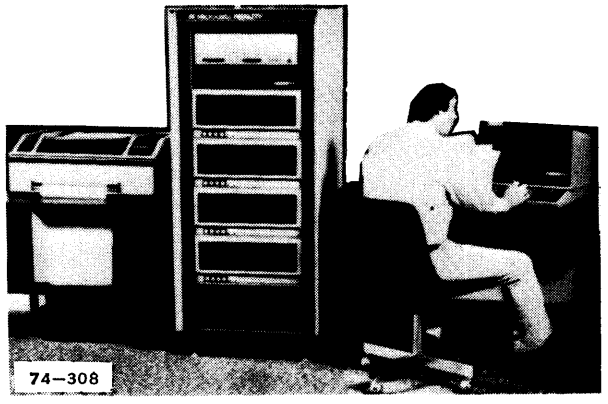

Figure E. Reality Speaks ENGLISH

At the other end of the scale, LSI allows a computer (with reasonable performance) to be built on very few chips for $500 and yet have a mean time between failures (MTBF) approaching 50,000 hours. Thus, today's minicomputer range is so broad that equipped with a variety of peripherals, it can be fitted for applications with budgets ranging from $10,000 to several millions of dollars. The unifying notions are no longer size or price. The term "minicomputer" now denotes modular construction and task-oriented system design.

MINICOMPUTER TECHNOLOGY

The "mini" in minicomputer acknowledges that these units have generally been associated with limited size, limited price, limited performance, and limited support from the manufacturer. Manufacturers are removing the "limitations" previously associated with minicomputers as fast as they can; superior performance and software are now available — at a price. Discussion will be anchored on middle-line minis, while the extremes of micros computers and mini-facility configurations are spotlighted.

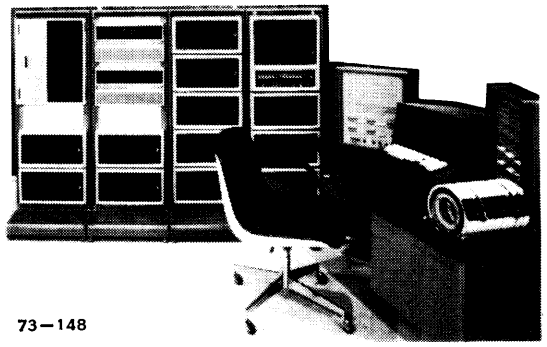

Figure F. Hewlett-Packard HP 3000

Design Philosophy

Minicomputers are designed as general-purpose computers with a mix of logical, arithmetic, and input/output (I/O) functions. These features are complemented with packaging that permits easy build-up from small configurations. Processor options, memory, and peripherals can, in general, be added by plugging-in circuit boards to prewired spare connectors in the computer chassis.

Minicomputer chassis are usually made of light sheet metal, which is satisfactory for practically all commercial installations. If the computer will be moved frequently, a specially ruggedized model might be selected. Recent packaging trends have been toward large circuit boards, which reduce the number of mechanical connections and make the units more reliable. For example, the entire Nova computer is contained on a single 15-inch-square circuit board; the Interdata 7/32 on two 15-inch boards.

Manufacturing economies are often effected by using power supplies of questionable merit. More than one manufacturer has had greater difficulty with the system's power supply design than with the processor.

The computer design can be shaded towards a broad applications market. A manufacturer can include many features as standard if the intended market requires those options. Machines intended for word-processing or accounting applications generally use shorter word lengths with multiple word instructions, and they implement hardware decimal arithmetic. Machines intended for scientific calculation or process control applications generally use long word lengths and frequently hardware for floating-point arithmetic.

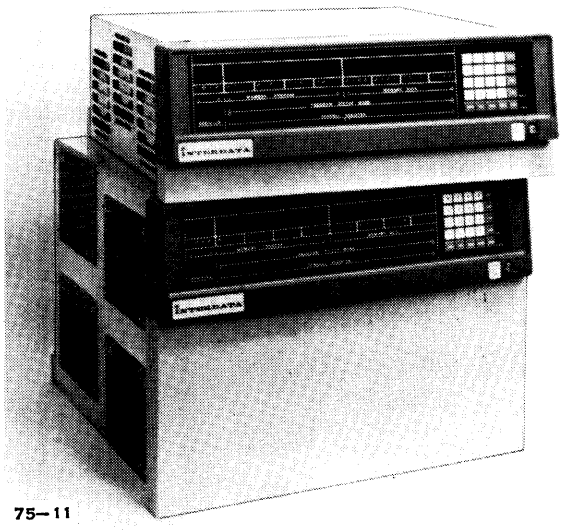

Figure G. Interdata Models 7/16 and 7/32

Table 1 summarizes the general characteristics of minicomputers. The "average" column presents a picture of the middle-of-the-line mini. Minimum and maximum columns indicate the range from very small, single task computers to very large, facility-oriented machines. A "maximum" mini would be supported with many peripherals, an operating system, and, probably, a large staff.

Table 1. Minicomputer Characteristics

	Minicomputer Size		
Characteristics	**Minimum**	**Average**	**Maximum**
Memory			
Word length (bits)	8	16	32
Type	Core or semiconductor	Core	Mixed
Size (bits)	256-4,096	To 65,536	To 262,000
Increment size (words)	256	8,192, 16,384	16,384, 32,768
Cycle time (μsec)	8	0.75-1.75	0.64 to .3
Parity check	No	Opt	Std
Memory protect	No	Opt	Std
Direct addressing (words)	±128	512-4,096	All of memory
Indirect addressing	No	Yes	Multilevel
Sub-word addressing	No	Byte, half-word	Byte, bit
Central Processor			
General-purpose registers	1, 2	2-4	To 64
Index registers	0	1-4	15
Hardware multiply/divide	Opt	Std	Std
Floating-point hardware	No	Opt	Std
Double-word instructions	No	Opt	Std
Input/Output			
Programmed I/O channel	Yes	Yes	Yes
I/O word size (bits)	8	8/16	8/16
Priority interrupt lines	1	1 std, up to 64	4 std, up to 256
Direct memory access	Opt	Std	Std
I/O maximum transfer rate, DMA (words/sec)	125,000	To/Million	To 5.0 x 10^6
Other Features			
Real-time clock	Opt	Yes	Yes
Power fail/restart	Opt	Yes	Yes
Largest disc (megawords)	4.8	9	85
Assembler	Yes (not macro)	Yes	Yes (macro)
Compiler	BASIC, FORTRAN	BASIC, FORTRAN, COBOL subset	BASIC, FORTRAN, COBOL, ALGOL
Operating system	Yes: cassette or core-based cassette	Yes: disc, tape, or core-based	Real-time, foreground/background, time sharing
Percentage of Units Installed	38	60	2
Purchase Price*	$1,000	$8,000	$22,000
Est. Annual Growth	+100%	+30%	+200%

*Purchase price is for the average computer in its class without peripherals.

Central Processor Unit (CPU)

The central processors are usually single-address, binary units with negative numbers expressed in two's complement form. Central processors vary most in the number of accessible registers, instruction sets implemented, instruction decoding technique, interrupt handling capability, and I/O facilities.

Arithmetic and logical operations are performed on data brought to the CPU from memory. The data is held and transferred between registers during these operations. A register is merely an assemblage of electronic components (flip-flops) that contain the data word while it is being processed. Some registers are accumulators (of data).

The elements of the computer are connected by buses over which data and instructions move. Generally two buses are used: one for transfers between memory and CPU and another for transfers between the CPU and its peripherals (the outside world).

Most processors use one-word instructions with the following format: 4 to 6 bits for operation code, 2 to 4 bits for modification field, and 8 or 9 bits for the address field. Most of the operation codes are used for memory referencing instructions. Non-memory referencing instructions use additional bits of the instruction word to define the operation code; thus, the number of instructions can be quite large. Most have an instruction set of 64 to 100 instructions; some have many more, over 200. The modification field further defines the instruction, usually specifying an addressing mode (indexing, indirect addressing, or both) and a literal (immediate) address; or specifying a two-word instruction. The address field provides an address increment or a literal. The effective address is calculated in accordance with the address mode; usually the contents of the program counter specify the base address and the address field specifies an increment or the core address within a page. Some minis have page registers that can be loaded with the page number of the core area from which operands are being extracted. Two-word instructions allow direct addressing of large memories — a common method of extending the addressing capability for large minis. The Interdata 7/32, for example, can address 1 million bytes of memory.

The basic instruction set usually includes the arithmetic operations of fixed-point add and subtract; multiply and divide are implemented by subroutine but usually are available with optional hardware.

Double-precision operations are sometimes provided. Most larger minis offer floating-point hardware as an option, but this feature is usually expensive. All offer some form of logical, compare, and shift operations. Many also offer byte and bit manipulation instructions. The I/O instruction is usually very general. It transfers control, status, and data words between the peripheral devices and the processor's accumulator. Commonly, the I/O instruction also provides control of optional features. They are addressed as external devices.

Classical CPU design includes a program counter, an accumulator, an accumulator extension register, and one or more index registers. Newer designs provide a number of general registers that can be used as accumulators or index registers. Sometimes a condition register keeps track of processor status with respect to overflow, operation mode, or the result of a comparison.

Some newer systems, such as the Digital PDP-11, feature two-address instructions that specify source and destination addresses calculated using the contents of general registers. This architecture lends itself to real-time processing and multiprogramming because the general registers can operate as stack pointers for stack manipulation and context switching.

Unfortunately, many manufacturers are stuck with old processor designs because of the large investment in software. Microcoding, however, has allowed some freedom; the processor can utilize modern design but emulate older systems in microcode for software compatibility. This need for compatibility places many restrictions on system design, but it does protect the users' investment in software.

Memory

Memory technology has advanced rapidly. In the early seventies, many people predicted that ferrite cores as CPU local memory would be replaced with solid-state memory. The decline in the cost of core, however, has kept core the standard for minicomputer memory. Semiconductor memory is faster, but it forgets when power is removed. A third type is Read Only Memory (ROM). As its name implies, it can only be read, not written. This restriction has two attributes: it is nominally twice as fast as a read/write memory having the same clock rate, and it is secure from inadvertent modification. Therefore, fixed, unchanging data or code can be located in ROM. Often all three types are offered by a manufacturer and can be mixed on a system.

Computer memory can be functionally divided into program storage and data storage. The CPU accesses a program instruction and then, based upon the instruction, recovers or replaces data. Besides communicating with the CPU, memory usually can communicate with I/O devices via direct-memory access (DMA) facilities. Thus, both the CPU and I/O devices share the memory bus.

Memory size can range from a few words for a small, fixed process to hundreds of thousands of words for a time-constrained major activity.[6] The addressing techniques used by the instruction set are often supplemented by special memory "mapping" hardware for very large memories. The mapping hardware provides selection of a particular block of physical memory. Memory is usually subdivided into modules of 4K, 8K, or 16K words; some vendors, such as Modular Computer and PRIME Computer, have 32K-word boards. More elegant memories have multiple ports of entry so that a module can be shared by two or more CPUs, or by a CPU and a DMA device. Multiple ports can double or triple throughput if data in one memory module can be processed while data is transfered between other memory modules and peripheral devices.

Memory word size can be extended to include provision for error recognition and correction. Simple detection is afforded by adding a parity bit. If several more bits are added to each word, special hardware can not only recognize errors but also correct them.

Memory protection can be accomplished word-by-word by adding a protect bit to each word. Area protection, using separate logic that establishes upper and lower bounds for protected memory, is much more common.

Core memory construction is very much a manual process; fine wires must be strung through the ferrite doughnuts. Consequently, memories are made in places

where labor costs are low — generally outside the United States. This construction method also makes it very expensive to thread tiny ferrite cores, and faster memory speeds are obtained by making the cores smaller. Thus, there is a natural price break for core memory with a cycle time of about 1 microsecond.

Instruction Set

The computer's instruction set defines the most primitive functions that are available to the programmer. When these operations are given mnemonic names (such as ADD for addition operator, BEQ for branch if registers equal) and combined with the rules for instruction use, the result is the machine's Assembly language.

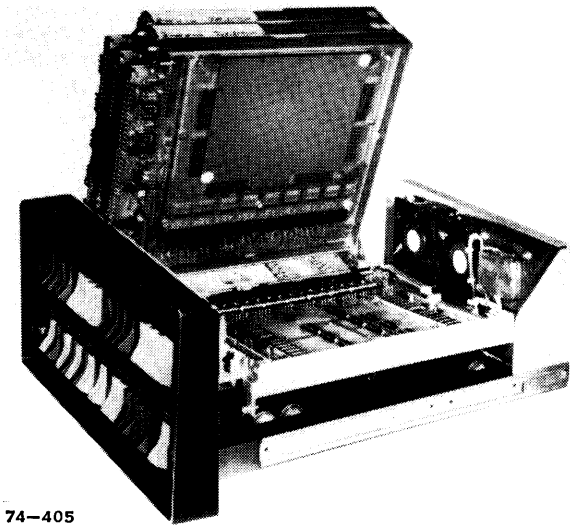

Figure H. MODCOMP II/12 with Two 32K-Word Memory Boards

A minicomputer's vocabulary usually consists of from 70 to 200 different operations, including memory reference, logical register manipulations, comparisons, and transfer instructions. The computer word has fields committed to define an operator, a memory address, and modifications to operator or address fields. Modifications to instructions may specify variations on a basic operator; modification of addresses defines indirect or indexing functions.

The computer's instruction set is usually determined by fixed wiring of electronic components within the machine. Most recent designs however, employ a concept first advanced by M. V. Wilkes in 1951.[7] Wilkes proposed that a program, that is, a sequentially executed procedure, could be brought inside the CPU and used to define the instruction set of the machine. An ADD instruction, a single operation as seen by the programmer, would actually be effected inside the CPU by a subroutine of microinstructions. Each microstep would deal with intrinsic computer operations that are more primitive than the Assembly language.

This approach, called firmware or microcode, provides a means of making changes in a computer's instruction set without scrapping the hardware design. This facility is of limited value to the user except for special circumstances, such as emulation or specialized, time critical instructions. It does permit the manufacturer, however, to extend or purify the computer's design with minimum pain. Firmware is of negative value if this approach reduces computer throughput. Within the past few years, the increased speed of logic circuits has made the technique practical. Early Interdata machines, for example the Model 3, used firmware but were slower than comparable hard-wired machines. ROM was used for its speed and security. Today, a number of manufacturers — Varian, Hewlett Packard, Prime — have

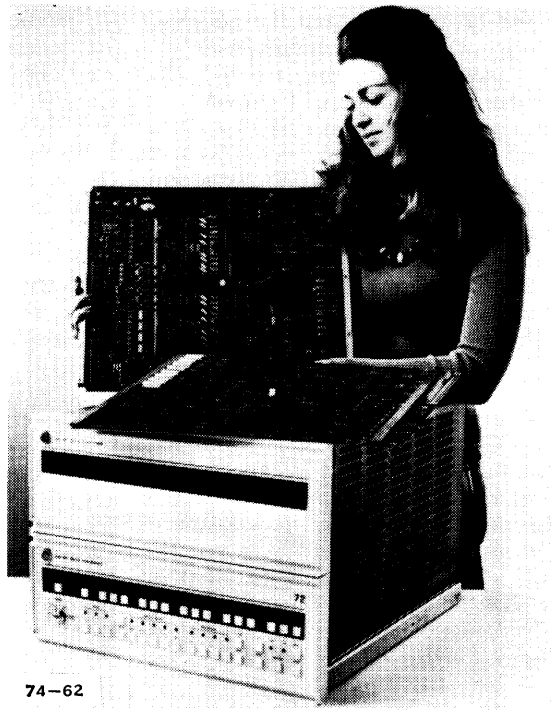

Figure I. Varian Data Machines V-72, Second in V70 Series

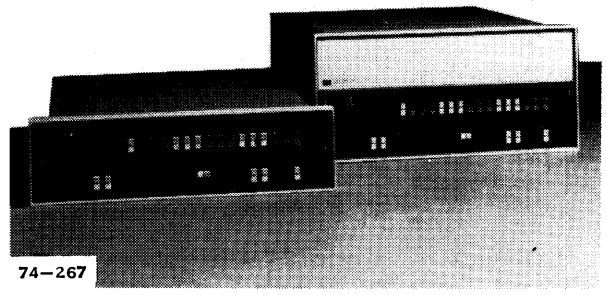

Figure J. Hewlett-Packard 21MX Computers

relaxed the read-only constraint and provide writable control store (WCS) for their systems. The speed of solid-state memory makes WCS practical. Now, for some systems, the instruction set can be modified or extended dynamically while the machine is operating.

Input/Output

Two basic means of I/O are available: programmed and automatic. The processor's data channel (or bus) is generally one word wide (16 bits for a 16-bit word processor). The channel transfers control and status information as well as data. For programmed I/O, all information is passed as a result of executing programmed instructions. For automatic I/O, control information is passed to a device controller specifying the mode of operation, the memory area involved in the transfer, and the amount of data to be passed. Once the transfer operation begins, it proceeds to completion using the DMA facility without further intervention by the program. Often, the completion of a block transfer causes an interrupt from the device controller to signal that the device is available for another transfer.

Fast devices such as tapes, discs, and drums require automatic block I/O. Slower devices can operate under either regime. Since hardware controllers for doing block I/O are relatively expensive, control information governing automatic block transfers can reside in special memory locations associated with one or more data channels, or it can reside in the device controllers.

Most minicomputer vendors provide controllers for industry standard I/O devices: high-speed paper tape units, punched card readers and punches, line printers, magnetic tape transports, plotters, displays, and Teletype units. Almost all manufacturers provide mass storage devices such as disc, drum, or tape for their products. Magnetic tape cassettes and floppy discs are among the latest offerings from the vendors. In addition, a number of independent firms offer peripherals with controllers and controller software for the popular minicomputers.[8]

Interrupt Function

The interrupt facility allows the computer to recognize the occurrence of an asynchronous external event. Then, the CPU pauses in its processing to service that event. Software analysis of the interrupt is required on the simpler minis to identify what to do. More sophisticated schemes provide a transfer vector and interrupt priorities or levels.

Interrupts include both external — outside world events — and internal — machine-generated events. Internal interrupts, sometimes called traps, include power failure sensing, illegal instructions, memory parity, memory protect, and real-time clock events.

When an interrupt is recognized, processor control is transferred to an interrupt processing routine. At this point, it is usually necessary to save the current status of all registers that will be used by the interrupt processor so they can be restored when the interrupt routine is finished. This status-saving/restoring is done automatically on a number of computers.

External interrupts are under program control and can usually be individually disabled or inhibited. A disabled interrupt level ignores an interrupt signal. An inhibited interrupt level stores the signal but does not cause an interrupt until the inhibition has been removed.

A hardware provision blocks out all interrupts until the interrupt servicing subroutine has stored the status of the processor: the contents of the accumulators, index registers, program counter, and overflow. In addition, hardware also blocks out all interrupt levels of an equal or lower priority than the one currently being serviced.

When each interrupt condition is connected to a unique interrupt level, the source is identified immediately. When several interrupt conditions are connected to a single interrupt level, additional processing is required. Some systems have a hardware provision for reading the address of the highest-priority device with a single I/O instruction. Others require a separate I/O instruction to test each device status flag. Most minis provide multiple interrupt levels; thus devices that require a fast response time can connect to unique interrupt levels, while several devices that can tolerate a longer response time are multiplexed into a lower-priority interrupt level. Some interrupt systems automatically inhibit the interrupt system from the time an interrupt is granted until the system is released by instruction. Others have hold-and-release interrupt instructions.

The efficiency of an interrupt system is determined by the time required for the overhead functions: to identify the interrupt source, to inhibit further interrupts until preliminary servicing is finished, and to initiate the interrupt service routine. These operations can be performed by hardware, software, or a combination of the two.

Software

All manufacturers supply "system software" to assist the user in developing applications programs. The minimum level of support includes a text editor, assembler, loader, and utility subroutine package. Most vendors also supply FORTRAN and BASIC language processors together with an operating system that permits their use. Such systems generally require at least 16,000 words of local memory and some form of high-speed data entry (disc, magnetic tape, or fast paper tape).

More elaborate operating systems supporting time-sharing and real-time operations are available from most

vendors. ALGOL, COBOL, and subsets of these languages are also available for some systems. At this level, diagnostics, debugging aids, and useful subroutine libraries are common.

Training

The major vendors conduct maintenance and programming courses for their customers. Typically an arrangement is made with the salesman when a customer wants to attend these sessions. Detailed reference material defining hardware and software products is generally available free from all manufacturers.

Successful minicomputer user groups that share software and product expertise are a rarity. [DECUS (Digital Equipment User's Society) is a notable exception.] Because machines are often dedicated to a single task, there has been no great pressure from users to maintain communication with each other. The impetus for such activity has been an off-again, on-again interest of the manufacturers. The trend to facility-oriented, big minis may change this situation.

APPLICATIONS

Appropriate applications for minicomputers are as numerous as leaves on a tree. The key attributes of a task to make it a candidate for solution with today's small computer technology are as follows:

- It requires computation or logical testing.
- Process is repetitive — frequently or cyclically performed.
- Manual method is either too slow or too inaccurate.
- Requirements change with time.
- Expenditure must be modest.
- Process must operate unattended.

Application areas for which minicomputers are used are so broad that whole fields of specialization develop within them. Process control applications, for example, can range from the control of a small, simple laboratory experiment to the control of a large oil refinery or chemical plant. Automating the laboratory process affects little outside the laboratory involved. Automating an oil refinery or chemical plant, however, has ramifications far beyond the computer site and can affect hundreds of people and pieces of equipment. In fact, the personnel problems in setting up a large process control center are so great that most books on the subject devote large portions of the text to ways of handling them.

Small computer applications can be divided into five broad categories, as shown in Table 2. For each application, special equipment and software have been developed and applied, depending on the size of the task in hand. Each satisfies one or more of the attributes identified previously. For further reference, the bibliography has been organized to reflect the breakdown shown in Table 2. Regardless of the nature of the task, the preeminent requirements for successful computer application are that management understand the task and make a solid commitment to the computer-based solution.

Table 2. Applications of Minicomputers

Computation
- Accounting Functions
- Sales Analysis
- Order Entry
- Inventory
- Production Scheduling
- Bill of Materials
- Engineering, Scientific Computation
- Time Sharing

Word Processing
- Key to Disc, Tape
- Text Editing
- Typesetting, Photo Composition
- Computer-Aided Design
- Computer-Aided Instruction

Communications
- Remote Batch Terminal
- Line Concentrator
- Front-End Processor
- Message Switching

Data Acquisition
- Telemetry Decommutation
- Data Reduction
- Data Conversion
- Laboratory Experiment Control
- Medical Test Analysis

Process Control
- Automatic Testing
- Numerical Tool Control
- Traffic Management

Because of their low cost, minicomputers tend to be located close to the hands of the user. Thus, minicomputer systems design must be very attentive to the human engineering of hardware and software.

Rather than look at the uses of a minicomputer from the point of view of a specific application, or vertical industry, one can look at the different ways the computer is used regardless of application. Viewed thus, minicomputers are used in the following ways:

- As stand-alone computer systems.
- As dedicated computers performing the same operation day after day.
- As modules in a hierarchical system.

As a stand-alone processing system, the computer performs a variety of functions depending on its programs. The stand-alone system can be a simple one, with small memory and a single typewriter station with slow paper tape for I/O. Software can include an assembler; a loader; I/O handlers; editing, debugging, and diagnostic routines; and some math subroutines.

On the other hand, the stand-alone system can be large and comprehensive. It could include a large internal

memory, a disc for external storage, and multiple I/O devices, such as key-entry stations, paper tape, magnetic tape, and printers. Software can include a disc operating system with control for several real-time processes in the foreground, and priority-selected batch processing facilities for programs written in an Assembler language, FORTRAN, or ALGOL in the background.

Dedicated processors can be used as an extension of the operator, who can do the job better, as in product or environmental testing, process monitoring, and data acquisition.[9] The computer interfaces directly to control or monitoring equipment and is programmed for interaction with the operator. Parameters for the function performed can be provided by the operator or by sensors. The computer acquires data, analyzes it in relationship to the parameters, and communicates the results to the operator or to equipment that it controls. In addition, the computer can prepare and maintain statistical records on data received.

A minicomputer can also function as one module in a large computer system, preprocessing data for the larger computer, handling communications among many terminals, or performing most functions on its own and calling on the large computer only when problems are too large or too complex for it to handle. These systems can be very efficient with each component performing those functions for which it is best suited.

There is a trend to decentralized systems that operate both as stand-alone computer centers and as terminals to a central facility. In this situation, a minicomputer (or smaller microprocessor) may be located at the remote sites while a larger minicomputer or maxi time-sharing system operates as the parent at the central site. This configuration is attractive to organizations with many remote offices. Large central files need to be maintained, and they are updated from the field offices periodically. Computation needs of both central and remote offices are performed by the on-site processors.

ADVANTAGES AND DISADVANTAGES OF MINICOMPUTERS

The greatest advantage of the minicomputer, in comparison to large computer systems, is that a user can buy the specific amount of computer power required for a job. The minicomputer is general-purpose and can be used to perform any function, within its size limitation, for which a program has been written. Because the overall cost is low, the minicomputer tends to be located at the problem site rather than in a computer center, and users can interact with it directly. It can be dedicated to a single problem or related set of problems. It can be fine-tuned to solve a problem as the problem should be solved. A general solution need not be adopted; a task-efficient approach is acceptable.

Generally, minicomputers are compact and rugged and do not require specialized environments. In addition, most minicomputers are as fast as, in some cases even faster than, their larger counterparts and can provide instantaneous response to an external request for service. Because a minicomputer is used by a smaller group of people, the effect of a computer malfunction is not as catastrophic as it is in a larger system. Indeed, hardware redundancy can be structured at moderate cost.

The greatest disadvantage of minicomputers to date has been the difficulty of programming because of the limited amount of software supplied with a system. This difficulty is gradually being overcome, especially for older designs. Vendors are commonly supplying operating systems that allow program development concurrent with on-line tasks.[8] Various manufacturers now supply ALGOL, FORTRAN, BASIC, and COBOL-subset language processors.

The other major disadvantage is the availability of field engineering and spare parts. This problem is endemic and not necessarily confined to new or small manufacturers. As the industry matures, more systems are being based on vendor-supplied operating systems and languages, and system software support is an important factor.

The very reliability occasioned by the move to large boards and wire-free packaging has created a spares problem. When the PDP-8 had 60 circuit boards of nine types, a spares kit could be obtained for a reasonable price. However, a spare for the Nova CPU is another complete CPU.

Other disadvantages relate to manufacturers' attempts to reduce costs. These items tend to be irritating rather than serious: switch toggles that break, lamp sockets poorly made, or inaccessible fuses and lamps. These problems tend to vary from manufacturer to manufacturer.

SELECTING A MINICOMPUTER

There is no best computer on the market, no computer has the lowest overall price/performance ratio, and no one can guarantee which computer is the best for a particular user application. On the other hand, many good computers are available, many computers have good price/performance ratios, and several computers can probably do a particular job well. The problem is to identify those computers.

Unfortunately, selecting a computer for a specific job is not easy. Still, if done without panic and without rush, the rewards of the search can include raising the staff's technical competence, understanding the individual application better, and building a firm foundation for the decision-making that will accompany future developments within the application.

The wise selection of a computer depends on the selector(s) fully understanding the application. A number

of people can be involved, but cooperation among the ultimate users is essential. The group of end users must develop a set of criteria for selecting a suitable computer; and these criteria must reflect the needs of each user's application area. Expressing these criteria in computer terms is a non-trivial task that must be accomplished, and should involve someone with a computer background. Because it is human nature for each to consider his personal needs most important, some member of the selecting group must have responsibility for leading the group toward satisfactory compromises. Such compromises might be expressed as weights applied to the selection criteria.

Developing the weighted selection criteria is an educational process and is the hardest part of the selection procedure. Application areas must be viewed in terms of what is now done, what can be done better by computers, and what can be expected in the future. Each person in the group must appreciate what computers can do from the functional point of view; each must discern that computers vary in architecture and capability; and each must understand that, whatever the hardware capability, the viability of the system is dependent on successful software.

The goal in any selection procedure is to choose a vendor or vendors that present the best combination of technical solution and system cost. Depending on the size of the project, the procedure for selection will be quite detailed or accomplished in an afternoon (with the back of an envelope for notes).

This procedure can be adjusted as necessary to suit large or small projects. The following algorithm is appropriate for selection:

- Establish minimum performance and maximum cost standards.
- Determine performance criteria, note thresholds or minimum performance levels, for example band width and speed.
- Relate performance criteria to computer and peripheral characteristics.
- Determine vendor characteristics that are important to the project.
- Assign numerical values to the quantifiable hardware and vendor characteristics.
- Rank the various characteristics and weight them, if necessary.
- Determine total cost of proposed solution — cost of vendor proposal plus cost of internal engineering, management, and programming for the proposed solution.
- Map the performance and price data developed.
- Make a subjective decision based on the clear understanding of cost and performance trade-offs provided by the objective data.

Objectivity can be maintained by setting up important criteria in advance of evaluation. Ranking or weight assignment is done before seeking vendor proposals. Objectivity is guaranteed by using measurable, quantifiable characteristics.

Cost-effectiveness requires considering all elements of a project that contribute to its cost. These factors include training, supplies, and spare parts. Note that even the FORTRAN programmer must relearn the language and the new compiler control mechanisms when moving to new hardware. An inexpensive printer that uses expensive, treated paper may not be a bargain over the system's lifetime.

The final decision is based on solid information. Subjective considerations are restricted to evaluating the importance of adequate cost and performance margins, based on maximum cost and minimum performance initially established. Observe that selection cannot be based on the notion of an absolute performance/cost evaluation. Many criteria, such as personnel experience, are situation- and time-dependent.

The difficult step in this algorithm is the conversion from task specification to computer characteristics. The selection criteria must be expressed in computer terms, and the weight applied to each criterion reflects the importance of that parameter to the particular application.

The following elements of computer systems usually form the basis for selection criteria:

- Central processor.
- Memory.
- I/O structure and channels.
- Interrupt system.
- Standard peripheral devices.
- Software.
- Manufacturer.

Central Processor and Memory

The central processor and memory determine to a large extent the computing power of a computer system. Important memory characteristics are word length, cycle time, and size. Ideally, the word length should correspond to the data precision required by the application. The cycle time determines the speed of the computer, but the user must beware of considering cycle time alone. How efficient is the instruction set for the specific application? For example, fast instruction execution may not offset a communications interface that requires several instructions for each I/O operation.

The memory size determines the complexity and size of programs the computer can run and the type of software that can be supported. Additional memory features that are often important are memory parity and memory protection.

Important central processor characteristics are the instruction set, addressing capability, speed of instruction execution, number and kind of program accessible registers, number of internal interrupts, and optional features.

If the instruction set does not include a required function such as floating-point arithmetic, software routines must perform the operation. These routines occupy memory storage space. Execution time is longer than for a comparable hardware operation. Some minicomputers have control stores (either writable or read-only) that can implement new, specialized instructions. Additional, pluggable hardware can be added to perform the required function. Floating point and fast Fourier transform processors are examples.

Memory organization can have a profound effect on the way in which software is developed. For example, the most successful mini, the PDP-8, has memory allocated in 256-word pages. An instruction can directly reference only those addresses within its page (or a base page). When working in a higher level language, the programmer is masked from such considerations, but inefficient execution times may result if program size passes certain thresholds.

The speed of instruction execution is usually a function of memory cycle time. Each instruction must be fetched from memory, and many instructions require another memory operation for data.

The number, size, and arrangement of index registers and accumulators affect the time required to do a job and the memory space required by the program. Index registers save memory references to software index registers set up in memory and thus cut down on the number of indirect references made. They can make the programmer's job easier for loop control and linking to subroutines. The number of accumulators also determines the precision of arithmetic operations, the ease with which precision can be increased, and, generally, the efficiency of the processor.

The number of internal interrupts and number of optional features offered are factors in determining the flexibility of the processor for a particular application. The selection criteria should specify all optional features required.

I/O Structure

Small computers are often tied to sensor- or operator-based systems, and the I/O structure is a major factor in evaluation. The most common I/O facility for minicomputers is a programmed party-line channel to which peripheral device controllers interface for transferring data, status information, and commands. The number of devices the channel can support and the maximum allowable length of the bus vary from CPU to CPU. Channel performance is determined by the number and kind of I/O instructions and the facilities for determining which device requires service.

I/O transfer rates are affected by the memory addressing techniques, the instructions provided for controlling and testing counters, and other factors such as the elegance of the I/O instructions. Most minicomputers have a generalized I/O instruction that is used to transfer data control words or status words between the accumulator and a peripheral device controller. The instruction set should be examined to determine how easily the processor identifies a device requiring service.

Most minicomputer systems include a direct memory access (DMA) channel to allow high-speed data transfers between peripheral devices and memory, with the data transfers under control of the channel.

Processor time devoted to I/O operations is a function of the number of peripheral devices in the system, their frequency of use, and the execution time of the software I/O routines. Requirements for the application must be carefully analyzed and the criteria defined to eliminate from consideration all computer systems that do not have minimum performance. Vendor proposals should note the number and kind of I/O channels supplied and the costs for extending these.

Interrupt System

The function of an interrupt system is to signal the processor that an untimed (untimely) event has occurred. A priority interrupt system establishes a hierarchy of importance for the attention-getting signals.

A simple interrupt configuration includes one line to which all devices interface. Software analysis is required to determine which device has caused the interrupt and what action to take. The Nova and PDP-8 machines use this scheme. The order in which interrupt servicing routines test the status of devices that can cause the interrupt establishes the priority of the devices.

A true priority interrupt system provides a number of interrupt lines, with a memory location dedicated to each line to select the interrupt servicing routine appropriate to the interrupt signal. This setup significantly decreases the response time of the processor to interrupt signals.

The priority of interrupt lines can be hardwired and fixed, or controlled by bits set in one or more programmable interrupt control registers. Programmable registers make the interrupt system more flexible — important if the various peripheral devices assume different priorities from program to program.

Normally, the instruction set includes a provision for blocking out all interrupts so that crucial processing can proceed, such as a routine to load or store the interrupt control registers. In addition, the interrupt system can block out all interrupts except those of a higher priority until an interrupt servicing routine is finished. The instruction set also includes some means of restoring the interrupt system to its state prior to the beginning of the interrupt servicing routine.

When a program is interrupted, the volatile CPU registers must be saved. This overhead may be handled in hardware or software. The method should be noted in the evaluation.

Standard Peripheral Devices

Vendor-offered peripheral devices and their delivery times may eliminate many minicomputers from consideration by the selection group. Most minicomputer manufacturers do not make all of their own peripheral devices. Instead, they buy standard devices and provide the controllers for a particular computer. Generally, the cost for peripheral devices is relatively higher than that for a processor. Recently, many new products have entered the marketplace. Costs have been dropping for two principal reasons:

- Performance standards have been moderated.
- Large minicomputer sales have permitted volume sales of peripherals.

The alphanumeric CRT/display with keyboard is a good example of how prices have been reduced.

Year	Performance	Price (interfaced)	Vendor
1967	250,000 cps	$40,000	CDC
1972	1,000 cps	3,000	Hazeltine
1975	100 cps	1,800	Digilog

The dilemma faced by the minicomputer manufacturer is which of the many new products to offer with the computer. The dilemma faced by the buyer is how many different vendors to use.

Today, the CPU manufacturer generally offers a wide variety of peripherals, but not necessarily the latest or best. The manufacturer also tends to develop and produce some peripherals, such as Hewlett Packard cartridge discs, Digital DECtapes, Data General cassettes and fixed-head discs.

Meanwhile, the popular computers are supported by many independent vendors who can supply plug-compatible devices. Often, as with a disc, significant software comes from the vendor. These peripheral vendors often are credible though some are not. In the area of peripheral evaluation, much greater emphasis should be on the device's performance in a benchmark situation since only a few devices fit the particular needs of a given project.

Interfaces Available

A majority of minicomputer manufacturers provide interfaces to standard data communications devices, to analog/digital and digital/analog devices, and to sense and signal modules. Some manufacturers specialize in these applications and have extensive hardware options as well as the software to support the equipment.

If the application requires interfaces to special-purpose devices, the selection criteria should include interface requirements. The cost of designing special-purpose interfaces can become a significant fraction of the total project cost.

Software

One of the most important components of a new computer is its software. It is critical to performance and is the most frequently underestimated, misunderstood item in the system budget. Because the cost of minicomputers is small, many minicomputers do not have extensive system software. The selection criteria should include the required software, with weights applied to the desired features for future as well as current needs. In fact, the system software supplied by the vendor controls the ease and speed of applications program development.

If the manufacturer writes off software production costs in the hardware price, the system cost increases as more system software is included. On the other hand, if the user needs system software not produced by the manufacturer of the system he buys, the cost for its development must be added to the price of his computer. This cost will be much higher than if the manufacturer distributed the software charge over many computers. In other words, well-conceived system software that is needed for an individual application is much cheaper for the user to buy from the manufacturer than to develop, and the selection criteria should reflect this view.

The user must determine the software selection criteria. Because software needs are tied to an application area as closely as hardware needs, criteria can vary from application to application. Despite the previous disclaimers, certain general software characteristics should be included in the software criteria.

Generally, the cost per line of software developed is inversely proportional to the investment in hardware. In other words, the less expensive the hardware, the more expensive it is to program. It is uneconomical, for example, for the programmer to do clerical chores such as loading a succession of paper tapes or stepping through a compiler process. If the system does not support program development, then an alternative must be identified and its cost.

System software universally includes an editor and an assembler. A variety of conventional and special-purpose compilers are available — not all from the same vendor.

Manufacturers emphasize the following features of their assemblers and compilers:

- Number of passes of the source code.
- Memory required.
- Quality of syntax checking.
- Pseudo-operation codes.
- Absolute or relocatable output code.
- User-defined macros in the Assembly language.
- Library calls and in-line Assembly code provided.

The selection committee must consider the ease and speed with which applications programs can be coded, debugged, and run on the system. An initial decision is what language should serve as a basis for development. The fundamental considerations are as follows:

- Compiler languages are superior because programs can be developed faster, documentation is better, and larger pools of trained programmers are available.
- Assembler languages produce more efficient code.
- Some languages will not be available on otherwise superior equipment.
- Compilers require operating systems for support. Larger, more elegant languages often are not acceptable in the user environment until many months after their first release (caveat emptor).

Most assemblers require a minimum of two passes of the source code to produce an assembled program, and a so-called one-pass assembler either leaves many references to be resolved by a loader or is a two-pass assembler, which does not require the source code to be read from an input device twice. The first pass checks the source code for syntactic errors and builds the symbol table in memory. The second pass completes the assembly and tags unresolved references for the loader. The language compiler adds one translation pass at the front end of this process.

Utility routines should be supplied for arithmetic and data conversion and for source code debugging. I/O handlers should be provided. Loaders should be furnished for all software supplied with the system and all applications programs.

System software should include diagnostic routines for system maintenance. Tests should be provided to check the operation of every unit in the system and to diagnose malfunctions within those units supplied as spare parts. Many manufacturers provide software on a modular basis. Each module requires a specific minimum hardware configuration, number of memory locations, optional features, interrupt lines, mass storage, and peripheral devices.

Operating systems for minicomputers are becoming increasingly important, particularly for systems that include mass storage devices. Most operating systems are of the foreground/background type; one or more real-time programs can be executed in the foreground and one batch program can be executed in the background. Batch background programs are sometimes priority-oriented. Time-sharing operating systems for minicomputers are also available from major minicomputer manufacturers and some independent vendors.[10]

Foreground/background operating systems make minicomputers suitable for real-time control applications, and increase the efficiency of the overall computing system. Real-time programs are incorporated into the operating system and are executed in the foreground, while batch programs can be executed during leftover processor time in the background. The important feature of these systems for control applications is that new real-time programs can be debugged and prepared for incorporation in the operating system without closing down the system.

Time-sharing operating systems are a variation of the foreground/background operating systems. Instead of real-time control programs being executed in the foreground, all time-sharing users are in the foreground.

Operating systems vary in complexity, depending on the kinds of applications for which they were designed. Most manufacturers who include operating systems in their software packages offer modular systems with more features available as the hardware configuration increases in size. Operating systems handle the following functions:

- Communication between the operator and the system.
- I/O.
- Servicing of the interrupt system.
- File definition and manipulation.
- Processor status.
- Initiation of program execution.
- Core assignment.

User programs have access to the preceeding facilities only through the operating system to ensure against inadvertent destruction of the programs in core.

System generation permits tailoring the operating system to a particular hardware configuration. Only those modules required by the application are incorporated into the operating system for that application. For example, if the hardware configuration includes no magnetic tape units, no magnetic tape handler programs are loaded. System generation occurs only once for an installation unless new equipment is added.

Organization of the operating system depends on the type of system. Foreground/background real-time systems execute programs on a priority basis; the priority of each program application is assigned on the basis of the required response time. The execution time of real-time programs is usually short, and any long calculations are performed by background programs. Background programs can be executed in the order received by the operating system, or programs can be executed in accordance with an assigned priority that can be changed by the operator via the console or control cards.

Time-sharing systems can assume all users have equal priority and allocate a time slice to each one. Alternatively, the time-sharing system can assume that some users have higher priority than others; and the programs of high-priority users are permitted to run to completion.

Communication between the operator and the system can be via a Teletype keyboard/printer, card or tape reader and punch, and/or line printer. The operating

system includes an interpreter routine that decodes messages from and generates messages to the operator. The communications codes provided limit an operator's control over the system.

Operating systems handle all I/O for the system; users specify their I/O via logical unit numbers. The operating system maintains queues for the use of I/O devices and overlaps I/O operations with processing.

The manufacturer designing the operating system makes various assumptions on which to base the system. These assumptions or system parameters are based on the hardware and the application for which the hardware will be used; they include such factors as the average core storage required by a foreground or background problem, the maximum number of foreground problems, the maximum number of priority levels allowed, the type of programs that can be run in the foreground and background, and the system software a user can utilize. Thus, a particular operating system can be too big and complex, too small and simpleminded, or about right for a particular application, depending on the parameters used in the system design. The selection criteria must spell out the minimum facilities required of the operating system.

The structures of various files are based on the anticipated needs of the applications for which the system was designed. The means for addressing, changing, and adding to files should be examined in the light of the file use for an application.

The operating system allocates memory for all programs executed. Normally, the memory map includes three main areas; one area is assigned to the resident portion of the operating system, another area is assigned to the resident applications programs, and the third area is assigned for temporary use by all other executing programs — whether system or user. The amount of memory devoted to resident applications programs and to temporary programs determines the size of programs that can be run. If the temporary storage area is too small for applications programs or for the required systems programs, then more memory must be added.

Manufacturers also emphasize the system software packages that can run under the operating system, the ease of inserting programs into the batch stream, the protection safeguards for users files, and the facilities for segmenting large programs into a size that can be handled by the system.

In general, when considering operating systems, the judgement criteria are not very different from those used in evaluating operating systems of larger computers. Usually, the small computer system must respond to new requirements, however. Some insight into operating system organization or methods for making additions — specifically in the I/O area — is desirable.

Qualifications of the Manufacturer

The characteristics attributed to the manufacturer supplying the system are important in selecting a system because users require many services from this manufacturer. Consideration should also be given to the following factors:

- Reputation of the sales personnel.
- Delivery schedules and reputation for meeting them.
- Maintenance, distance of computer site from manufacturer or service center, and quality of the field engineering staff.
- Software support available for applications programming.
- Number of systems delivered.
- Quality of documentation on hardware and software.
- Training provided.
- General reputation of the hardware and software.
- Financial health of the vendor.

Settling on a System

At this point, the selection criteria should include only those features that are relevant to the application. Some criteria are critical; these must be identified, and all computers without the critical features should be ignored. From the selection criteria, the selection committee should make up a hardware list and, using AUERBACH reports or other computer surveys, select a group of manufacturers that can do the job.

The committee can calculate hardware costs from price lists or seek bids from the manufacturers of acceptable computers. Seeking bids is preferable if special equipment, special services, or a competitive bid is required.

The first step is to solicit the "long list," which describes the functional requirements and requests a response of qualification and interest in bidding. From this information the "short list" of three to six vendors will do; these are asked for a formal proposal.

Using the performance criteria described previously, the next step is to calculate the system performance for all acceptable computers:

$$P_c = \sum_{i=1}^{N} W_i \; S_i$$

where P = system performance
c = a particular computer system
i = a selection criterion for an application
N = the total number of selection criteria for that application
W = criterion weight
S = implementation scale factor. [11]

A unique performance number (P) can now be associated with each acceptable computer system.

When the proposals for the computer hardware are received, the selection committee can compute a total system price. This price includes the manufacturer's system price plus the estimated in-house costs for programming, hardware, and operations. Once the total system costs for all proposed systems are obtained, the price/performance ratios are calculated for each by dividing total system cost by the performance number.

Logically, using this method, the selection committee selects the computer with the lowest price/performance ratio (PPR). Other factors, however, can dictate selecting some other system. The total system cost in relationship to the computer budget, for example, might force the selection of a lower-priced computer with a higher price/performance ratio. If two computers are roughly equivalent, the committee might select one over the other because of delivery schedules. Having performed the analysis described in the preceding paragraphs, the selection committee can make decisions on a sound analytical basis, and that is the main advantage of this approach.

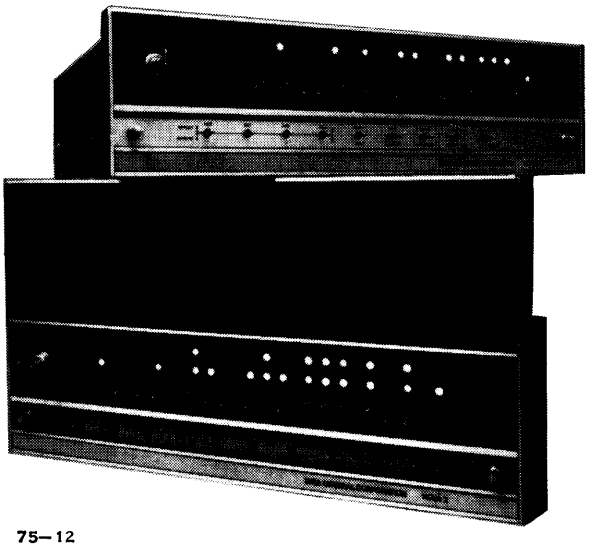

Figure K. Data General Nova 2/4 and 2/10

FUTURE DEVELOPMENTS

The rise of minicomputer technology has been explosive. The diversification of equipment and applications has been dramatic since 1968. Viewed from the standpoint of the problem to be solved, the history of computing technology can be described as follows:

Pre-history	Mechanical computing; abacus to Hollerith.
50's	Widespread computation, but unreliable and expensive.
60's	Centralized large computers with languages and operating systems: problems forced to conform to batch processing regimes.
70's	Decentralized task-oriented processing, using language and processors scaled to the task.
Beyond	Further melding of hardware and software techniques, with highly individual designs extending into the CPU itself.

It is a fact that minicomputer manufacturers are selling larger average systems. One minicomputer manufacturer spokesman notes that the average system now shipped is valued at $37,000. Four years ago it was only $14,000. More system software and more peripherals are available. The basic small computer is still very much the big seller; but it has larger cousins now. The genealogy can be observed by looking at Data General as an example of the industry trend maker: first the Nova, then the Supernova; the line was subsequently filled out with Nova 800 and Nova 1200, then the "hairy" (big) 840; all software compatible; followed by the tiny Nova 2/4 and 2/10; now the much grander ECLIPSE. Another example is Varian: first came the simple 620A, then the fast 620F, next the economical L100, and finally the V70 Series; all software upward compatible.

The glamour and promotion are concentrated on the maxi-mini and the new compilers, but this rising scale of grandeur is deceptive. At the other end of the spectrum, history is repeating itself. As the mini has challenged large computer designers, now the microprocessor challenges the established minicomputers. The burgeoning activity centers on a new set of suppliers — the computer-on-a-chip vendors who are producing scaled-down minicomputers. The decade ahead should see far greater emphasis on system engineering, task-oriented design than was ever true for minicomputer design. The fortunate user can now choose from an almost complete spectrum of solutions for a problem and truly find just the right amount of hardware and software to do the job.

Figure L. Data General ECLIPSE® Computer

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MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE			WORD LENGTH (Bits)				MAX MEM (Bytes)			PERIPHERALS			SOFTWARE		MAJOR MARKETS					
		Process Control	Microcomputers	Minicomputers	8	12	16/18	24/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
ACEC-92	68						•				•	•			•	•						•
AEG 60-07	72			•	•				•			•					•					•
60-10	69			•		•				•		•	•		•		•					•
60-50	68			•				•			•	•			•	•	•					•
TR 86				•				•			•	•					•					•
AI-Denshi Sokki																						
Aicom-C4	70						•			•		•	•			•						•
C4P	71						•			•		•	•			•						•
C5	72						•			•		•	•	•		•						•
American Microsystems, Inc.																						
AMI 6800	74		•		•				•			•	•	•		•					•	
Applied Computing Technology																						
PPS-4MP	73		•						•						•						•	
UMPS-4	73		•						•						•						•	
Applied Data Communications																						
70-100	75		•		•					•		•	•	•	•						•	
Applied Systems																						
ASC/8	74		•		•							•	•	•	•						•	
Arcturus 18C	71						•				•	•	•	•						•		
18D	73			•			•			•		•	•	•						•		
Brown-Boveri																						
DP 100	69						•					•	•	•	•	•	•					
DP 1000	72						•			•					•		•					
Burnt Hill																						
Electronics 204	70						•			•										•		
Canon-Jimuki																						
Canon BP-1000	71							•	•							•						•
Pasca 2500	72							•	•			•										•
Chuo-Denshi																						
CEC 555	68						•			•		•				•						•
CEC 5555	69						•		•			•	•	•		•						•
CEC 5557	70						•		•			•	•	•		•						•
CEC 555M	71						•				•					•						•
CEC 555H	71						•				•					•						•
CDC																						
SC1700	69			•			•			•		•	•	•	•	•	•	•	•	•	•	•
1704	66			•			•			•		•	•	•	•	•	•	•	•	•	•	•
1714	72			•			•				•	•	•	•	•	•	•	•	•	•	•	•
1784 System 17	73			•			•				•	•	•	•	•	•					•	
CII 10010					•					•		•		•	•	•	•	•		•		•
10020							•				•	•	•	•	•	•	•	•				
Mitra 15/20	71			•			•		•			•		•	•	•	•	•		•		•
Mitra 15/21	71			•			•			•		•		•	•	•	•	•		•		•
Mitra 15/30	71			•			•			•		•		•	•	•	•	•		•		•
Mitra/125	75			•			•				•	•		•	•	•	•	•		•		•
Cincinnati Milacron																						
CIP/2200	72			•			•			•		•	•	•	•						•	
Computer Automation																						
LSI 2/10	73			•			•			•		•	•	•	•	•	•	•		•	•	•
LSI-2/20	73			•			•			•		•	•	•	•	•	•	•		•	•	•

MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE			WORD LENGTH (Bits)				MAX MEM (Bytes)			PERIPHERALS			SOFTWARE		MAJOR MARKETS					
		Process Control	Microcomputers	Minicomputers	8	12	16/18	24/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
Computer Automation (Contd.)																						
LSI-2/60 (megabytes)	75			●			●				●	●	●	●	●	●	●	●		●	●	●
LSI-3/05	75			●			●		●	●		●			●		●	●		●	●	●
LSI-3/05A	75			●			●		●			●	●	●		●	●	●		●	●	●
LSI-3/05B	75			●			●		●			●	●	●		●	●	●		●	●	●
LSI-3/05C	75			●			●		●			●	●	●		●	●	●		●	●	●
Alpha/LSI	73			●			●			●		●	●	●	●	●	●	●		●	●	●
Naked Mini	73			●			●			●		●	●	●	●	●	●	●		●	●	●
Computer Signal Processors																						
CSP-30	70			●			●				●	●	●								●	
CSP-125	73			●			●				●	●	●								●	●
Computer Technology																						
MiniMod	73			●			●				●	●	●	●	●	●		●		●		
Modular One	68			●			●				●	●	●	●	●	●		●		●	●	
Control Logic																						
L series	73		●		●				●					●	●						●	
M series	74		●		●				●					●	●						●	
Cramer Electronics																						
CRAMERKIT	75		●		●				●					●	●						●	
Data General																						
ECLIPSE S/100	75			●			●			●		●	●	●	●	●	●	●	●	●	●	●
ECLIPSE S/200	75			●			●				●	●	●	●	●	●	●	●	●	●	●	●
Nova 2/4, 2/10	73			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Nova 3/4	75			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Nova 3/12	75			●			●				●	●	●	●	●	●	●	●	●	●	●	●
Nova 800	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Nova 820	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Nova 830	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
Nova 840	73			●			●				●	●	●	●	●	●	●	●	●	●	●	●
Nova 1200	70			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Nova 1210	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Nova 1220	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Supernova	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Supernova SC	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Datamate Computer																						
DM-16	69			●			●			●		●	●	●		●					●	
DM-70	70			●			●			●		●	●	●		●					●	
Data Numerics																						
DL8A	75		●		●					●			●								●	
Datasaab D5	70			●			●				●	●	●	●	●	●	●					●
D21	65							●			●	●	●	●	●	●	●					●
Dietz Minca																						
513	69			●			●		●			●			●		●					
523	69			●			●			●		●	●		●		●					●
621	71			●	●		●				●	●	●	●	●	●	●	(1)	(1)			●
1600	73						●			●		●	●	●	●	●	●					●
Digico Micro																						
16	68			●			●			●					●	●	●			●		
16-P	70			●			●				●	●	●	●	●	●	●			●		
16V	72			●			●				●	●	●	●	●	●	●			●		

MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE: Process Control	COVERAGE: Microcomputers	COVERAGE: Minicomputers	WORD LENGTH (Bits): 8	WORD LENGTH (Bits): 12	WORD LENGTH (Bits): 16/18	WORD LENGTH (Bits): 24/32	MAX MEM (Bytes): 32K	MAX MEM (Bytes): 32-64K	MAX MEM (Bytes): 64K	PERIPHERALS: Disc/Drum	PERIPHERALS: Mag Tape	PERIPHERALS: Data Comm	SOFTWARE: Oper Sys	SOFTWARE: Fortran/Algol	MAJOR MARKETS: Germany	MAJOR MARKETS: France	MAJOR MARKETS: Italy	MAJOR MARKETS: U.K.	MAJOR MARKETS: U.S.A.	MAJOR MARKETS: Other
Digital Computer Controls																						
D-112	70			●		●				●		●	●	●							●	
D-112H/SC	72			●		●				●		●	●	●							●	
D-116	72			●			●			●		●	●	●							●	
D-216	75			●			●			●		●	●	●	●	●					●	
D-316	75			●			●			●		●	●	●	●	●					●	
D-416	75			●			●			●		●	●	●	●	●					●	
D-616	75			●			●				●	●	●	●	●	●					●	
Digital Equipment																						
MPS Series	74		●	●	●				●			●	●	●	●	●	●	●	●	●	●	●
PDP-8/A	74			●		●				●		●	●	●	●	●	●	●	●	●	●	●
Super 8	75			●		●				●		●	●	●	●	●	●	●	●	●	●	●
PDP-8/E	70			●		●				●	●	●	●	●	●	●	●	●	●	●	●	●
PDP-8/F	72			●		●			●	C		●	●	●	●	●	●	●	●	●	●	●
PDP-8/M	71			●		●				●		●	●	●	●	●	●	●	●	●	●	●
LSI-11	75			●			●			●		●	●	●			●	●	●	●	●	●
PDP 11/03	75			●			●			●		●	●	●			●	●	●	●	●	●
PDP-11/04	75			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11/05	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11/10	72			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11E/10	73			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11/15	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11/20	70			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11/R20	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11/35	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
PDP-11/40	72			●			●				●	●	●	●	●	●	●	●	●	●	●	●
PDP-11/45	72			●			●				●	●	●	●	●	●	●	●	●	●	●	●
PDP-11/50	73			●			●			●		●	●	●	●	●	●	●	●	●	●	●
PDP-11/70	75			●			●				●	●	●	●	●	●	●	●	●	●	●	●
PDP-12	70			●		●				●		●	●	●	●	●	●	●	●	●	●	●
PDP-15/10	70			●			●		●			●					●	●	●	●	●	●
PDP-15/20	70			●			●		●			●	●	●	●	●	●	●	●	●	●	●
PDP-15/30	70			●			●		●		●	●	●	●	●	●	●	●	●	●	●	●
PDP-15/35	70			●			●		●		●	●	●	●	●	●	●	●	●	●	●	●
PDP-15/40	70			●			●		●		●	●	●	●	●	●	●	●	●	●	●	●
PDP-15/50	71			●			●		●		●	●	●	●	●	●	●	●	●	●	●	●
PDP-15/70	72			●			●				●	●	●	●	●	●	●	●	●	●	●	●
PDP-15/76	72			●			●				●	●	●	●	●	●	●	●	●	●	●	●
PDP-15/78	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
PDP-VMS	75			●			●				●	●	●	●	●	●	●	●	●	●	●	●
Digital Laboratories PB 96	74		●		●					●		●		●	●						●	
Digital Scientific																						
META 4	70			●			●				●	●			●	●					●	
Elbit 100						●			●			●					●	●				●
Electronic Associates																						
EAI PACER 100	72			●			●			●		●	●	●	●	●	●	●	●	●	●	●
Electronic Processors																						
EPI-118	70			●			●				●	●	●	●	●	●					●	
EPI-218	72			●			●				●	●	●	●	●	●					●	

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		Process Control	Microcomputers	Minicomputers	8	12	16/18	24/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
Fabritek MP 12	74		•			•			•				•	•	•	•					•	
Fairchild Semiconductor																						
F8S-Simboard	75		•		•				•												•	
F8-C	75		•		•				•						•						•	
Ferranti Argus 400								•			•	•		•	•	•	•	•		•		•
500	68			•				•			•	•		•	•	•	•	•		•		•
600	70			•	•				•		•	•		•	•	•	•	•		•		•
700E	74			•			•				•	•	•	•	•	•	•	•		•		
700S	73			•			•				•	•	•	•	•	•	•	•		•		
700T1	74			•			•			•		•	•	•	•	•	•	•		•		
700T2	74			•			•			•		•	•	•	•	•	•	•		•		
Foxboro																						
FOX 1	71	•						•			•	•			•	•	•	•	•	•	•	•
FOX 2/10	72	•					•			•		•			•	•	•	•	•	•	•	•
FOX 2/30	72	•					•			•		•			•	•	•	•	•	•	•	•
Fujitsu Facom R	69						•				•	•	•	•		•					•	•
Facom R/R-E	70						•				•	•	•	•		•					•	•
Facom Mate II	73			•			•			•		•	•		•	•						•
U-200	72			•			•				•	•	•		•	•						•
GEC																						
903	66						•				•		•		•	•	•	•		•		•
905	69			•			•				•	•	•	•	•	•	•	•		•		•
2050	72			•	•					•		•		•			•	•		•		•
4080	72			•	•						•	•	•	•	•	•	•	•		•		•
M.2140	69						•				•	•	•	•	•	•				•		
Myriad	65							•			•	•		•		•				•		
General Automation																						
GA-8/55	75		•		•					•				•			•	•	•	•	•	•
GA-16/110	75			•			•				•	•	•	•	•	•	•	•	•	•	•	•
GA-16/220	76			•			•				•	•	•	•	•	•	•	•	•	•	•	•
GA-16/330	76			•			•				•	•	•	•	•	•	•	•	•	•	•	•
GA-16/440	75			•			•				•	•	•	•	•	•	•	•	•	•	•	•
GA-18/30	69			•			•			•		•	•	•	•	•	•	•	•	•	•	•
SPC-12	68			•	•				•					•	•		•	•	•	•	•	•
SPC-12/10	71			•	•				•			•	•	•	•		•	•	•	•	•	•
SPC-12/15	71			•	•				•			•	•	•	•		•	•	•	•	•	•
SPC-12/20	71			•	•				•			•	•	•	•		•	•	•	•	•	•
SPC-16	70			•			•				•	•	•	•	•	•	•	•	•	•	•	•
SPC-16/40	71			•			•			•		•	•	•	•		•	•	•	•	•	•
SPC-16/45	71			•			•			•		•	•	•	•		•	•	•	•	•	•
SPC-16/60	71			•			•			•		•	•	•	•		•	•	•	•	•	•
SPC-16/65	71			•			•			•		•	•	•	•		•	•	•	•	•	•
SPC-16/80	71			•			•			•		•	•	•	•		•	•	•	•	•	•
SPC-16/85	71			•			•			•		•	•	•	•		•	•	•	•	•	•
General Instruments																						
GIC 1600	75		•				•			•				•	•						•	
GIC 1601	75		•				•			•				•	•						•	
GRI Computer																						
GRI-99, Model 10	72			•			•			•			•				•	•		•	•	

MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE			WORD LENGTH (Bits)				MAX MEM (Bytes)			PERIPHERALS			SOFTWARE		MAJOR MARKETS					
		Process Control	Microcomputers	Minicomputers	8	12	16/18	24/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
GRI Computer (Contd.)																						
Model 30	72			●			●			●			●		●		●	●		●	●	
Model 40	72			●			●			●			●		●		●	●		●	●	
Model 50	74			●			●			●		●	●	●	●	●	●	●		●	●	
GTE Information Systems																						
IS/1011	75		●		●						●										●	
IS/1014	74		●		●		●		●												●	
Harris																						
Slash 1	69			●				●			●	●	●	●	●	●	●	●		●	●	●
Slash 3	72			●				●			●	●	●	●	●	●	●	●		●	●	●
Slash 4	73			●				●			●	●	●	●	●	●	●	●		●	●	●
Slash 4VMS	74			●				●			●	●	●	●	●	●	●	●		●	●	●
Slash 5	72			●				●			●	●	●	●	●	●	●	●		●	●	●
Slash 5R	73			●				●			●	●	●	●	●	●	●	●		●	●	●
Slash 7	75			●				●			●	●	●	●	●	●	●	●			●	●
S110	75			●				●			●	●	●	●	●	●	●	●			●	●
S120	75			●				●			●	●	●	●	●	●	●	●			●	●
S210	75			●				●			●	●	●	●	●	●	●	●			●	●
S220	75			●				●			●	●	●	●	●	●	●	●			●	●
S230	75			●				●			●	●	●	●	●	●	●	●			●	●
S240	75			●				●			●	●	●	●	●	●	●	●			●	●
Hewlett-Packard	72			●			●				●	●	●	●	●	●	●	●			●	●
Access/2000	75			●			●			●		●	●	●	●	●	●	●	●	●	●	●
HP 2100A	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
HP 2100S	72			●			●			●		●	●	●	●	●	●	●	●	●	●	●
HP 21MX	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
HP 3000CX	74			●																		
50CX	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
100CX	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
200CX	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
300CX	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
HP 9500	70	●					●				●	●	●	●	●	●	●	●	●	●	●	●
9700	73	●					●				●	●	●	●	●	●	●	●	●	●	●	●
Hitachi																						
Hitac 10	69						●			●		●	●	●		●					●	
Hitac 20	75			●			●			●		●		●	●	●						●
Hitac Mini	71						●		●							●					●	●
Hokushin Hoc 700E	71						●				●	●			●	●						●
Hollinbeck Enterprises																						
MP-68	75		●		●					●		●		●	●						●	
MP-11	75		●				●			●		●		●	●	●					●	
Honeywell																						
DDP-516	67			●			●			●		●	●	●	●	●	●	●	●	●	●	●
H112	69			●		●			●								●	●	●	●	●	●
H316	69			●			●			●		●	●	●	●	●	●	●	●	●	●	●
HPAC 4010	70	●						●			●	●		●	●	●				●	●	
HPAC 4020	67	●						●			●	●		●	●	●				●	●	
HPAC 4400	75	●						●			●	●	●	●	●	●				●	●	
System 700	72			●			●		●		●	●	●	●	●	●	●	●	●	●	●	●

MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE			WORD LENGTH (Bits)				MAX MEM (Bytes)			PERIPHERALS			SOFTWARE		MAJOR MARKETS					
		Process Control	Microcomputers	Minicomputers	8	12	16/18	24/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
Honeywell (Contd.)																						
725-G, S, M	74			●			●			●		●	●	●	●	●	●	●	●	●	●	●
735-G, S	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
IBM																						
1130	65			●			●			●		●	●	●	●	●	●	●	●	●	●	●
1800	66			●			●			●	●	●	●	●	●	●	●	●	●	●	●	●
System/7	71			●			●				●	●	●	●	●	●	●	●	●	●	●	●
ICS Multum	72			●			●				●	●	●	●	●	●				●		
Informatek																						
Matek 1026	72						●				●	●	●	●	●	●		●				
Intel																						
8008-1	71		●		●				●									●			●	●
8080	73		●		●					●								●			●	●
3001	75		●															●			●	●
Interdata																						
Model 1	70			●	●				●			●	●	●			●			●	●	●
Model 70	71			●			●			●		●	●	●	●	●	●			●	●	●
Model 74	73			●			●			●		●	●	●	●	●	●			●	●	●
Model 80	71			●			●			●		●	●	●	●	●	●			●	●	●
Model 85	73			●			●			●		●	●	●	●	●	●			●	●	●
RD-800	75			●			●			●		●	●	●	●	●	●			●	●	●
RD-850	75			●			●			●		●	●	●	●	●	●			●	●	●
7/16	74			●			●			●		●	●	●	●	●	●			●	●	●
7/32	74			●			●				●	●	●	●	●	●	●			●	●	●
8/32	75			●				●			●	●	●	●	●	●	●			●	●	●
Intertechnique																						
Multi-2	75		●														●	●	●	●		●
Multi-4	73			●	●				●								●	●	●	●		●
Multi-4/01	74			●			●		●			●	●		●	●	●	●	●	●		●
Multi-4/02	74			●			●		●			●	●		●	●	●	●	●	●		●
Multi-4/05	74			●			●		●			●	●	●	●	●	●	●	●	●		●
Multi-4/M.301	74						●		●			●	●		●		●	●	●	●		●
Multi-4/M.302	74						●		●			●	●		●		●	●	●	●		●
Multi-4/M.305	74						●		●			●	●	●	●		●	●	●	●		●
Multi-6	75			●													●	●	●	●		●
Multi-8	69			●	●					●							●	●	●	●		●
Multi-8M.301	70			●			●			●		●	●		●	●	●	●	●	●		●
Multi-8M.302	70			●			●			●		●	●		●	●	●	●	●	●		●
Multi-8M.304	70			●			●			●		●	●	●	●	●	●	●	●	●		●
Multi-8M.350	71			●			●			●		●	●		●	●	●	●	●	●		●
Multi-20	72			●	●						●	●	●		●	●	●	●	●	●		●
Multi-20/01	72			●			●				●	●	●		●	●	●	●	●	●		●
Multi-20/05	72			●			●				●	●	●		●	●	●	●	●	●		●
Multi-20/06	72			●			●				●	●	●	●	●	●	●	●	●	●		●
ITT System 310																						
Keronix IDS 16M	75		●				●			●					●	●		●	●		●	●
Krantz Elektronik																						
MULBY 3/30, 3/35	73				●					●		●	●	●	●	●	●					
Krupp EPR 1100	73					●					●	●	●		●		●					

MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE			WORD LENGTH (Bits)				MAX MEM (Bytes)			PERIPHERALS			SOFTWARE		MAJOR MARKETS					
		Process Control	Microcomputers	Minicomputers	8	12	16/18	23/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
Laben 70																						
701	73					•	•			•		•	•		•	•			•			•
Leeds & Northrup																						
LN 5400	74	•					•				•	•	•	•	•	•	•	•	•	•	•	•
Lockheed Electronics																						
MAC 16	69			•			•				•	•	•	•	•	•	•			•	•	
MAC Jr	70			•			•				•	•	•	•	•	•	•			•	•	
SUE 1110	71			•			•			•		•	•	•							•	
SUE 1111 (System III)	72			•			•			•		•	•	•							•	
SUE 1112	72			•			•			•		•	•	•							•	
Marme GMG 5000	72						•			•		•	•					•				
Martin Research																						
AT 804-3	75		•		•				•			•	•	•	•						•	
AT 811-3	75		•		•					•		•	•	•	•						•	
Matsushita-Tshushin																						
MACC-7/S	70						•		•			•	•	•		•						•
MACC-7/F	71						•		•			•	•	•		•						•
MB Metals K-202	72				•						•	•	•	•	•	•				•		•
Micro Computer Machines MCM/70	75		•		•				•			•		•	•						•	
Micro Computer Systems MINIC	71			•	•						•	•	•	•						•		
Micro Consultants																						
1601	71			•			•			•		•								•		
Microdata																						
Micro-One	74			•	•					•											•	
Micro 400	70			•	•						•	•	•	•							•	
Micro 800 Series	69			•	•					•	•	•	•	•							•	
Micro 1600 Series	71			•	•					•		•	•	•							•	
3200	73			•			•				•	•	•	•	•						•	
32/S	74			•			•				•	•	•	•							•	
MICROKIT 8/16	75		•		•					•			•	•	•						•	
MITS Altair 8800	75		•		•				•			•			•						•	
Mitsubishi Denki																						
MELCOM 70	71						•				•	•	•	•	•	•						•
MELCOM 83	69							•	•			•	•	•								•
Modular Computer MODCOMP																						
I/5	71			•			•			•		•	•	•	•	•	•	•		•	•	
I/15	71			•			•			•		•	•	•	•	•	•	•		•	•	
II/5	72			•			•			•		•	•	•	•	•	•	•		•	•	
II/10	72			•			•			•		•	•	•	•	•	•	•		•	•	
II/12	74			•			•				•	•	•	•	•	•	•	•		•	•	•
II/20	72			•			•				•	•	•	•	•	•	•	•		•	•	
II/25	72			•			•				•	•	•	•	•	•	•	•		•	•	
II/26	74			•			•				•	•	•	•	•	•	•	•		•	•	•
II/26CP	74			•			•				•	•	•	•	•	•	•	•		•	•	•
II/201	74			•			•				•	•	•	•	•	•	•	•		•	•	•
II/221	74			•			•				•	•	•	•	•	•	•	•		•	•	•
II/231	74			•			•				•	•	•	•	•	•	•	•		•	•	•
III/5	72			•			•				•	•	•	•	•	•	•	•		•	•	
IV/10	73			•			•				•	•	•	•	•	•	•	•		•	•	

MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE			WORD LENGTH (Bits)				MAX MEM (Bytes)			PERIPHERALS			SOFTWARE		MAJOR MARKETS					
		Process Control	Microcomputers	Minicomputers	8	12	16/18	24/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
Modular Computer MODCOMP (Contd.)																						
IV/25	73			•			•				•	•	•	•	•	•	•	•		•	•	
Monolithic Memories MMI 300			•				•		•						•						•	
Motorola 6800	74		•		•				•					•	•	•					•	
Mycro-Tek, Inc. MT 8080 PR	75		•		•				•			•			•						•	
National Semiconductor																						
PACR	75		•			•			•					•							•	
IMP 16	72		•			•			•					•							•	
Nihon-Denki																						
NEAC-M4	69							•		•		•				•						•
NEAC 3200 M30	71						•		•			•		•		•						•
NEAC 3200 M50	71						•			•		•		•		•						•
JEC 5							•		•							•						•
Nihon Minicon																						
(Nova) N-Model 01							•			•		•	•	•		•						•
(Nova) N-Model 02							•			•		•	•	•		•						•
(Nova) N-Model 03/SO							•			•		•	•	•		•						•
Nihon Musen																						
JAC 120M-520	70							•		•		•	•	•		•						•
Nord 1	69						•				•	•	•	•	•	•	•			•		•
5, 10, 20	73			•			•				•	•	•	•	•	•						•
Nuclear Data																						
ND 812	70			•		•			•			•	•								•	
Oki-Denki																						
OKITAC 4300S	69						•			•		•	•	•	•	•						•
OKITAC 4300E	69						•			•		•	•	•	•	•						•
OKITAC 4500	70						•				•	•	•	•	•	•						•
OKITAC 4000	71						•				•	•	•	•	•	•						•
Ordoprocesseurs																						
Ordo 16A	71			•			•		•					•				•				
MF 300	71						•		•				•	•	•			•				
PCS Micropac 80	74		•		•					•				•	•						•	
Micropac 80/A	75		•		•					•				•	•						•	
Philips Electrologica																						
P850	71			•			•		•								•	•	•	•	•	•
P850M	73			•			•		•								•	•	•	•	•	•
P852M	74			•			•			•		•	•	•	•	•	•	•	•	•	•	•
P855M	73			•			•			•		•	•	•	•	•	•	•	•	•	•	•
P856M	75			•			•			•		•	•	•	•	•	•	•	•	•	•	•
P857M	75			•			•				•	•	•	•	•	•	•	•	•	•	•	•
P860M	73			•			•			•		•	•	•	•	•	•	•	•	•	•	•
P880	71			•			•				•	•	•		•	•	•	•	•	•	•	•
P/9200	69						•				•	•	•	•	•	•	•	•	•			•
PRIME Computer																						
PRIME 100	72			•			•			•		•	•	•	•	•				•	•	
PRIME 200	72			•			•			•		•	•	•	•	•				•	•	
PRIME 300	73			•			•				•	•	•	•	•	•				•	•	
Pro-Log																						
PLS-401	73		•						•												•	
PLS-441	75		•						•						•						•	

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		Process Control	Microcomputers	Minicomputers	8	12	16/18	24/32	32K	32-64K	64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
Pro-Log (Contd.)																						
MPS-803	74		●		●				●						●						●	
MPS-883	75		●		●				●						●						●	
R2E MICRAL	73		●	●	●					●		●	●	●	●			●				
RCA Cosmac Microkit			●		●				●												●	
Raytheon RDS-500	73						●			●		●	●	●	●	●					●	
Regnecentralen																						
RC 7001	71						●				●	●	●	●	●	●						●
RC 7002	72						●				●	●	●	●	●	●						●
RC 7003	72						●				●	●	●	●	●	●						●
RC 7004	71						●				●	●	●	●	●	●						●
RC 7004SC	71						●				●	●	●	●	●	●						●
Ricoh RICOM-8	71							●	●			●				●						●
Rockwell																						
PPS-4	73		●						●			●		●	●						●	
PPS-8	75		●		●				●			●		●	●						●	
Scientific Micro Systems																						
SMS-300	75		●		●				●												●	
SMS-3000 (MCSIM)	75		●		●				●			●									●	
Selenia																						
GP-16	70						●			●				●		●			●			
GP-160	73			●			●			●		●	●	●	●	●			●			
Siemens																						
101	68						●				●						●	●	●	●		●
301	69			●				●		●				●	●		●	●	●	●	●	●
302	67			●				●		●				●	●		●	●	●	●	●	●
303	65			●				●			●			●	●		●	●	●	●	●	●
304	67			●				●			●	●	●	●	●		●	●	●	●	●	●
305	67			●				●			●	●	●	●	●	●	●	●	●	●	●	●
306	70			●				●			●	●	●	●	●	●	●	●	●	●	●	●
320	72			●			●				●	●	●	●	●	●	●	●	●	●	●	●
404/3	70			●			●				●	●	●		●		●	●	●			●
404/6	70			●			●				●	●	●	●	●		●	●	●			●
PR 330	73			●			●				●	●	●		●	●	●	●	●	●		●
Signetics N 3001	75		●						●												●	
N 3002	75		●						●												●	
2650 PC 1001	75		●		●				●												●	
Spiras Systems	69		●				●				●	●	●	●		●					●	
SPIRAS-65	69			●			●				●	●	●	●		●					●	
SYSTEMS Engineering																						
SEL 32	75						●			●		●	●	●	●	●	●		●	●		
Takachiho																						
TK-70	70						●		●			●	●	●		●						●
TK-7100	71						●		●			●	●	●		●						●
Teac TEAC-16	70						●		●				●	●	●	●						●
Telefunken TR 86	68							●			●	●	●	●	●	●	●					●
Telemecanique																						
T621	73				●				●			●	●	●	●	●		●	●			
T1000	71			●			●			●		●	●		●	●	●	●	●	●		●

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Telemecanique (Contd.)																						
T1600	72			●			●			●		●	●	●	●	●	(2)	●	●	●		●
T2000	69			●			●				●	●	●		●	●	●	●	●	●		●
T2000/10	72			●			●			●		●	●		●	●	●	●	●	●		●
T2000/20	72			●			●				●	●	●		●	●	●	●	●	●		●
Solar 16-05	75			●			●			●							●	●	●	●		●
Solar 16-40	75			●			●				●						●	●	●	●		●
Solar 16-65	75			●			●				●						●	●	●	●		●
Texas Instruments																						
Intel 8080	75		●		●				●												●	
TI 960A	71			●			●				●	●	●	●	●	●	●	●	●	●	●	
TI 960B	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
TI 980A	72			●			●				●	●	●	●	●	●	●	●	●	●	●	
TI 980B	74			●			●				●	●	●	●	●	●	●	●	●	●	●	●
TI 990/4	75		●				●				●						●	●	●	●	●	●
TI 990/10	75			●			●			●	●	●	●	●	●	●	●	●	●	●	●	●
TMS 1000	74		●						●												●	
TMS 1100	74		●		●				●												●	
TMS 9900	75		●				●										●	●	●	●	●	●
Three Phoenix PTT 8000	74		●		●				●												●	
Toshiba																						
TOSBAC 40A	70						●				●	●	●	●		●						●
TOSBAC 40B	71						●					●	●	●		●						●
TOSBAC 10	71					●			●			●	●	●		●						●
TOSBAC 10E	71					●						●	●	●		●						●
TOSBAC 40N								●			●	●	●	●	●	●						●
Toshiba America TLCS-12 EX-2	74		●			●			●				●		●						●	
TLC-12A EX-IA	75		●			●			●				●								●	
Transitron Electronics																						
TDS/16	75		●				●			●		●			●						●	
TMC 1601	75		●				●			●		●			●						●	
Varian Data																						
520/i	68			●	●					●		●	●	●	●		●	●	●	●	●	●
620/f	70			●	●		●			●		●	●	●	●	●	●	●	●	●	●	●
620/f-100	72			●			●			●		●	●	●	●	●	●	●	●	●	●	●
620/i	67						●			●		●	●	●	●	●	●	●	●	●	●	●
620/L	71			●			●			●		●	●	●	●	●	●	●	●	●	●	●
620/L-100	72			●			●			●		●	●	●	●	●	●	●	●	●	●	●
622/i	68						●			●		●	●	●	●	●	●	●	●	●	●	●
V71	74			●			●			●		●	●	●	●	●	●	●	●	●	●	●
V72				●			●			●		●	●	●	●	●	●	●	●	●	●	●
V73	73			●			●			●		●	●	●	●	●	●	●	●	●	●	●
V74	73			●			●				●	●	●	●	●	●	●	●	●	●	●	●
V75	75			●			●				●	●	●	●	●	●	●	●	●	●	●	●
Warner and Swasey Comstar System 4	72		●						●			●	●	●							●	
Comstar System 4A, 4B	75		●						●			●	●	●							●	
Comstar System 8A	75		●		●					●		●	●	●	●	●					●	
Comstar System 8D	75		●		●					●		●		●	●	●					●	
Western Digital MCP 1600	75		●		●				●			●		●	●						●	

MANUFACTURER AND MODEL NUMBER	First Delivery	COVERAGE: Process Control	COVERAGE: Microcomputers	COVERAGE: Minicomputers	WORD LENGTH (Bits): 8	WORD LENGTH (Bits): 12	WORD LENGTH (Bits): 16/18	WORD LENGTH (Bits): 24/32	MAX MEM (Bytes): 32K	MAX MEM (Bytes): 32-64K	MAX MEM (Bytes): 64K	PERIPHERALS: Disc/Drum	PERIPHERALS: Mag Tape	PERIPHERALS: Data Comm	SOFTWARE: Oper Sys	SOFTWARE: Fortran/Algol	MAJOR MARKETS: Germany	MAJOR MARKETS: France	MAJOR MARKETS: Italy	MAJOR MARKETS: U.K.	MAJOR MARKETS: U.S.A.	MAJOR MARKETS: Other
Westinghouse																						
2500	71	●					●				●	●	●	●	●	●					●	
2550	72	●					●				●	●	●	●	●	●					●	
P2000	69	●					●				●	●		●	●	●	●	●	●	●	●	●
Wintek W 6800	75		●		●				●			●	●	●		●					●	
Xerox																						
Sigma 3	70			●			●				●	●	●	●	●	●	●	●		●	●	●
530	73			●			●				●	●	●	●	●	●	●	●		●	●	●
Yasukawa-Denki																						
MEMOCON-16	70						●		●			●		●		●						●
Zuse Z43	69						●					●	●	●	●	●	●					●

Notes:

(1) Dietz Mincal 621 is marketed in France and Italy under the label Telemecanique T621.
(2) Telemecanique T1600 is marketed in West Germany, Netherlands, Scandinavia, and Eastern Europe under the label Dietz Mincal 1600.

SPECIFICATION CHART

Microprocessors—Microcomputers

MANUFACTURER	American Microsystems Inc.	Applied Computing Technology	Applied Computing Technology	Applied Data Communications	Applied Systems Corp.
Model Number	AMI 6800	UMPS-4	PPS-4MP	70-100	ASC/8
PHYSICAL PACKAGE					
Number of boards	–	2	7	1	3 minimum
Dimensions	–	5 x 7"	5 x 7"	16 x 15"	Depend on opts
Number of chips	1	4	Variable	–	1
Number of pins/chip	40	42	42	–	40
Power Supply (std, opt)	+5V opt	Opt	Std	Opt	Std/opt
Console (std, opt)	No	Opt	Std	Opt	Opt
Cabinet (std, opt)	No	Std	Std	Opt	Rugged opt
PROCESSOR					
Manufacturer	Motorola	Rockwell	Rockwell	Intel	Intel
Model Number	6800	PPS-4	PPS-4	8080	8080
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	pMOS	nMOS	nMOS
Word size					
Data, bits	8	4	4	8	8
Instruction, bits	8, 16	8	8	8/16/24	8/16/24
Clock frequency, KHz	100	200	200	2000	2000
Add Time, reg to reg, μsec	2	4.0 (4-bit wd)	4.0 (4-bit wd)	2	2
Number of instructions	72	50	50	74	74
Number of registers	6 internal	2 (12-bit)	2 (12-bit)	–	–
μprogrammed	No	Yes	Yes	No	No
Fixed-point Arithmetic (+, –, X, ÷) Implementation (binary, BCD); (std, opt)	Yes	Binary, BCD	Binary; BCD	Std	Std
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	nMOS	pMOS	pMOS	NA	nMOS
Word size, bits	8	8	8		8
Capacity, words	1K	16K	16K		32K
Cycle time, μsec	0.575	1.25	1.25		
RAM (std, opt)					Opt
Technology	nMOS	pMOS	pMOS	nMOS	
Word size, bits	8	4	4	8	8
Capacity, words	128	4K	4K	16K CPU; 64K system	64K
Cycle Time, μsec	1.0	1.25	1.25	–	–
PROM					
Technology	–	pMOS	pMOS	–	nMOS
How programmed?	–	UV erasable	UV erasable	UV reprogrammable	Elect.
Word size, bits	–	8	8	8	8
Capacity, words	–	16K	16K	4K CPU; 64K system	64K
Cycle time, μsec	–	1.0	1.0	–	–
INPUT/OUTPUT					
I/O word size, bits	8	Three 4-bit groups	Three 4-bit groups	8/32	8/32
Number of device addresses	10 max	16	16	To 2K	To 2048
Programmed I/O	No	Yes	Yes	Yes	Yes
Direct Memory Access	Yes	Yes	Yes	Opt	Opt
Type of interrupt system	Vectored	NA	NA	Vectored	Vectored
I/O rate, wds/sec	–	4K	4K	500K	500K
Device interfaces available (List)	General purpose communications interface; peripheral interface adapter; async communications interface adapter modem; universal sync receiver xmitter	Keyboard; display; printer; teletype; RS-232; paper tape reader; Silent 700	Keyboard display; printer; teletype RS-232; paper tape reader; Silent 700	IBM compatible floppy disc; 3M tape cartridge; 9-track tape; GP I/O card; ROM programmer; memory expansion; real-time clock; RS-232 and current loop; sync or async communications controller	T2L; EIA Communications; teletype; printer; graphic; CRT; disc; keyboard; A/D
SOFTWARE					
Assembler	Yes	Yes	Yes	–	Yes
Cross assembly (what system?)	Yes	FORTRAN IV	FORTRAN IV	–	FORTRAN; (IBM 370)
Simulators (For what)	360/370 IBM	Time share	Time share	–	Yes
Languages	FORTRAN IV	No	No	–	Basic; PL/M
Operating System	No	No	Yes	ADC micro Exec*	Yes
Software (bundled?)	No	Yes	Yes	–	Opt
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes		Opt
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?		Prototypes small production systems	Stand-alone development system for Rockwell PPS-4 microcomputer set	Stand-alone small business system; word processing; communication system	Communications controller for IBM bi-sync protocol to multiple async terminals
First Delivery	12/74	12/73	4/73	4/75	1974
Number delivered	–	60	70	–	–
STANDARD SYSTEM		1K wds ROM; 1K wds RAM	1K wds ROM; 1K wds RAM	CCPC board with RS232/ TTY controller; 1K bytes ROM; 4K RAM	1K wds ROM/1K wds RAM
PRICE, $	Single quantities/69	855/695	2495; 2495	1300	1,000
Other Features			Prom programmer; high speed tape reader; RS-232 interface as options	*also ADC Micro DOS, floppy disc in same enclosure opt expandable to 8	Optional communications terminal control features for ASCII/EBCDIC conversion; buffering and multiplexing

SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Cramer Electronics	Control Logic	Control Logic	Data Architects	Data Numerics
Model Number	CRAMERKIT 1	L Series	M Series	CM101	DL8A
PHYSICAL PACKAGE					
Number of boards	–	3 minimum	3 minimum	1	1
Dimensions	–	3" x 4.5"	3" x 4.5"	13.1 x 6.1 x 2	16" x 8"
Number of chips	25	25	23	92	90
Number of pins/chip	Various	Variable	Variable	–	Varies
Power Supply (std, opt)	Opt	Opt	Opt	Opt	Opt
Console (std, opt)	Std	Opt	Opt	Opt	Opt
Cabinet (std, opt)	Opt	Opt	Opt	Opt	Opt
PROCESSOR					
Manufacturer	Intel/T.I./Motorola/AMD	Intel	Intel	Intel	Intel
Model Number	8080A/8080/6800/9080	8008-1	8080	4004-4040	8080
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	nMOS	pMOS	
Word size					
Data, bits	8	8	8	4	8
Instruction, bits	8	8/16/24	8/16/24	8/16	8
Clock frequency, KHz	–	250	2000	636	–
Add Time, reg to reg, μsec	–	12.5	2.0 +	12.6	–
Number of instructions	–	48	78	45	–
Number of registers	–	7	8	17	–
μprogrammed	–	No	No	No	–
Fixed-point Arithmetic (+, -, X, ÷)					
Implementation (binary, BCD); (std, opt)	–	Binary std	BCD & Binary; std	BCD & Binary std	
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	–	NA	NA	Any std	All
Word size, bits	–		–	8	8
Capacity, words	–		–	4K banks	64K
Cycle time, μsec	–		–	1.1	Various
RAM (std, opt)	Std	Opt	Opt	Any std	All
Technology	nMOS	pMOS	pMOS		
Word size, bits	8	8	8	4	8
Capacity, words	1024	1K/board	1K/board	4K banks	64K
Cycle Time, μsec	0.45	1.5	1.5	1.1	Various
PROM		Opt	Opt	Std	All
Technology	FAMOS(1)	pMOS	pMOS	FAMOS(1)	
How programmed?	Pgmr avail as kit	UV Erasable; FAMOS	UV Erasable; FAMOS	Electrically	Electrically
Word size, bits	8	8	8	8	8
Capacity, words	1024	512/board	512/board	256 or 512	8
Cycle time, μsec	0.45	1.0	1.0	1.0	Various
INPUT/OUTPUT					
I/O word size, bits	8	8	8	4	8
Number of device addresses	8	32	256 in/256 out	32	Various
Programmed I/O	Yes	Yes	Yes;	Yes; std	Yes
Direct Memory Access	Yes	Opt	Opt	No	Yes
Type of interrupt system	1 interrupt	Vectored; 8 levels	Vectored; 8 levels	No; uses polling	8-level
I/O rate, wds/sec	–	13K	43K	20K	To 1M Hertz
Device interfaces available–(List)	RS-232; TTY; audio cassette	TTY; EIA RS 232C; general serial; general parallel; high speed paper tape reader and punch; CRT; floppy disc; PROM programmer	TTY; EIA RS-232C; general serial; general parallel; high speed paper tape reader; high speed punch; CRT; floppy disc; PROM programmer	TTY; 4-bit parallel; 8-bit parallel; time of day; gp serial interfaces all on same board as processor	Mag tape; cassette; cartridge; TTY; CRT; paper tape; keyboard
SOFTWARE					
Assembler	Avail 1st qtr 1976	Yes	Yes	Yes	Yes
Cross assembly (what system?)	–	PDP-8	PDP-8	Tymshare	PDP-8/PDP-11
Simulators (For what)	–	N/A	N/A	Tymshare	–
Languages	–	L Series Assembly	M Series Assembly	Assembler	–
Operating System	Yes	ODT	ODT	Custom	–
Software (bundled?)	Yes	Bundled or separate	Bundled or separate	No	–
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	–	Yes	Yes	Yes	No
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	Yes	Simulation	Simulation	Communications controller	
First Delivery	9/75	4/73	9/74	–	1975
Number delivered	–	2,250 L and M	2,250 L and M	–	25 +
STANDARD SYSTEM	With 1K wds ROM and 1K RAM	With 1K wds ROM/with 1K wds RAM	With 1K wds ROM/ with 1K wds RAM	With 1K words ROM	1K ROM/1K RAM
PRICE, $	495	569/460	729/620	1,740	950/850
Other Features	(1) Floating gate Avalanche MOS	LDS series development series contains processor; 4K bytes RAM; Monitor/ debugger loader; parallel I/O interfacing; TTY interface; console; powered enclosure; assembler; editor; PROM programmer for 2,340	MDS-M Series development system includes processor; 5K RAM; Monitor/debugger/loader; parallel I/O interface; TTY interface; console; powered enclosure; assembler; editor; PROM programmer costs $2,340	(1) Floating gate Avalanche MOS	

MANUFACTURER	Digital Equipment	Digital Equipment	Digital Laboratories	Fabritek	Fairchild Semiconductor
Model Number	LSI-11	MPS System	PB 96	MP12	F8S-simboard
PHYSICAL PACKAGE					
Number of boards	1	1	1	2	1
Dimensions	10.5 x 8.5"	8.5 x 10 x 0.5	9 x 15"	16.3 x 9.5"	12 x 6"
Number of chips	55	50	72	130	–
Number of pins/chip	16	18	14/16	14/16	5/12
Power Supply (std, opt)	Opt	Std	Opt	Opt (+5VDC)	Std
Console (std, opt)	Opt	Std	Opt	Std	–
Cabinet (std, opt)	Opt	Std	Opt	Opt	–
PROCESSOR					
Manufacturer	Digital Equipment	Intel	Digital Labs	Fabritek	Fairchild
Model Number	LSI-11	8008	PB96P	MP-12	3850
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	TTL	Bipolar	nMOS
Word size					
Data, bits	16	8	8	12	8
Instruction, bits	16	8	8/16	12	8
Clock frequency, KHz	833	500K	9600	12,000	2000
Add Time, reg to reg, μsec	3.5	20.0	5.9	3.0	5
Number of instructions	Over 400	48	18	28	60
Number of registers	8	–	12	Single accumulator	67
μprogrammed	Yes	Yes	No	No	Yes
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Opt	–	Opt	Binary	–
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	nMOS	–	MOS/pROM	Bipolar	MOS
Word size, bits	16	–	8	12	8
Capacity, words	28K	–	1K	2K	1K
Cycle time, μsec	0.5	–	1.2	1.5	5
RAM (std, opt)					
Technology	nMOS and Core	nMOS opt	Opt	Core	MOS
Word size, bits	16	8	8	12	8
Capacity, words	28K	4K/board	64K	4K	2K
Cycle Time, μsec	0.5; 1.2	1.1	5.6	1.5	5
PROM					
Technology	MOS	Opt	1702A	Bipolar	Bipolar
How programmed?	Fusible link			FL	Fused link
Word size, bits	16	8	8	12	8
Capacity, words	28K	4K/board	1024	2K	2K
Cycle time, μsec	0.7	1.0	1.2	1.5 μsec	5
INPUT/OUTPUT					
I/O word size, bits	16	8	8	12	8
Number of device addresses	4K	–	12	63	4
Programmed I/O	Yes	–	Yes	Yes	–
Direct Memory Access	Yes	No	Opt	Single channel	–
Type of interrupt system	Single-line; vectored	–	Opt	Single channel	Vectored
I/O rate, wds/sec	833K wds/sec	–	2.9 μsec/byte	PIO 66KHX/DMA 666KHz	–
Device interfaces available–(List)	For serial devices	Full duplex serial interface	RS232C; TTY; punch tape; card reader; floppy disc; keyboard; Burroughs self-scan	Async communication; high speed paper tape; RDR/PCH; TTY; cassette tape; line printer; char printer; digital input/ output; D to A; IBM compatible mag tape; extension data store	
SOFTWARE					
Assembler	Yes	PDP-8	Yes, pass	Yes	Yes
Cross assembly (what system?)		PDP-8	PDP-8 pass	IBM 360/370	FORTRAN
Simulators (For what)		–	PDP-8	NA	F8
Languages	BASIC; FORTRAN; FOCAL	–	None	PDP-8 compatible	–
Operating System	RT-11	–	Editor	Real-time exec	–
Software (bundled?)	Unbundled	–	Yes	Yes	Debug
APPLICATIONS					
Replace Hard-wired logic	–	–	Yes	Yes	Yes
Commercial processing	–	–	Yes	No	Yes
Data acquisition	–	–	Yes	Yes	Yes
Terminals	–	Yes	Yes	Yes	Yes
Device controllers	–	Yes	Yes	Yes	Yes
Process control	–	Yes	Yes	Yes	Yes
Any others?	General purpose mini-computer		Word processing; large buffer/controller; communications buffer; programmable calculator interface		
First Delivery	4/75	1974	3/74	–	6/75
Number delivered	–		–	–	15
STANDARD SYSTEM	4K words RAM	–	With 1K wds ROM/ With 1K wds RAM	With 4K words RAM; power supply; chassis and 12-bit microcomputer	NA
PRICE, $	990	–	295/275	2395	
Other Features			Architecture oriented towards use of large serial working memory (CCDS or other shift registers). Made of TTL IC's readily available. Licensing arranged for most users if desired.		

SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Fairchild Semiconductor	General Automation	General Automation	General Automation	General Instrument
Model Number	F8-C	GA-16/110	GA-16/220	GA-8/55	GIC 1600
PHYSICAL PACKAGE					
Number of boards	7	1	2	1	4
Dimensions	6 x 8"	7-3/4 x 11"	7-3/4 x 11"	7-3/4 x 11"	9.75" x 9.25
Number of chips	–	2	2	1	202
Number of pins/chip	5/12	48	48	40	14-40
Power Supply (std, opt)	Std	Opt (plug in)	Opt (plug-in)	Opt (plug in)	Opt
Console (std, opt)	Std	Std	Std	Std	Std
Cabinet (std, opt)	Std	Opt	Opt	Opt	Std
PROCESSOR					
Manufacturer	Fairchild	GA	GA	Intel	General Instrument
Model Number	3850	–	–	8080	CP1600
Technology Used (n/pMOS, bipolar)	nMOS	nMOS	nMOS	nMOS	nMOS
Word size					
Data, bits	8	16	16	8	16
Instruction, bits	8	16	16	8	10
Clock frequency, KHz	2000	12.6	–	2000	5000
Add Time, reg to reg, μsec	5	2.0	2.0	2.0	2.4
Number of instructions	60	91 std; 120 opt	91 std; 120 opt	89	87
Number of registers	67	16	16	7	8
μprogrammed	Yes	Yes	Yes	Yes	No
Fixed-point Arithmetic (+, –, X, ÷) Implementation (binary, BCD); (std, opt)		Binary std	Binary std	Binary and decimal conversion std	Std
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	MOS	Bipolar	Bipolar	Bipolar	nMOS
Word size, bits	8	16	16	8	10-16
Capacity, words	1K	64K	64K	58K bytes	32K/card
Cycle time, μsec	5	0.5	0.5	0.5	0.5
RAM (std, opt)					
Technology	MOS	nMOS	nMOS	nMOS	nMOS
Word size, bits	8	16-18 opt	16-18 opt	8	16
Capacity, words	4K	64K	64K	56K bytes	8K/card
Cycle Time, μsec	5	0.5	0.5	0.5	0.5
PROM					
Technology	Bipolar	Bipolar	Bipolar	Bipolar	pMOS; Silicon gate
How programmed?	Fused link	Fusible link	Fusible link	Fusible link	electrically; UV
Word size, bits	8	16	16	8	16
Capacity, words	4K	64K	64K	56K	4K wds/card
Cycle time, μsec	5	0.5	0.5	0.5	1.5
INPUT/OUTPUT					
I/O word size, bits	8	16	16	16	16
Number of device addresses	4 per board	64	64	64	65K
Programmed I/O		Std	Std	Std	Yes
Direct Memory Access	Option	Std	Yes	Yes	Yes
Type of interrupt system	Vector	Vectored priority	3-level vectored	Vectored priority	Multilevel vectored
I/O rate, wds/sec		PIO 200K; DMA 2M	PIO 200K; DMA 2M	PIO 100K; DMA 2M	–
Device interfaces available (List)		DIO; AC in; AC out; Analog out; threshhold in; async comm; sync; bisync; SDLC; TTY; CRT; paper tape reader/punch; plotter; line printer; cassette; cartridge; floppy disc; magtape; disc	TTY; CRT; paper tape; card reader/punch; plotter line printer; cassette; cartridge; floppy; magtape; disc	Digital In/Out; AC in/out analog in/out; threshold in; async comm; async mux; sync comm; bisync; SDLC; TTY; CRT; paper tape reader; plotter	TTY; EECO; REMEX or Tally high speed reader/ punch; EIA interface devices
SOFTWARE					
Assembler	Yes	–	Yes	No	Yes
Cross assembly (what system?)	FORTRAN	SPC-16 & GA 16/330	SPC-16 & GA-16/330	360/370	FORTRAN IV, F level;
Simulators (For what)	F8	SPC-16/GA-16/330	SPC-16 & GA-16/330	360/370	GIC 1600 or host
Languages	–	FORTRAN, COBOL, BASIC	FORTRAN; COBOL; BASIC	PL/M 360/370	Assembly
Operating System	Yes	RTX	RTX; FSOS1DBOS; RTOS	No	Resident monitor
Software (bundled?)	Yes	No	No	No	On-line bundled
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?		Communications buffer	Communication buffer	Communications machine control	Telecommunications
First Delivery	9/75	–	–	5/75	–
Number delivered	5	–	–	–	–
STANDARD SYSTEM	N/A				CPU, 8K memory, console, ODP firmware, I/O and software
PRICE, $		–	–	–	3400
Other Features		Compatible with SPC-16 software and I/O; PF/AR; RTC port; integral displays; operations monitor; remote load; single PC board; parity opt; memory protect opt; cold start ROM	PF/AR; 1ms RTC; integral display; microconsole ROM; operations monitor; remote load; 2-board configuration; parity (opt); memory protect (opt); cold-start ROM	PF/AR; 1usec RTC; cold start ROM; integral operator display; TTY/ CRT; remote load; operations monitor alarm; microconsole opt complete micro on single board	

MANUFACTURER	General Instrument	GTE Information Systems	GTE Information Systems	Hollinbeck Enterprises	Hollinbeck Enterprises
Model Number	GIC 1601	IS/1011	IS/1014	MP-68	MP-11
PHYSICAL PACKAGE					
Number of boards	4	1 or more	1 or more	3	3
Dimensions	9.75" x 9.25"	12.5" x 20"	12.5" x 20"	8" x 14"	8.5" x 10"
Number of chips	209	80 +	80	–	–
Number of pins/chip	14 to 40	–	–	–	–
Power Supply (std, opt)	Opt	Opt +5V, +12V, -12V	Std	Std	Std
Console (std, opt)	Std	Opt	Opt	Std	Std
Cabinet (std, opt)	Std	Opt	Opt	Std	Std
PROCESSOR					
Manufacturer	General Instrument	GTE	GTE	AMI	DEC
Model Number	CP 1600	IS/1011	IS/1014	6800	LSI-11
Technology Used (n/pMOS, bipolar)	nMOS	Bipolar	Bipolar	nMOS	nMOS
Word size					
Data, bits	16	8	8 or 16	8	16
Instruction, bits	10	16	8, 16	8	16
Clock frequency, KHz	5000		.06	1000	1000
Add Time, reg to reg, μsec	2.4	0.2	.2 (GP Reg to accum)	2	2
Number of instructions	87	40	80	72	400
Number of registers	8	17	16	5	8
μprogrammed	No	Yes	Yes	Yes	Yes
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Std	Binary std	Binary Std	Std	Binary, std
MEMORY					
Types – (ROM/RAM/PROM)					
ROM		Opt	Opt		
Technology (n/pMOS, bipolar)	nMOS	Bipolar	Bipolar	nMOS	nMOS
Word size, bits	10-16	16	8 16	8	8
Capacity, words	32K/card	65K (off board)	16K	61K	61K
Cycle time, μsec	0.5	0.15	1	1	1
RAM (std, opt)		Opt	Std		
Technology	nMOS	Bipolar/core	Core (off board)	nMOS	nMOS
Word size, bits	16	16	8	8	16
Capacity, words	8K/card	1K	16K	61K	28K
Cycle Time, μsec	0.5	0.15	0.75	0.8	0.8
PROM		Opt	Opt		
Technology	pMOS; silicon gate	Bipolar	Bipolar	nMOS	nMOS
How programmed?	Electrically and UV	Fusible link	Fusible link	Elec	Elec
Word size, bits	16	16	8 or 16	8	16
Capacity, words	4K wds/card	65K	4K on board	61K	28K
Cycle time, μsec	1.5	0.15	0.1	0.1	1
INPUT/OUTPUT					
I/O word size, bits	16	8	8	8	16
Number of device addresses	65K	256	256	4096	4096
Programmed I/O	Yes	–	Yes	Std	Std
Direct Memory Access	Yes	–	Yes	Std	Std
Type of interrupt system	Multi-level vectored	–	–	Vector	Vector
I/O rate, wds/sec	–	–	–	45K bytes/sec	90K wds/sec
Device interfaces available - (List)	TTY; EECO; REMEX or Tally high speed reader/ punch; EIA interface devices	Buffer memory; interval timer, cyclic redundancy check/generate; code conversion memory	Cash register; modem controllers; debug hardware	Floppy disc RS-232; modem	Floppy disc; RS232; modem
SOFTWARE					
Assembler	Yes	No	No	Resident	Resident
Cross assembly (what system?)	F-level FORTRAN IV	GTE IS 1000	GTE/IS 1000	No	No
Simulators (For what)	GIC 1600 or host	No	No	No	No
Languages	Assembly	No	No	BASIC	BASIC, FORTRAN IV, COBOL
Operating System	Resident monitor	No	No	DOS	RT-11
Software (bundled?)	On-line bundled	No	No	No	No
APPLICATIONS					
Replace Hard-wired logic	Yes	–	–	No	No
Commercial processing	Yes	–	Yes	Yes	Yes
Data acquisition	Yes	–	–	Yes	Yes
Terminals	Yes	Yes	No	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	–	Yes	Yes	Yes
Any others?	Telecommunications	–			Yes
		For hardware debug; memory units;communications interfaces			Floppy disc; RS-232; modem
First Delivery	7/75	1/75	11/74	8/75	12/75
Number delivered	25	–	–	–	NA
STANDARD SYSTEM	CPU, 8K memory, console, ODP firmware, I/O and software			With 1K words of ROM	1K words ROM
PRICE, $	3500			7500	9,000
Other Features				Includes 16KB RAM; dual floppy disc; assembler; loader, text editor and operating system; OEM discounts available	Includes 16KB RAM; dual floppy disc; assembler; loader; text editor; and operation system; OEM discounts available

SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Intel	Intel	Intel	Intel	Intel
Model Number	4004 (MCS-4)	4040 (MCS40) (Intellec 4)	8008	8080	MDS-800 (8080A)
PHYSICAL PACKAGE					
Number of boards	1	–	–	–	4 std; 14 more opt
Dimensions	6.18 x 8 x .06"	–	–	–	–
Number of chips	7	1	1	1	–
Number of pins/chip	16/24	24	40	40	16/24/40
Power Supply (std, opt)	Opt	Opt	Opt	Opt	Std
Console (std, opt)	Opt	Opt	No	No	TTY; CRT opt
Cabinet (std, opt)	Opt	Opt	No	No	Std
PROCESSOR					
Manufacturer	Intel	Intel	Intel	Intel	Intel
Model Number	4004	4004	8008	8080	8080A
Technology Used (n/pMOS, bipolar)	pMOS	pMOS	pMOS	nMOS	nMOS
Word size					
Data, bits	4	4	8	8	8
Instruction, bits	8, 16	8, 16	8, 16, 24	8, 16, 24	Multiple of 8
Clock frequency, KHz	740	740K	500 to 800	2080 to 3000	2000
Add Time, reg to reg, μsec	10.8	10.8	20/12.5	2-1.33	–
Number of instructions	46	60	48	78	72
Number of registers	16	24	7 8-bit data regs	7 8-bit data regs	6 16-bit
μprogrammed	No	No	No	No	No
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Binary, BCD Std	Binary; Logical BCD Std	Binary	Binary, BCD	Binary; BCD Std
MEMORY					
Types – (ROM/RAM/PROM)					
ROM	Std	Std			
Technology (n/pMOS, bipolar)	pMOS	pMOS	pMOS, nMOS, Bipolar	pMOS, nMOS, bipolar	All
Word size, bits	4	8	8	8	8
Capacity, words	1K	256	250-2K	250-2K	2K or 14K
Cycle time, μsec	–		0.5-1.5	0.5-1.5	0.07
RAM (std, opt)	Std	Std			Std
Technology	pMOS	–	pMOS, nMOS, CMOS	pMOS, nMOS, CMOS	nMOS
Word size, bits	4-bits	-	1, 4	1, 4	8
Capacity, words	320	–	256-4K	256-4K	16K
Cycle Time, μsec	–	–	1.5	1.5	1
PROM	Opt	Std			
Technology	–	–	pMOS, nMOS, bipolar	pMOS, nMOS, bipolar	nMOS, bipolar
How programmed?	–	–	Fusible link, FAMOS	Fusible link, FAMOS(1)	PROM programmer
Word size, bits	–	–	8; 4	8; 4	4/8
Capacity, words	1K	–	2-8K	2K-8K	12K
Cycle time, μsec	–	–	0.5-1.5	0.5-1.5	0.07
INPUT/OUTPUT					
I/O word size, bits	4-bits	–	8	8	8; 16 DMA
Number of device addresses	–	–	256	256	256 expandable
Programmed I/O	–	–	–	–	Yes
Direct Memory Access	No	–	–	–	Yes
Type of interrupt system	None	–	Vectored 8-level	Vectored 8-level	8-user mask
I/O rate, wds/sec	–	–	–	–	–
Device interfaces available – (List)	Clock; memory; I/O	Clock, RAM; I/O			RS232 (CRT); TTY; High speed reader; Line printer
SOFTWARE					
Assembler	–	Resident	Resident	Resident	Yes
Cross assembly (what system?)	Yes	Yes	FORTRAN IV	FORTRAN IV	Yes FORTRAN IV
Simulators (For what)	Yes	Yes	FORTRAN IV	FORTRAN IV	Yes FORTRAN IV
Languages	FORTRAN IV	FORTRAN IV	PL/M	PL/M	PL/M
Operating System	–	–	Yes	–	Yes
Software (bundled?)	No	No	Yes	No	Yes
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?			Billing, accounting	Avionics	Prototype, development systems support is prime target
First Delivery	-	-	1971	1973	6/75
Number delivered	–	–	1M	–	300 +
STANDARD SYSTEM					With 2K wds ROM, 16K wds RAM, text editor, assembler monitor
PRICE, $	National Semiconductor second source	-	–	–	3950
			–	–	ICE (In Circuit Emulator) processor boards & cable with plug to prototype
Other Features					Dip socket, including all software support for user defined break point settling & debugging

MANUFACTURER	Keronix	Martin Research	Martin Research	Micro Computer Machines	MICROKIT
Model Number	IDS 16M	AT 804-3	AT 811-3	MCM/70	8/16
PHYSICAL PACKAGE					
Number of boards	1	4	4	5	4
Dimensions	7 x 10"	5.5 x 7"	5.5 x 7"	–	6 x 8"
Number of chips	50	–	–	–	29
Number of pins/chip	–	16, 18, 20, 24	16, 20, 24, 40	–	40 max
Power Supply (std, opt)	Opt	Opt	Opt	Std	Std
Console (std, opt)	Opt	Std	Std	Std	Std
Cabinet (std, opt)	Opt	Opt	Opt	Std	Std
PROCESSOR					
Manufacturer	Keronix	Intel	Intel/AMD/TI	Intel	Intel/AMD/TI
Model Number	IDS 16M	8008; 8008-1	8080; 8080A	–	8080
Technology Used (n/pMOS, bipolar)	Bipolar	pMOS	nMOS	–	nMOS
Word size					
Data, bits	16	8	8	–	8
Instruction, bits	16	8, 16, 24	8, 16, 24	–	8, 16, 24
Clock frequency, KHz	100	500; 800	2000; 3200	–	200
Add Time, reg to reg, μsec	1.5	2.0; 12.5	2; 1.25	–	2
Number of instructions	192	48	Std	–	78
Number of registers	4	17	8	–	7
μprogrammed	No	No	No		No
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Std binary	No	No	–	Binary; BCD std
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	MOS	–	–	MOS	–
Word size, bits	16	–	–	8	–
Capacity, words	2K	–	–	32K	–
Cycle time, μsec	0.5	–	–		–
RAM (std, opt)		Std			
Technology	MOS	nMOS	nMOS	MOS	nMOS
Word size, bits	16	8	8	8	8
Capacity, words	32K	16K	64K	2K, 4K or 8K	56K
Cycle Time, μsec	0.8	0.45	0.45		0.48 rd; 0.96 write
PROM					
Technology	MOS	pMOS	pMOS	–	EAROM UV erasable
How programmed?	–	Electric (1702A)	Electric (1702A)	–	Electric
Word size, bits	16	8	8	–	8
Capacity, words	2K	2K +	2K +	–	8K
Cycle time, μsec	0.5	1.0	1.0	–	0.45
INPUT/OUTPUT					
I/O word size, bits	16	8	8	8	8
Number of device addresses	62	32	548	199	512
Programmed I/O	Yes	Opt	Opt	Yes	Yes
Direct Memory Access	Yes	No	Opt	–	Yes
Type of interrupt system	Priority	Single level	8-level vectored	–	Vectored; priority
I/O rate, wds/sec	500K one-line	31K one-line	12K (PIO); 2M (DMA)	120	50K
Device interfaces available - (List)	TTY; real-time clock; paper tape reader and punch	TTY; 5-level TTY (Baudot); floppy disc; cassette tape; TV text (planned); PROM programming; multiprocessor (planned); ASCII keyboard (planned); Okidata 110-cps printer	TTY; 5-level TTY (baudot); floppy disc; cassette tape; TV text (planned); PROM programming (planned) multiprocessor interface planned; Okidata 110 cps printer (avail); CRT monitor (planned)	Printer/plotter; communications subsystem; EIA RS 232C; current loop; APL/ASCII; ASCII; IBM correspondence; any user-defined 5, 6, 7 or 8-level code	Keyboard; CRT display; cassette tape; RS-232C; real-time clock; 110 cps line printer; 8 bit interprocessor port
SOFTWARE					
Assembler	Yes	Yes	Yes	–	Resident
Cross assembly (what system?)	–	Yes	Yes	–	IBM 370
Simulators (For what)	–	Yes	Yes	–	IBM 370
Languages	BASIC; FORTRAN	No	No	APL	–
Operating System	Yes	Monitor	Monitor	AVS virtual OS	Yes
Software (bundled?)	Bundled	No	No	Yes	Yes
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	–	No
Commercial processing	Yes	–	–	Yes	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	No
Process-control	Yes	Yes	Yes	Yes	Yes
Any others?		Educational use; OEM prototyping	Educational use; OEM prototyping	Technical problem solving; scientific problem solving	Software development; microcomputer product testing and text editing
First Delivery	10/75	5/75	11/75	11/74	5/75
Number delivered	–	100	–	100 +	12
STANDARD SYSTEM	1K words ROM or 1K words RAM	256 bytes PROM, 256 bytes RAM	256 bytes PROM and 512 bytes RAM	With 32K ROM; 2K words RAM	With 1K ROM; 8K RAM
PRICE, $	2000	395	495	6500	3850
Other Features	Fully transparent to all applications for the Data General Nova	Extra RAM available to bring capacity up to 1K at $950/256 bytes; 4K RAM board avail Kit only price–$295	Extra RAM available to bring capacity up to 1K at $950/256 bytes; kit only price–$445	Price includes 100K bytes virtual cassette storage; power fail/protect; I/O interface; printer/plotter driver; integral display; keyboard; virtual operating system	Complete development system; 8K RAM, 2 cassette tape drives; keyboard; display, real-time clock interface to printer and PROM programmer

SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	MITS	Monolithic Memories	Motorola	Mycro-Tek, Inc.	National Semiconductor
Model Number	Altair 8800	MMI 300	6800	MT 8080 PB	PACE
PHYSICAL PACKAGE					
Number of boards	1 to 16	1 to 13	–	1	–
Dimensions	17 x 15"	6.6 x 9.6" cards	–	13.5 x 7.5"	–
Number of chips	1	Various	6	–	1
Number of pins/chip	40	Various; 14 to 40	40, 24	–	40
Power Supply (std, opt)	Std	Std; 5V	No	5V, 3A opt	+5, -12
Console (std, opt)	Std	N/A	No	MT 210 opt	–
Cabinet (std, opt)	Std	Opt	No	Opt	–
PROCESSOR					
Manufacturer	Intel	Monolithic Memories	Motorola	Intel	National
Model Number	8080	MMI 300	MC 6800	8080	IPC-16A/500
Technology Used (n/pMOS, bipolar)	nMOS	Bipolar	nMOS Si-Gate	nMOS	pMOS
Word size					
Data, bits	8	16	8	8	16
Instruction, bits	8	16	8, 16, 24	8	16
Clock frequency, KHz	2000	3300	100 to 1000	1843	2000
Add Time, reg to reg, μsec	2	0.9	2	2.71	8
Number of instructions	78	36 (expandable)	72	78	45
Number of registers	6	16	6	7	4
μprogrammed	No	Yes	No	No	No
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Opt		BCD, std	Std	Binary or BCD
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)		Bipolar	nMOS SiGate	pMOS/nMOS	pMOS/bipolar
Word size, bits		1 to 10	8	8	8; 16
Capacity, words		To 10K	1024	2K	512; 1K
Cycle time, μsec		100 max	0.575	0.5	
RAM (std, opt)				Opt	
Technology	nMOS	Bipolar; nMOS	nMOS SiGate	nMOS	nMOS
Word size, bits	8	64; 256, 1K bipolar 4K nMOS	8	8	4
Capacity, words	4K or 1K	4K max	128	1/4K to 8K	256
Cycle Time, μsec	0.47; 0.85	To 200	0.575	0.650	
PROM					
Technology	MOS	Bipolar	–	pMOS	pMOS
How programmed?	Electric	Fusible link	–		Stored charge
Word size, bits	8	1 to 10	–	8	8
Capacity, words	2K	8K	–	1K std, 4K opt	512
Cycle time, μsec	1	100	–	0.850	
INPUT/OUTPUT					
I/O word size, bits	8	16	8	8	16
Number of device addresses	256	62	4; 2	256	64K
Programmed I/O	Yes	Yes	Yes	Opt	Yes
Direct Memory Access	Yes	Yes	No	Opt	Yes
Type of interrupt system	8-level	microprogrammed	Vectored	8-level vectored	Hardware or software vectored
I/O rate, wds/sec	8.5	–	30K-bytes; 500Kbps	1M wds/sec	60K bytes
Device interfaces available (List)	Flexible disc drives; 110 char/sec line printer; ASR-33 TTY; CRT terminal; audio tape recorder; cyclops camera; plus general interfaces for most peripheral equipment		Modem; clocks; dynamic RAMS; static ROM; error pattern reg; longitudinal redundancy check, static character generators; A/D logic subsystem; bit rate generator polynomial generators	CRT with editor; control panel with monitor; high density memory; 32K on one card; high speed paper tape reader; line printer, dual cassette	16-bit bus transceiver (BTE); System clock (STE); 16-bit address latch (ALE/16); 8-bit address latch (ALE/8); 8-bit bidirectional interface latch (ILE/8); 16-bit bi-directional interface latch (ILE/16)
SOFTWARE					
Assembler	Yes	–	Resident/editor	Yes–MACRO	Yes
Cross assembly (what system?)	–	–	For time share nets	IBM	GE; Tymshare
Simulators (For what)	–	–	Selected 16-bit minis	IBM	–
Languages	Extended BASIC	Diagnostic	FORTRAN IV	PLM/Assembly	ASMB
Operating System	DOS-OS	Nova-type	EDOS Floppy disc	Yes	–
Software (bundled?)	Yes	Custom	Both bundled & unbundled	Yes	Most
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	No	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	General purpose computer			Education in microprocessor field; build up of small quantities	
First Delivery	1/75	–	4/74	4/75	4/75
Number delivered	3500	–	–	10	–
STANDARD SYSTEM	With 1K words RAM	With 8K RAM	MPU, 2K RAM, 8K ROM, 2 PIAs + one ACIA, diagnostics for debugging; pc board	With 1K ROM/with 1K RAM	–
PRICE, $	760/(536 for kit)	1,850	149 1-99 Qty	750/975	–
Other Features	Real-time clock	Military temp range devices available	Exorciser evaluation modules, floppy disc system, high speed paper tape reader, memory I/O modules, software pkged in various storage media available	Comb. PC board and wire wrap on one card. On card power convertor eliminates 3 power supplies aimed at small quantity prototype build-up	8 or 16-bit data handling; 5-level vectored priority interrupts

MANUFACTURER	National Semiconductor	PCS	PCS	Plessey Microsystems	Pro-Log
Model Number	IMP-16	MICROPAC 80	MICROPAC 80/A	MIPROC-16	PLS-401
PHYSICAL PACKAGE					
Number of boards	–	5	5	3	1
Dimensions	–	–	–	10" x 19"	4.5 x 6.5"
Number of chips	5	–	–	44	–
Number of pins/chip	24	–	–	N/A	–
Power Supply (std, opt)	+5, -12	Std	Std	+5V Std	+5V and -10V
Console (std, opt)	–	Std	Std	Std	–
Cabinet (std, opt)	–	Std	Std	Std	–
PROCESSOR					
Manufacturer	National	Intel	Intel	–	Intel, National
Model Number	IMP-16A/500	8080	8080	–	4004
Technology Used (n/pMOS, bipolar)	pMOS	nMOS	nMOS	Bipolar	pMOS
Word size					
Data, bits	16	8	8	16	4
Instruction, bits	16	8-24	8-24	16	8
Clock frequency, KHz	700	2000	2000	3000	714.3
Add Time, reg to reg, μsec	4.2	1.5	1.5	0.35	44.8
Number of instructions	43-71	78	78	82	44
Number of registers	4	7	7	256	16
μprogrammed	Yes	No	No	Yes	No
Fixed-point Arithmetic (+, -, X, ÷)					
Implementation (binary, BCD); (std, opt)	Binary	Std	Std	Binary	User-programmed
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	pMOS/BIP	–	–	Bipolar	–
Word size, bits	8; 16	8	8	16	–
Capacity, words	512; 1K	64K	64K	4K	–
Cycle time, μsec		1	1	0.075	–
RAM (std, opt)					
Technology	nMOS	–	–	Bipolar	pMOS
Word size, bits	4	–	–	16	4
Capacity, words	256	64K	64K	4K	320
Cycle Time, μsec		1	1	0.050	11.2
PROM					
Technology	pMOS	–	–	Bipolar	pMOS silicon gate
How programmed?	Stored charge	–	–	Fuse link	Series 90 PROM programmer
Word size, bits	8	8	–	16	8
Capacity, words	512	64K	64K	4K	1K
Cycle time, μsec		1	1	0.070	11.2
INPUT/OUTPUT					
I/O word size, bits	16	16	16	16	4
Number of device addresses	64K	256	256	512	4
Programmed I/O	Yes	Std	Std	–	–
Direct Memory Access	Yes	No	No	No	No
Type of interrupt system	Hardware or software vectored	Vectored	Vectored	Externally vectored	No
I/O rate, wds/sec	180K bytes	140K	140KB	3M	190K
Device interfaces available (List)	16-bit bus transceiver (BTE); System clock (STE); 16-bit address latch (ALE/16); 8-bit address latch (ALE/8); 8-bit bidirectional interface latch (ILE/8); 16-bit bidirectional interface latch (ILE/16)	TTL; high and low level digital and analog; TTY; RS 232 high speed communications, strain gage, stepper motor peripheral, interrupt expander, real-time clock; battery pack; PROM programmer	TTL; high and low speed analog and digital; TTY; RS 232; high speed communications; strain gage; stepper motor; peripheral; interrupt expander; real-time clock; battery pack	TTY; RS232;tape reader	TTL; Relay; opto-isolators; TRIAC's TTY; drivers; TTL to Hi-Ninil; MOS
SOFTWARE					
Assembler	Yes	Yes	MACRO	–	–
Cross assembly (what system?)	GE; Tymshare	HP-2100	HP 2100	FORTRAN IV	–
Simulators (For what)	–	No	No	Yes	–
Languages	ASM8; SM/PL	Assembly	Assembly	Yes	Assembly
Operating System	FDOS	BOS 80	BOS 80/A	–	–
Software (bundled?)	Most	Yes	Yes	Bundled	–
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	No	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?				Military	Automatic test equipment
First Delivery	6/72	3/74	6/75	1975	2/73
Number delivered	–	300	5	12	–
STANDARD SYSTEM	–	With 1K words ROM	With 1K words ROM	With 1K wds RAM	With 1K word ROM (single quantity)
PRICE, $	–	2650	2950	760 in quantity	275 at 500 quantity, price is $171 with 1K words PROM and 320 bits of RAM
Other Features	Optional instruction sets avail; also user micro-programmable	Hardware used by almost all major industries			

SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Pro-Log	Pro-Log	Pro-Log	R2E	RCA Cosmac
Model Number	PLS-441	MPS-803	MPS-883	MICRAL	Microkit
PHYSICAL PACKAGE					
Number of boards	1	3	3	–	11
Dimensions	4.5 x 6.5"	4.5 x 6.5"	4.5 x 6.5"	–	4.5 x 3"
Number of chips	–	–	–	1	–
Number of pins/chip	–	–	–	–	–
Power Supply (std, opt)	+5V, -10V	+5V, -9V	+12V, +5V, -10V	Std	+5, +12, -9 (110AC)
Console (std, opt)	–	–	–	Std	No
Cabinet (std, opt)	–	–	–	Std	–
PROCESSOR					
Manufacturer	Intel	Intel	Intel	Intel	RCA
Model Number	4040	8008	8080	8008	COSMAC
Technology Used (n/pMOS, bipolar)	pMOS	pMOS	nMOS	–	CMOS
Word size					
Data, bits	4	8	8	8	8
Instruction, bits	8	8	8	8, 16, 24	8
Clock frequency, KHz	714.3	357	625 or 1000	–	2000
Add Time, reg to reg, μsec	44.8	14	5 or 8	12.5	
Number of instructions	52	48	111	52	59
Number of registers	24	7	7	15	16
μprogrammed	No	No	No	No	No
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	User-programmed	User-programmed	User programmed	Binary	Binary
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	–	–	–	Bipolar	–
Word size, bits	–	–	–	8	–
Capacity, words	–	–	–	16K	–
Cycle time, μsec	–	–	–	1.0	–
RAM (std, opt)					
Technology	pMOS	nMOS	nMOS	MOS	nMOS
Word size, bits	4	8	8	8	8
Capacity, words	640	2K	2K	16K	1024
Cycle Time, μsec	11.2	2.8	1.6; 1	1.0	0.65
PROM					
Technology	pMOS silicon gate	pMOS silicon gate	pMOS silicon gate	Bipolar	nMOS
How programmed?	Series 90 PROM programmer	Series 90 PROM programmer	Series 90 PROM programmer	–	ER and Elec.
Word size, bits	8	8	8	8	8
Capacity, words	1280	1K	1K	16K	512
Cycle time, μsec	11.2	2.8	1.6 or 1	1.0	0.7
INPUT/OUTPUT					
I/O word size, bits	4	8	8	8	8
Number of device addresses	4	4	4	64	Any
Programmed I/O				Std	Yes
Direct Memory Access	No	Yes	Yes	No	Yes
Type of interrupt system	Single interrupt	Multi-level	Multi-level		Software
I/O rate, wds/sec	190K	250K	500K	1M	250K (DMA)
Device interfaces available – (List)	TTL; Relay; Opto-isolators; TRIAC's; TTY; drivers; TTL to Hi-NiNil; MOS	TTL; relay; opto-isolators; TRIAC's; TTY; drivers; TTL to NiNil; MOS	TTL; relay; opto-isolators; TRIAC's; TTY; Drivers; TTL to HiNil; MOS	Optical electronic inputs; relay output; TTY, magnetic tape, paper tape; printer	TTY (ASR 33) 38 execu-port; T.I. silent 700
SOFTWARE					
Assembler	–	–	–	Yes	Cross, batch
Cross assembly (what system?)	–	–	–	–	FORTRAN IV
Simulators (For what)	–	–	–	–	Cross-A
Languages	Assembly	Assembly	Assembly	–	Assembly
Operating System	–	Monitor program	Monitor program	TTY; cassette	–
Software (bundled?)	–	No	No	Yes	No
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	–	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	–	Yes
Terminals	Yes	Yes	Yes	–	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	Automatic test equipment	Automatic test equipment	Automatic test equipment	Message switching; preprocessing	
First Delivery	5/75	2/74	6/75	3/73	–
Number delivered	–	–	–	–	–
STANDARD SYSTEM	With 1K words ROM (single quantity)	Single quantity with 1K of 1702A PROM	Single quantity with 1K of 1702A PROM	With 256 wds of ROM	With 1K words RAM
PRICE, $	450 at 500 qty, price is $265 with 1K words of PROM and 320 bits of RAM	725	865	1,700 OEM discounts available	3000
Other Features					

MANUFACTURER	Rockwell	Rockwell	Scientific Micro Systems	Scientific Micro Systems	Signetics
Model Number	PPS-4	PPS-8	SMS-300	SMS-3000 (MCSIM)	N 3001
PHYSICAL PACKAGE					
Number of boards	–	–	1	14-20	–
Dimensions	–	–	2-5/8 x 6-7/8"	–	–
Number of chips	1	1	1	–	1
Number of pins/chip	42	42	64	–	40
Power Supply (std, opt)	-17V	-17V	No	Std	5V
Console (std, opt)	No	–	No	Std	–
Cabinet (std, opt)	No	–	No	Std	–
PROCESSOR					
Manufacturer	Rockwell	Rockwell	SMS	SMS	Signetics
Model Number	PPS-4	PPS-8	SMS-300	SMS-300	N3001
Technology Used (n/pMOS, bipolar)	pMOS	pMOS	Bipolar	Bipolar	Schottky bipolar
Word size					–
Data, bits	4	8	8	8	11 minimum
Instruction, bits	8	8	16	16	222,000
Clock frequency, KHz	199KC	256KC	6666	6666	–
Add Time, reg to reg, μsec	0.15	12	0.3	0.3	19
Number of instructions	50	109	8	8 types	1
Number of registers	7	9	8	8	Yes
μprogrammed	Yes	Yes	No	No	
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Binary	Binary	Software	Software subroutines	Microprogrammed
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	pMOS	pMOS	Bipolar	NA	Bipolar
Word size, bits	8	8	16	NA	4, 8
Capacity, words	4K	16K	512 8-bit	NA	32 to 1K
Cycle time, μsec	5	4	70	NA	0.05
RAM (std, opt)				Std	
Technology	pMOS	pMOS	NA	Bipolar	Bipolar
Word size, bits	4	8	NA	16	1, 2, 4, 9
Capacity, words	4K	16K	NA	4K	4 to 1K
Cycle Time, μsec	5	4	NA	60nsec	0.05
PROM					
Technology	EEROM (elec erasable)	EEROM (elec erasable)	Bipolar	NA	Bipolar
How programmed?	Microprocessor	Microprocessor	Fused link	NA	NI-CR Link
Word size, bits	8	8	8	NA	4, 8
Capacity, words	256	256	512 8-bit	NA	32 to 512
Cycle time, μsec	–	PPS compatible	70	NA	0.05
INPUT/OUTPUT					
I/O word size, bits	4	8	2 to 8	1 to 8	9
Number of device addresses	–	–	512	512	1
Programmed I/O	Yes	Yes	Yes	Yes	–
Direct Memory Access	No	Yes	No	No	–
Type of interrupt system	None	Vectored	Software emulation	Software emulation	Priority
I/O rate, wds/sec	100K	125K	250-35K	200K-350K	–
Device interfaces available – (List)	Floppy disc controller; serial data controller; telecommunications data controller; parallel data controller; gp I/O; gp keyboard and display; keyboard and printer; printer controller; victor dot matrix printer	Floppy disc; serial data; telecommunications data; parallel data; gp I/O; GP keyboard and display; keyboard and printer; victor dot matrix printer; display			All 7400, 8T, 74LS, 74S series devices; all TTL-compatible devices
SOFTWARE					
Assembler	Yes	Yes	Yes	Yes	Micro assembler
Cross assembly (what system?)	IBM 370, GE	370, GE, Tymshare	FORTRAN source	FORTRAN source	–
Simulators (For what)	Hardware/software	Hardware/software	No	Hardware simulation	–
Languages	Assembly	Assembly	–	–	–
Operating System	ROM resident	ROM resident	–	Yes	–
Software (bundled?)	Yes	Yes	No	No	–
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	No	No	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	Communication concentrators	Communication concentrators	Data communication controller, mux and concentrator	Data communication controller, mux and concentrator	Electronic games; peripheral equipment; communications
First Delivery	1973	1975	1975	1975	7/75
Number delivered	Over 1 million	Thousands	100 +	12	–
STANDARD SYSTEM	With 1K words ROM/ 1K words RAM	With 1K ROM in 100-unit quantities; 1K RAM	With 1K words ROM	With 1K words RAM	With 1K words ROM
PRICE, $	51/71 (Qty of 100)	68.50/108.50 (100 qty)	505 (for qty 1)	4895 (for qty 1)	20
Other Features	All modular LSI, no TTL required; smart I/O's contain address information so that I/O polling is not required after interrupt occurs; DMAC controls up to 8 blocks of data on a priority basis	All modular LSI, no TTL required; smart I/O's contain address info so that I/O polling is not required after interrupt occurs; DMAC controls up to 8 blocks of data on priority basis	Control-oriented, 1-board system with expandable I/O interface	MCSIM is real-time in-circuit simulation of SMS microcontroller systems. Programs are checked and verified in users environment	Multibus structure; masking capability; non-destructive data testing; zero detection; carry look ahead operation

SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Signetics	Signetics	Texas Instruments	Texas Instruments	Texas Instruments
Model Number	N 3002	2650PC1001	TMS 1000	TMS 1200	8080
PHYSICAL PACKAGE					
Number of boards	–	1	1-chip	–	–
Dimensions	–	6 x 8	–	–	–
Number of chips		43	1	1	1
Number of pins/chip	28	16 to 40	8	40	40
Power Supply (std, opt)	5 Volts	No	No	No	Opt
Console (std, opt)	–	No	No	No	No
Cabinet (std, opt)	–	No	No	No	No
PROCESSOR					
Manufacturer	Signetics	Signetics	TI	TI	TI
Model Number	N3002	2650	TMS 1000	TMS 1200	8080
Technology Used (n/pMOS, bipolar)	Schottky bipolar	nMOS	pMOS	pMOS	nMOS
Word size					
Data, bits	2^n	8	4	4	8
Instruction, bits	7 minimum	18, 16, 24	8	8	8, 16, 24
Clock frequency, KHz	222,000	1000	400	400	3000-2080
Add Time, reg to reg, μsec	0.3	6.0	72 (mem-mem)	72 (mem-mem)	1.3-2
Number of instructions	40 +	75	43	43	78
Number of registers	11	7 GP, 2 status, 8 RAS	1 accumulator	1 accumulator	7 GP
μprogrammed	Yes	No	Yes*	Yes*	No
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Microprogrammed	Binary and BCD	Binary std	Binary std	Binary, BCD
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	Bipolar	Bipolar	pMOS	pMOS	pMOS; nMOS; bipolar
Word size, bits	4,8	8	4/8	4/8	8
Capacity, words	32 to 1K	1K	1024	1024	250-2K
Cycle time, μsec	0.05	1.0	3	3	0.5-1.5
RAM (std, opt)					
Technology	bipolar	nMOS	pMOS	pMOS	pMOS, nMOS, CMOS, bipolar
Word size, bits	1, 2, 4, 9	8	4	4	1-4
Capacity, words	4 to 1K	1K	64	128	256-4K
Cycle Time, μsec	0.05	1.0	3	3	1.5
PROM					
Technology	Bipolar	Bipolar	–	–	pMOS, nMOS, bipolar
How programmed?	NI-CR link	Fuse link	–	–	Fusible link, FAMOS
Word size, bits	4, 8	8	–	–	8, 4
Capacity, words	32 to 512	1K	–	–	250-2K
Cycle time, μsec	0.05	1.0	–	–	0.50-1.5
INPUT/OUTPUT					
I/O word size, bits	2^n	8 or serial	4 in, 8 out	4 in, 8 out	8
Number of device addresses	Unlimited	256 or 4 x 8 or 2 serial	2"	213	–
Programmed I/O	Yes	Std	Yes, 11 bits	Yes, 13 bits	–
Direct Memory Access	Yes	Std	No	No	No
Type of interrupt system	Priority	Vectored	No	No	Vectored, 8-level
I/O rate, wds/sec	–	176KB	Programmed	Programmed	–
Device interfaces available – (List)	All 7400, 8T, 74LS, 74S, series devices; all TTL compatible devices	TTY RS232 8-bit parallel	TMS 6011 UART; FIFO (TMS 4024); linear circuits; display drivers	TMS 6011 UART; FIFO (TMS 4024); linear circuits; display drivers	
SOFTWARE					
Assembler	Micro assembler	No	Yes	Yes	Resident
Cross assembly (what system?)	–	370 or PDP/11	GE, Tymshare, NCSS	GE, Tymshare, NCSS	FORTRAN IV
Simulators (For what)	–	2650 up	Target system	Target system	FORTRAN IV
Languages	–	FORTRAN IV	–	–	–
Operating System	–	No	No	No	Yes
Software (bundled?)		No	Yes	Yes	No
APPLICATIONS					
Replace Hard-wired logic	Yes	No	Yes	Yes	Yes
Commercial processing	Yes	No	Yes	Yes	Yes
Data acquisition	Yes	No	Yes	Yes	Yes
Terminals	Yes	No	Yes	Yes	Yes
Device controllers	Yes	No	Yes	Yes	Yes
Process control	Yes	No	Yes	Yes	Yes
Any others?	Electronic games; peripheral equipment; communications	Prototyping	Home appliances, liquid flow control metering	Home appliances, liquid flow control metering	Billing & accounting avionics
First Delivery	7/75	6/75	11/74	11/74	
Number delivered	–	25	–	–	
STANDARD SYSTEM	With 1K words ROM	With 1K ROM/1K RAM			
PRICE, $	11	975/975	Single chip 10	Single chip 10	
Other Features	Multibus structure; masking capability; non-destructive testing of data; zero detection; carry look-ahead operation	Std ROM contains PIPBUG, a signetics de-bugging package			Intel 8080 second source
			*discouraged	*discouraged	

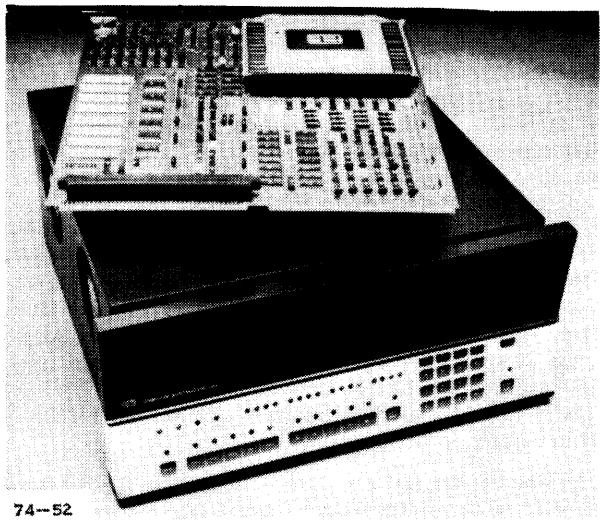
MANUFACTURER	Texas Instruments	Three Phoenix	Toshiba America	Toshiba America	Transitron Electronic Corp
Model Number	TMS 990/04	PTT 8000	TLCS-12 EX-2	TLC-12A EXIA	TDS/16
PHYSICAL PACKAGE					
Number of boards	NA, 1-chip	3	14 boards	13	Rack mount cabinet
Dimensions	–	14" x 5"	–	–	5.25 x 19 x 12
Number of chips	1	–	1 chip CPU	1	–
Number of pins/chip	64	–	42 pins	36	–
Power Supply (std, opt)	Opt	Std	Std	Std	Std
Console (std, opt)	Opt	–	Opt	Std	Std
Cabinet (std, opt)	Opt	–	Opt	Std	Std
PROCESSOR					
Manufacturer	TI	Intel	Toshiba	Toshiba	Transitron
Model Number	TMS 9900	8008	T3153	T3190	TMC-1601
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	pMOS Si-Gate E/D	pMOS Si-Gate E/D	Bipolar (Schottky)
Word size					
Data, bits	16	8	12	12	16
Instruction, bits	16/32/48	8	12, 24	12; 24	16, 32, 48
Clock frequency, KHz	3000	4193.2	1000	1000	5000
Add Time, reg to reg, μsec	4.6	–	10	10	0.4 incl memory fetch
Number of instructions	69	–	18	20	95
Number of registers	16	–	8 GP	8 GP	8 gen, 3 dedicated
μprogrammed	No	–	Yes	Yes	Yes
Fixed-point Arithmetic (+, –, X, ÷) Implementation (binary, BCD); (std, opt)	Binary; hdwr/multiply divide std	–	Binary std	Binary std	Software BCD
MEMORY					
Types – (ROM/RAM/PROM)					
ROM					
Technology (n/pMOS, bipolar)	EROM	None	pMOS Si-Gate E/D	pMOS Si-Gate E/D	Bipolar
Word size, bits	16	–	128 x 4	512 x 8 or 1024 x 4	16
Capacity, words	32K	–	8.5K x 12/system	3.5 x 12/system	32K
Cycle time, μsec	1.0	–	1	1.0	0.20
RAM (std, opt)					
Technology	nMOS	Std	pMOS Si-Gate E/D	pMOS Si-Gate E/D	Bipolar
Word size, bits	16	8	128 x 4	128 x 4	16
Capacity, words	58K	1K	4K x 12/system	4K x 12/system	32K
Cycle Time, μsec	1.33		1	1	0.20
PROM	Opt	Opt			Opt
Technology	–	–	pMOS Si Gate	pMOS Si-Gate	Bipolar
How programmed?	PROM programmer opt	–	Electrical	Electrical	Fusible link
Word size, bits	16	8	512 x 4	512 x 4	16
Capacity, words	32K	3K	3.5K x 12/system	3.5 x 12/system	32K
Cycle time, μsec	0.66		1.0	1	0.20
INPUT/OUTPUT					
I/O word size, bits	1-16	8	12	12	8 or 16
Number of device addresses	256	16	3K	3K	52
Programmed I/O	Yes	Yes	None	None	Yes
Direct Memory Access	Yes	Yes	Opt	Opt	Data channel
Type of interrupt system	8 vectored interrupts	None	8 priority levels	8 priority levels	Vectored 4-level
I/O rate, wds/sec	1.5M bps; 1M wds/sec	–	–	–	1M wds/sec
Device interfaces available (List)	EIA RS232; TTL; 16 in, 16 out, EIA 16 in, 16 out; Async; Sync; ASR; KSR; TI 733, Model 913 video display, card reader, floppy disc; printer, PROM programmer; cartridge disc		TTY/CASHIO M-500/ TEKTRO 4101 interface; PROM programming module; PTR; PTP; printer (Diablo); digital cassette; typewriter (IBM 735); analog input interfaces	TTY/CASHIO M-5000/ TEKTRO 4010; PROM programming module; PTR; PTP (FACIT); digital cassette; typewriter (IBM 735); analog input interfaces	Paper tape reader, paper tape punch; card reader; serial printer; line printer; floppy disc; CRT; TTY
SOFTWARE					
Assembler	Yes	–	Yes	Yes	Yes
Cross assembly (what system?)	GE, NCSS, Tymshare	–	GE 635	GE 635 (TOSBAC 5600)	Tymshare
Simulators (For what)	TMS 9900 microprocessor	–	GE 635	GE 635 (TOSBAC 5600)	Tymshare
Languages	Assembler	–	Assembler	Assembler	N/A
Operating System	Yes	–	Yes	No	FLOS (Floppy disc)
Software (bundled?)	–	–	Yes	Yes	Priced separately
APPLICATIONS					
Replace Hard-wired logic	Yes	No	Yes	–	Yes
Commercial processing	–	No	Yes	–	Yes
Data acquisition	Yes	Yes	Yes	–	Yes
Terminals	Yes	Yes	Yes	–	Yes
Device controllers	Yes	No	Yes	–	Yes
Process control	Yes	No	Yes	–	Yes
Any others?	Prototype development systems support for TMS 9900		Machine-tool control; industrial robot instrumentation	System software development	Software development system for TMC/1601
First Delivery	1st quarter 1976	–	1974	1975	Fall/75
Number delivered	–	–	10K kits	1K kits	–
STANDARD SYSTEM	990/4 with 8K wds memory, 6 slot chassis, 20 amp power; programmer's panel and TI 733 ASR	With 1K words RAM	With 1K wds ROM/ with 1K RAM	With 1K words ROM/ with 1K words RAM	–
PRICE, $	5,950	2500	2000/2350	1790/2140	–
Other Features	Prototyping system 16K-byte memory, Silent 700 ASR, and PROM kit				Hardware multiply/divide; RAM stack; real-time clock; software-diagnostics; editor; debugger subroutine library; 90 day warranty

SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Transitron Electronic Corp	Warner & Swasey	Warner & Swasey	Warner & Swasey	Warner & Swasey
Model Number	TMC/1601	Comstar System 4	Comstar System 4A and 4B	Comstar System 8A	Comstar System 8D
PHYSICAL PACKAGE					
Number of boards	1	Depends on configuration	Depends on configuration	Depends on configuration	Depends on configuration
Dimensions	8 x 8"	4.5 x 4.5	4.5 x 4.5	4.5 x 4.5"	4.5 x 4.5"
Number of chips	40	–	–	Variable	Variable
Number of pins/chip	–	–	–	–	–
Power Supply (std, opt)	+5V	Opt	Opt	Opt	Opt
Console (std, opt)	–	Opt	Opt	Opt	Opt
Cabinet (std, opt)	–	Opt	Opt	Opt	Opt
PROCESSOR					
Manufacturer	Transitron	Intel	Intel	Warner & Swasey	Warner & Swasey
Model Number	–	4004	4040	M8-A	M8-D
Technology Used (n/pMOS, bipolar)	Bipolar (Schottky)	pMOS	pMOS	Bipolar	Bipolar
Word size					
Data, bits	16	4	4	8	8
Instruction, bits	16, 32, 48	8; 16	8; 16	8-48	8-48
Clock frequency, KHz	5000	5,185	5,185 & 8000	4000	8000
Add Time, reg to reg, μsec	0.40 incl mem. fetch cycle	10.8	10.8; 7.0	2.75	1
Number of instructions	95	46	60	114	114
Number of registers	8 gen; 3 dedicated	16	24	32	256
μprogrammed	Yes	No	No	Yes	Yes
Fixed-point Arithmetic (+, –, X, ÷)					
Implementation (binary, BCD); (std, opt)	Software BCD	Std	BCD std	Firmware	Firmware
MEMORY					
Types – (ROM/RAM/PROM)					
ROM	Opt				
Technology (n/pMOS, bipolar)	Bipolar	–	–	nMOS	nMOS
Word size, bits	16	–	–	8	8
Capacity, words	32K	–	–	64K	64K
Cycle time, μsec	0.20	–	–	0.5	0.5
RAM (std, opt)		Opt	Opt	Opt	Opt
Technology	Bipolar	pMOS and CMOS	pMOS and CMOS	nMOS & CMOS	nMOS & CMOS
Word size, bits	16	4	4	8	8
Capacity, words	32K	2.5K	10.24K	64K	64K
Cycle Time, μsec	0.20	10.8	10.8 & 7.0	0.5 & 0.75	0.375, 0.5 & 0.75
PROM					
Technology	Bipolar	pMOS	pMOS	nMOS	nMOS
How programmed?	Fusible link	Opt programming device	Opt programming device	Opt programming device	Opt programming device
Word size, bits	16	8	8	8	8
Capacity, words	32K	4K	8K	64K	64K
Cycle time, μsec	0.20	10.8	10.8 & 7.0	0.5	0.5
INPUT/OUTPUT					
I/O word size, bits	8 or 16	4	4	8	8
Number of device addresses	64	64	64	256	256
Programmed I/O	Yes	Yes	Yes	Yes	Yes
Direct Memory Access	Yes (data channel)	No	No	Multiport RAM	Multiport RAM
Type of interrupt system	Vectored 4-level	–	16 priority levels	7-level	7-level
I/O rate, wds/sec	1M wds/sec	11.5K	11.5K & 17.8K	2M	2M
Device interfaces available – (List)	Paper tape reader; paper tape punch; card reader; serial line printer; floppy disc; CRT teletype	Line printer; paper tape reader and punch; mag tape cassette; mag tape xport; floppy disc; card reader; A/N display; TTY, RS-232C; analog, digital and power switching interface modules	Line printer; paper tape reader/punch; mag tape xport; floppy disc; card reader; AN display; TTY; RS-232C; analog, digital and power switching interface modules; mag tape cassette	Line printer; paper tape reader/punch; mag tape cassette; floppy disc; card reader; A/N display; LED display; RS-232C or 20 MA TTY current loop thumbwheel switches; serial data comm	Line printer; paper tape reader/punch; mag tape cassette; floppy disc; card reader; A/N display; LED display; RS-232C or 20 MA TTY current loop thumbwheel switches; serial data comm
SOFTWARE					
Assembler	Yes	No	No	No	No
Cross assembly (what system?)	Tymshare	ANSI FORTRAN IV	ANSI FORTRAN IV	ANSI FORTRAN IV	ANSI FORTRAN IV
Simulators (For what)	Tymshare	No	No	No	No
Languages	N/A	Comstar Process	Control compiler	FORTRAN	FORTRAN
Operating System	FLOS (floppy disc)	No	No	Yes	Yes
Software (bundled?)	Priced separately	No	No	Yes	Yes
APPLICATIONS					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	No	No	No	No
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?		Control applications for industrial automation; machine tool control; traffic control	Control applications for industrial automation; machine tool control; traffic control; material handling	Machine tool, traffic, and industrial computer control; data entry and retrieval; material handling	Machine tool, traffic, and industrial computer control; data entry and retrieval; material handling control
First Delivery	Fall/75	2/72	3/75; 4/75	5/75	7/75
Number delivered	–	1200	40; 10	–	–
STANDARD SYSTEM		With 1K words RAM	With 1K words RAM	CPU; real-time clock; 1K RAM; power supply; monitor/control	CPU; real-time clock; 1K RAM; power supply regulators; monitor/control unit
PRICE, $	–	1200	1200	2000	2300
Other Features	Hardware multiply/divide; RAM stack; real-time clock; software diagnostics; editor; debugger; subroutine library; 90 day warranty	114 I/O modules available incl clocks, modems, timers; Machine language and process control programming equipment; self teaching educator; diagnostic and test equipment	114 I/O modules available includes clocks, timers, modems; machine lang and process control lang; programming equipment; self-teaching educator and complete diagnostic and test equipment	Std system also includes 64 TTL inputs, 32 outputs, cabling; multiply/divide; commercial and wide temp versions available	Std system also includes 64 TTL inputs, 32 outputs, cables; multiply/divide; commercial and wide temp versions; overflow and floating pt arith

MANUFACTURER	Western Digital	Wintek
Model Number	MCP 1600	W6800
PHYSICAL PACKAGE		
Number of boards	1	Variable
Dimensions	8 x 10	5.75" x 6"
Number of chips	–	Variable
Number of pins/chip	–	–
Power Supply (std, opt)	–	Std
Console (std, opt)	–	Opt
Cabinet (std, opt)	–	Opt
PROCESSOR		
Manufacturer	Western Digital	Motorola
Model Number	MCP 1600	M6800
Technology Used (n/pMOS, bipolar)	nMOS	nMOS
Word size		
Data, bits	8; 16	8
Instruction, bits	16	8
Clock frequency, KHz	3300	100
Add Time, reg to reg, μsec	2.1 (16-bits)	2
Number of instructions	84	72
Number of registers	26	Two 8-bit; three 16-bit
μprogrammed	Yes	No
Fixed-point Arithmetic (+, –, X, ÷)		
Implementation (binary, BCD); (std, opt)	Microprogrammable	Opt
MEMORY		
Types – (ROM/RAM/PROM)		
ROM		
Technology (n/pMOS, bipolar)	nMOS	–
Word size, bits	8	–
Capacity, words	1K	–
Cycle time, μsec	0.3	–
RAM (std, opt)		Static; dynamic
Technology	nMOS	nMOS
Word size, bits	4	8
Capacity, words	256	4K bytes/module; 8K bytes/module
Cycle Time, μsec	0.3	0.65; 0.35
PROM		
Technology	–	MOS, eROM
How programmed?	–	1702A programmer
Word size, bits	–	8
Capacity, words	–	2K bytes/module
Cycle time, μsec	–	1.5
INPUT/OUTPUT		
I/O word size, bits	16	8
Number of device addresses	65K	Variable
Programmed I/O	Yes	Std
Direct Memory Access	Yes	Opt
Type of interrupt system	4 priority levels	Vectored (opt)
I/O rate, wds/sec	–	1M
Device interfaces available – (List)	Serial communications; floppy disc controller available 1/75	Std I/O and mass memory devices
SOFTWARE		
Assembler	Yes, Tymshare	–
Cross assembly (what system?)	PDP 11 & PDP 10	Tymshare
Simulators (For what)	Micro level	Tymshare
Languages	Assembly	PL/1 (2nd qtr 76)
Operating System	Yes	–
Software (bundled?)	No	–
APPLICATIONS		
Replace Hard-wired logic	Yes	Yes
Commercial processing	Yes	–
Data acquisition	Yes	Yes
Terminals	Yes	–
Device controllers	Yes	–
Process control	Yes	Yes
Any others?	Emulation of existing sets; data base computations; minicomputer applications	Custom hardware and applications
First Delivery	–	9/75
Number delivered	–	–
STANDARD SYSTEM	With 1K words ROM	With 1K wds ROM/ with 1K wds RAM
PRICE, $	250 (over 100)	1900/1600
Other Features	Microprogrammable to allow 3 levels of application. 1) emulation; 2) fast micro level controllers; 3) miniprocessor	For custom applications

COMPUTER AUTOMATION INC.
LSI Series System Report



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OVERVIEW

Computer Automation's LSI Series consists of low-cost 16-bit, microprogrammed minicomputers aimed exclusively at the OEM market. Like their predecessors, Naked Mini-16 and Alpha-16, the LSI Series is packaged in "naked" versions without power supply or console, as well as in "alpha" versions with these features. All are microprogammed and organized around a Maxi-Bus® with at least three major I/O subsystems: DMA, direct memory channels, and programmed I/O. All LSI Series computers except the 3/05 also have block transfer I/O capability.

The LSI Series uses two basic processors. LSI processor 3/05 uses bipolar MSI technology and is mounted on a half-size 7 x 15-inch board. It competes with microcomputers and small minicomputers. The LSI-2 systems all use the same TTL MSI processor, although the processor cycle time for the Model 2/10 is half that of the 2/20 or 2/60. The 2/60 is the MEGABYTER system, allowing attachment of up to one million bytes of memory. Thus, the line extends across the whole range of the minicomputer market.

All models have the same basic architecture, same number of registers; same priority interrupts; same word or byte addressing using eight addressing modes; same 4K/8K/16K-word core memory modules; same combination modules of RAM, ROM, and PROM; and so on. The chief differences are in speed, instruction set, and memory capacity. Table 1 lists characteristics common to all models.

The LSI-2/60, or MEGABYTER, added to the line in 1975, extends the capabilities of the LSI-2 line upward by adding instructions optimized for real-time, multiprogramming, communications, and business applications and by expanding memory capacity to one million bytes in 32K-word memory banks. The MEGABYTER uses the same processor as the rest of the LSI-2 line, thus it can use all the peripherals and software developed for other LSI-2 models. The LSI-2/60 implements the following facilities in addition to those available for the LSI-2/10 and 2/20:

- Expansion of the 2/20's stack processing capabilities.
- String instructions that can move up to 255 bytes at a time, can compare strings, and can move mismatched characters.
- Decimal arithmetic for adding and subtracting up to 31 digit strings.
- Bit manipulation; direct addressing to the bit level.

CRC (cyclic redundancy check), character generation, hardware multiply/divide, and interleaved memory are standard features.

The NAKED MILLI LSI-3/05, also added in 1975, uses the same basic architecture as the LSI-2 Series; but the processor is different, with a cycle time that is somewhat slower. The LSI-2 Series uses a faster processor and either 960-nanosecond or 1,200-nanosecond memory modules. Although LSI-3/05 uses the same 1,200-nanosecond memory as the LSI-2 Series the processor slows instruction execution time. Thus, execution time for an add or subtract instruction is 6.0 microseconds on the LSI-3/05, 2.4 microseconds on the 2/10, and 2.06 microseconds on the 2/20 and 2/60. The 2/10 uses the same processor as the 2/20 and 2/60, but cycle time is halved.

LSI-3/05 is designed with bipolar MSI circuitry and TTL logic to produce a compact, low-cost system. However, the NAKED MILLI is still upward compatible with the LSI-2 line and can attach the same peripherals and interfaces as the larger systems. Programs developed on LSI-2 systems can run on the LSI-3/05 by using subroutines for missing instructions. Table 2 lists the differences among the LSI Series models.

HEADQUARTERS
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18651 Von Karman
Irvine CA 92664
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Table 1. CAI LSI Series: Common Mainframe Characteristics

Characteristics	LSI Series
CENTRAL PROCESSOR	
General-Purpose Registers	8
Addressing	
Direct	768 words or bytes
Indirect	Multilevel, to 32K wd or 64K bytes/level; 128K wd max
Indexed	Yes
Floating-Point Arithmetic	No
Priority Interrupt Levels (std; max)	5; 256
MAIN STORAGE	
Type	Semiconductor; core; mixed
Cycle Time (μ sec)	0.96; 1.2
Basic Addressable Unit	Word or byte
Increment Sizes (bytes)	8K, 16K, 32K (core); 1K, 2K, 4K, 8K (MOS)
Memory Parity	Opt
Memory Protect	No
ROM	Yes
RAM	Yes; can be mixed with core
I/O Transfer Rate	
DMA (wd or bytes/sec)	625,000 (1.25M with interleaved memory)
Programmed I/O	34,247 via registers
Programmed (wd or bytes/sec)	24,631 direct to memory
Direct Memory Channels (wd or bytes/sec)	26,738
No. of DMA Channels (std; opt)	2; 64
Conditional I/O	Std
Max Addressable I/O Devices	248

Computer Automation (CAI) was formed in August 1967 to manufacture and market minicomputers to the OEM market. Since its introduction of the Alpha and Naked Mini Series and the later LSI versions, the company has shipped more than 9,000 systems. It also produces and markets the Capable Tester System; this computer-driven production line tester for digital logic modules was originally designed for CAI's in-house logic production facility.

The Capable Tester line includes 12 models ranging from test-only models to systems that provide computerized design of test programs using a new simulation software system called BigSim. BigSim is a preproduction simulator that builds, refines, and verifies test programs from engineering designs of circuit boards with up to 400 integrated circuits. The models in the mid-range of the Capable Tester line are based on an LSI-2 with 16K words of memory; models using BigSim incorporate a disc-based LSI-2 with a 64K-word memory.

Table 2. Differences Among LSI Series Systems

Model Number	3/05	2/10	2/20	2/60
No. of Instructions	95	162	182	224
Stack Processing Instructions	No	No	Yes	Yes
Block Transfer I/O	No	Yes	Yes	Yes
Main Memory				
Min Size wd	256	4K	4K	8K
Max Size wd	32K	256K	256K	512K

Computer Automation has expanded steadily and now has 18 direct sales offices and service facilities in the United States. A number of distributors market CAI systems in other parts of the world; D.C. Industries in Australia; the Metric companies (Scandia Metric AB in Sweden, Finn Metric oy in Finland, SC Metric A/S in Denmark, and Metric A.S. in Norway) in the Scandinavian countries; Geveke Elektronica en Automatie nv in Belgium, Netherlands, Luxembourg, and Germany; Data Care AG in Switzerland; Tranchant Electronique in France; Computer Advances in South Africa; Alfatronica in Spain; and Electro Marketing in Japan. Computer Automation has its own subsidiary, CAI Ltd, in England for sales to the United Kingdom and for support in certain parts of Europe.

Peripherals for the LSI Series include discs, diskette, magnetic tape, printers, card reader, paper tape reader and punch, process I/O, and communications. The new distributed I/O interface can support up to eight intelligent cables, which can connect to a variety of peripherals. These programmable interfaces let users simplify interfacing to any serial or parallel I/O device.

Software for the LSI-2 Series includes DOS, COS, and MOS batch operating systems, BASIC, ALGOL, FORTRAN IV, and assembly language processors. A real-time executive (RTX) allows multiprogramming. An optimized version of the FORTRAN IV compiler, designed to produce more compact object code, was introduced in 1975 at the same time as the MEGABYTER and LSI-3/05 NAKED MILLI.

Software for the LSI-3/05 includes the RTX, an I/O executive (IOX), the OMEGA conversational assembler/editor, loader utilities, and a debug package. Programs developed under DOS on the LSI-2 can usually run on the LSI-3/05 without difficulty.

PERFORMANCE AND COMPETITIVE POSITION

The LSI Series extends across the entire minicomputer market, thus its members compete with different systems in different market segments. This has not always been the case. Former CAI systems, represented now by the 2/10 and to some extent the 2/20, tended to compete at the low end of the minicomputer market with the low and middle portions of the Data General Nova or the Digital PDP-11 lines, for example. The minicomputer market has now expanded, both downwards and upwards; and the LSI line has done likewise.

Computer Automation has a competitive advantage over minicomputer manufacturers who sell both to end

users and in the OEM market. Computer Automation sells only OEM, and customers are not concerned about the company becoming a competitor. Also, primarily as an OEM supplier, Computer Automation stresses thorough testing of system components, as well as reliability in meeting production deadlines and living up to contractual obligations.

Although Computer Automation entered the field only 7 years ago, the company grew rapidly until last year when its steady growth rate was slowed somewhat due to the unfavorable economic climate. Expansion of its product line at both ends and the new I/O interfacing has provided other markets for CAI systems and spurred a return to near previous growth levels. The company has delivered 9,000 systems and expects to hit a 10,000 figure in the last quarter of 1975.

The LSI-2/60 MEGABYTER expands the LSI-2 line upwards; it provides an upward path for current customers and should also attract new customers on its own merit. Its new instructions and the million-byte memory capacity make it suitable for large communications, data entry, real-time, or other multiprogramming systems capable of considerable expansion. The range in the instruction set, I/O structure, and memory capacity allow it to compete with the Digital PDP-11/45, Data General ECLIPSE, and Interdata 7/32 and 8/32. These companies sell their systems in OEM as well as end-user versions.

MEGABYTER does not perform memory mapping; instead, programs execute out of a 32K-word memory bank. An instruction is used to switch from one bank to another. Memory protect and hardware floating-point arithmetic are currently unavailable. The Universal Interface should save many OEM manufacturers considerable time and money in system building. The MEGABYTER is particularly suited to control multiterminal distributed processing systems for data entry, accounting, and text editing.

The Computer Automation LSI-3/05 NAKED MILLI occupies an intermediate position in the computer market, between microprocessors and minicomputers. Like microprocessors (the computers-on-a-chip), the 3/05 was designed to be a component. Even the power supply and console are priced separately. Like minicomputers, the LSI-3/05 Series has systems software so the user can quickly implement applications.

Microprocessors range in size and capability from the Intel single chip to National Semiconductor's four-chips-on-a-board. Some manufacturers provide only chip sets, leaving the user to provide I/O, interface logic memory, and programs. Others provide board-level systems that include memory and ease the I/O interfacing problems but rarely provide standard interfaces to peripherals other than Teletypes.

The big advantage of the CAI minicomputer lies in its completeness: memory, peripherals, and software. For many applications the LSI-3/05 costs the same as or less than an in-house developed microcomputer, and implementation of the total system would be faster with the LSI-3/05. The distributed I/O subsystem option supports the concept of quick and easy interfacing. In addition, the user of an LSI-3/05 can move up to the compatible LSI-2 Series if requirements outstrip the LSI-3/05 processor capability.

The NAKED MILLI LSI-3/05 has several competitors from minicomputer makers also trying to extend market penetration downward. Digital has used the Intel microcomputer in its MPS system, which is not compatible with the PDP-8 or PDP-11 lines.

Digital nas also introduced a bottom-of-the-line PDP-11 and PDP-8. The LSI-11 is a 1-board system with RAM memory and a 2-board system with core memory. The PDP-8/A is a compact 1-board CPU that is implemented with MOS technology. Both the PDP-8/A and LSI-11 are more expensive than the LSI-3/05.

Data General's Nova 2 is sold at the board level. It is faster than the LSI-3/05 and also more expensive.

User Reactions

A manufacturer of blood serum analyzers bought about 200 CAI LSI units as components, partly because of the price but largely because the 1-board CPU means simpler maintenance. The CAI computer is used for mathematical analysis of chemical reactions and for printing reports for doctors. The analyzers are controlled by another computer system. This user is very pleased with the performance of the system; CAI's support has been very good, and response to service requests is prompt. The user made only one criticism; he feels the programming manuals could be improved.

A second user is a prominent POS manufacturer using the system as a ROM simulator and a testing device for customized ROM units. The LSI-2 is programmed with the desired logic pattern, and the pattern is then tested before it is fused into ROM firmware by another system. The resulting chips are then retested by the CAI unit. The company bought 15 of the LSI-2 systems and is now using some as field trial units. This manufacturer has found the mini to be an excellent machine with a very good capacity. He likened it to a Nova system, with capabilities somewhere between the Digital PDP-8 and PDP-11.

A department in a communication equipment manufacturing facility bought a single LSI-2 with an 8K-word memory and a Teletype for an in-house machine control application. The department chose the system over Digital and Hewlett-Packard systems for three reasons: price, I/O structure, and the fact that a neighboring department had one.

This communication equipment user has had no problems whatsoever with his system, so he was unable to

Table 3. CAI Peripherals

Model No.	Description
DISCS	
22530	Moving Head Disc Subsystem; 1 fixed, 1 removable cartridge; 2.46M wd/drive; 4 drives/controller
22566	Floppy disc; 243K bytes/disc; dual drive; 2 dual drives/controller
TERMINALS	
22205-00	Teletype ASR 33-20/3JC; 10 cps
22230-00	A/N Display; 1,920 char, 24 x 80 char; 64-char set; to 9,600 baud
PUNCHED CARDS	
22077-20	285-cpm reader
PAPER TAPE	
22223-11	300-cps reader
22223-60	300-cps reader; 75 cps punch
PRINTERS	
22107-06	100 cps printer (60-150 lpm); 80 col
MAGNETIC TAPE	
22224-15	9-track; 800 bpi; 25 ips; 4 drives/controller
	Single/dual cassette drives; 520K bytes/cassette; 4 drives/controller
PROCESS I/O	
13213-00	Digital I/O; 16-bit DTL/TTL compatible
13214-20	Relay Output Module; 32-bit (1 x 32, 2 x 16, or 4 x 8)
13215-00	Relay Input Module; 32-bit (1 x 32, 2 x 16, or 4 x 8)
13216-00	Output Module; 64-bit (1 x 64, 2 x 32, 4 x 16, or 8 x 8)
13218-00	Input Module; 64-bit (64-, 32-, 16-, or 8-bit inputs)
14223	Utility I/O; 8- or 12-bit-parallel input or output
COMMUNICATIONS	
14236	Single or Dual Interface for 1 or 2 EIA RS232-compatible CRTs, leased line modems, or TTYs (current loop)
14535	Async Programmable Modem Controller; 1 line to 9,600 baud
14512	Async Programmable Modem MUX; for 2 or 4 lines
14513	Sync Programmable Modem Controller; to 50K baud
14523	Automatic Calling Unit MUX; for 1-4 ACUs.

Table 4. Naked Mini/Alpha LSI: Software

Package	Description
Real-Time Executive (RTX)	Modular system consisting of multitasking executive (RTX nucleus); I/O executive (IOX) subsystem; communications executive (COMX); requires 650 wd of memory and console.
Disc Operating System (DOS)	For control of sequential job operations; with system secondary storage on disc; requires 16K wd of memory, disc, Teletype, real-time clock, printer, paper tape I/O.
Operating System (OS)	For batch assembly & execution of user programs; supports disc storage, any combination of std peripherals; runs on any LSI-3 computer.
BETA Assembler (2 versions)	Relocatable; one version requires 4K wd of memory; another (8K) version supports unit record I/O with intermediate mass storage.
OMEGA Conversation Assembler	Adds on-line editing, updating, conversational capabilities to BETA.
360 Cross Assembler (XASM)	Written in IBM FORTRAN IV, Level G; produces output identical to BETA & OMEGA.
Advanced BASIC	Dartmouth BASIC with nested recursive subroutines, calculator mode & other extensions; requires 4K words of memory.
Extended BASIC	Advanced BASIC with string manipulation & matrix instructions; requires 8K words of memory.
Extended Multiple User BASIC	Same as Extended BASIC, but for 8 users; requires 8K words of memory (16K recommended).
FORTRAN IV	ANSI FORTRAN IV with added features; stresses compact object code; requires 16K words to compile, 8K words to run.
File Manager	Program storage & retrieval for small memories; 4K words of memory plus disc, magnetic tape, or cassette unit.
Utilities	Source tape preparation; loader; TTY/CRT utility; math packages; diagnostics.

offer any opinion on CAI's service organization. When asked what he thought about the programming manuals, he said they are as good as anyone else's manuals. Readers apparently feel that writers for all the manufacturers seem to leave something out as self-evident, when it is not self-evident to the user. This user's only annoyance was that he could not obtain logic diagrams and documentation on the memory board because it is proprietary. The user wanted to trace causes of trouble himself when it occurred.

CONFIGURATION GUIDE

All models in the LSI-2 and LSI-3 Series can be configured without console and power in the Naked line or in a package with chassis and power in the Alpha line.

All minimum Naked Minis consist of a processor with memory but no power or control console. The Naked Mini 16s and LSI-2s also include a chassis and motherboard with varying number of slots available, usually five or six. Jumbo versions have nine slots. The minimum NAKED MILLI LSI-3/05 has no chassis and motherboard; the CPU and up to 8K words of memory are all contained on a single board. Naked systems must be bought in minimum quantities of five units in the LSI Series and 10 units in the older 16 Series.

All Alpha systems include the processor, memory, chassis, power supply, and control console; slots are available on the minimum system for attachment of additional memory and controller/interfaces.

The following processor options are available for the LSI Series: power fail restart (PFR); Teletype 33 ASR interface; real-time clock (0.1, 1.0, and 10.0K Hertz) with two interrupts; autoload ROM (programmed for paper tape reader, Teletype, cassette, magnetic tape, or disc); and an EIA RS232 CRT interface that can be added to the Teletype interface. In addition, there is a Basic Variables option (a prerequisite for certain other options) offset of processor interrupts, enabling power fail interrupt, and sense register jumpering for operation without console. DMA is a standard feature. Processor options are mounted piggyback on the processor board instead of on a separate card, so they must be factory installed.

The minimum LSI-2 processor is contained on one board with memory on another, leaving three slots for additions. Each expansion chassis adds five or nine slots to the system. System size is limited by the maximum memory size (up to 256K words on LSI-2/10 or 2/20 and up to 512K words on the 2/60 with the Memory Bank Control option) and by the maximum number of peripherals that can be addressed (up to 256 individual device controllers) and handled by the system software. Peripheral offerings are summarized in Table 3.

Both LSI-3/05 and LSI-2 systems can be purchased without memory, or they can be packaged with various memory modules. The LSI-3/05 can attach all RAM, a RAM/ROM module, or RAM/EPROM (Erasable Programmable ROM) modules.

Computer Automation supplies three packaged Alpha LSI-2 configurations that are less expensive than the total of all components. These four configurations are available on short delivery.

- 30010-16 Standard DOS 20 — CPU, 16K words of core memory, all processor options except RS232 interface, disc (2.46 million words), printer, paper tape reader/punch, Teletype ASR 33 expansion chassis and power supply, and DOS software.
- 30010-32 Expanded DOS 20 — same as 30010-16 but with a total of 32K words of core memory.
- 30012-32 Expanded DOS 60 — same as 30010-32, except the LSI-2/20 is replaced by an LSI-2/60 MEGABYTER.

Minimum requirements for the other software packages, together with a brief description of the packages appears in Table 4.

COMPATIBILITY

The LSI-3 and LSI-2 Series are upward compatible; the 3/05 is upward compatible to the 2/10, 2/20, and 2/60. The 3/05 has subroutines available to simulate missing instructions so that programs developed on the other models can run on the 3/05. The LSI Series is also completely compatible with the earlier Alpha-16 and Naked Mini-16 series. Peripherals can attach to any LSI or the older 16 line, with the exception of discs. The disc interfacing is slightly different for the LSI line than for the older 16 line.

MAINTENANCE

Computer Automation sells only to OEM manufacturers, it does not provide the type of on-site preventive and emergency maintenance contracts usually associated with end users. The company does offer a 1-year warranty. Components that break down are immediately replaced or repaired free of charge during the first 30 days. After that, parts are repaired at the factory, while the user has access to "loaned" components (20 percent of purchase price) during the repair period.

TYPICAL PRICES

Model Number	Description	Purchase Price* $
	SYSTEMS	
30010-16/66	Standard DOS 20 (contains Jumbo Alpha LSI-2/20 computer with 16K words of 1,200-nsec core memory, power fail restart, Basic Variables, Teletype interface, real-time clock, EIA RS232 CRT interface, autoload & autoload ROM set options, ASR 33 Teletype, paper tape reader & punch with integral controllers, line printer, 4.92-million-byte disc subsystem, enclosure, & software)	29,975
30010-32/82	Expanded DOS 20 (plus 16K words of 1,200-nsec core memory & FORTRAN IV)	33,950
30012-32/82	Standard DOS 60 (same as 30010-16/66 with LSI-2/20 replaced by LSI-2/60 MEGABYTER)	35,550
	CENTRAL PROCESSOR AND WORKING STORAGE	
	NAKED MILLI	
10300-00	NAKED MILLI LSI-3/05 CPU on Half Card (includes 95 instructions, power/fail restart, vectored priority interrupts, & 16-bit DMA port)	295*
10300-01	Same as 10300-00 with Real-Time Clock & Autoload	395*
10370-38	Same as 10300-01 with 256 words of RAM Memory & Sockets for up to 8K Words of ROM	465*
10380-04	Same as 10300-01 with 4K Words of RAM Memory	725*
10390-52	Same as 10300-01 with 1K Words of RAM & 2K Words of Ultraviolet EPROM	1,575*
10390-62	Same as 10300-01 with 2K Words of RAM & 2K Words of EPROM	1,725*
10390-64	Same as 10300-01 with 2K Words of RAM & 4K Words of EPROM	2,750*
	Alpha LSI-3/05	
10373-38	Alpha LSI-3/05A (includes chassis for 3 half cards, 10-amp power supply w/o fans, operator's console, 10300-01 CPU, 256 words of RAM with sockets for up to 8K words of ROM)	825
10373-58	Same as 10373-38 Except with 1K Words of RAM	950
10383-04	Same as 10373-38 Except with 4K RAM-Only Memory	1,146
10393-62	Same as 10373-38 Except with 2K Words of RAM & 2K Words of EPROM	2,100
10393-64	Same as 10373-38 Except with 2K Words of RAM & 4K Words of EPROM	3,125
10375-38	Alpha LSI-3/05B (includes chassis for 5 half cards, fan, 15-amp power supply, operator's console, 10300-01 CPU, 256 words of RAM with sockets for up to 8K words of ROM)	975
10375-58	Same as 10375-38 Except with 1K Words of RAM	1,115
10385-04	Same as 10375-38 Except with 4K Words of RAM Memory	1,345
10395-62	Same as 10375-38 Except with 2K Words of RAM & 2K Words of EPROM	2,275
10395-64	Same as 10375-64 Except with 2K Words of RAM & 4K Words of EPROM	3,300
10376-38	Same as 10375-38 Except with Programmer's Console Instead of Operaotr's Console	1,190
10376-58	Same as 10376-38 Except with 1K Words of RAM	1,335

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price* $
10386-04	Same as 10385-04 Except with Programmer's Console instead of Operator's Console	1,575
10386-08	Same as 10386-04 Except with 8K Words of RAM	1,995
10396-62	Same as 10395-62 Except with 2K Words of RAM & 2K Words of EPROM & Programmer's Console	2,545
10396-54	Same as 10396-62 Except with 1K Words of RAM & 4K Words of EPROM	3,425
	Options	
13628-01	Autoload ROM	48
12635-01	Piggyback Teletype Interface	150
	Development Systems	
10368-16	Prototype Development System	4,095
10369-16	Program Development System	5,795
	NAKED MINI LSI-2/10 & 2/20	
	NAKED MINI LSI-2/10 & 2/20 CPU includes 188 instructions, multiple stack handling, hardware multiply/divide, memory scan & extensive byte capability, 5 vectored priority interrupts expandable to 256, 2 direct memory channels increased to 64; available in 5-unit quantities only)	
53586-00	NAKED MINI LSI-2/10 CPU on Full Card (power fail restart option)	1,500
10640-04	Same as 53586-00 Except with 4K Words 980-nsec Core Memory	1,750
10660-16	Same as 53586-00 Except with 16K Words of 1,200-nsec Core Memory	3,300
53506-00	NAKED MINI LSI-2/20 CPU on Full Card (power fail restart option)	1,900
10450-04	Same as 53506-00 with 4K Words of 980-nsec Core Memory	2,300
10460-16	Same as 53506-00 Except with 16K Words of 1,200-nsec Core Memory	3,875
	Alpha LSI-2/10 & 2/20	
	(Alpha LSI-2/10 & 2/20 configurations include a central processor, memory, chassis with power supply)	
10780-28	Alpha LSI-2/10 Except with 4K Words of RAM Memory & Operator's Console	1,975
10740-24	Same as 10780-28 Except 4K Words 980-nsec Core Memory	2,440
10741-28	Same as 10740-28 Except Jumbo Version	3,565
10760-36	Same as 10780-28 Except with 16K Words of 1,200-nsec Core Memory	3,990
10761-36	Same as 10761-36 Except Jumbo Version	4,245
10740-04	Same as 10740-24 Except with Processor's Console Instead of Operator's Console	2,540
10741-08	Same as 10740-28 Except with Programmer's Console Instead of Operator's Console	3,665
10550-24	Same as 10740-24 Except for Alpha LSI-2/20 Instead of 2/10	2,765
10551-28	Same as 10741-28 Except for Alpha LSI-2/20 Instead of 2/10	3,915
10550-04	Same as 10550-24 Except Programmer's Console Instead of Operator's Console	2,765
10551-08	Same as 10551-28 Except Programmer's Console Instead of Operator's Console	4,015
	LSI-2 CPU Options	
12500-00	Power Fail Restart	250
12500-01	Automatic Startup	150
12505-39	Option Pack (includes Basic Variables, Teletype interface, real-time clock, and autoload)	485
12505-55	Option Pack (same as 12505-39 except with EIA RS232 CRT interface)	560
13505-01	Autoload ROM	60
13505-02	Same as 13505-01 Except with Loaders for Floppy Disc Controller or Peripheral Subsystem Plus Microdiagnostic Program	145
13505-03	Autoload ROM	145
	MEGABYTERS	
10951-08	MEGABYTER (includes 8K words of core 980-nsec memory, jumbo chassis, power supply, programmer's console, power fail restart, Basic Variables, Teletype & EIA CRT interface, real-time clock, autoload, & autoload ROM set)	6,850
10961-16	Same as 10951-08 (with 16K words of 1,200-nsec core memory)	7,900
10951-16	Same as 10961-16 Except Contains 2 Interleaved 8K-Word Core Memory Modules	8,765
	Memories	
11650-38	256 Words of RAM Memory & Sockets for 8K Words of ROM	290
11650-58	1K Words of RAM Memory & Sockets for 8K Words of ROM	400
11642-04	4K Words RAM Memory	550
11530-52	1K Words of RAM & 2K Words of EPROM	1,425
11530-64	2K Words of RAM & 4K Words of EPROM	2,600
11550-08	8K Words of 980-nsec Core Memory	1,950
11560-16	16K Words of 1,200-nsec Core	3,050
	Memory Options	
12090-40/20	On-Card Battery Backup	95
12545-00	Memory Bank Control	900
30100-01/02	EPROM Programmer	2,950
	MASS STORAGE	
22566-00	Dual Floppy Disc Drives	3,700
22530-00	Moving-Head Disc Drive	10,200
18566-XO	Dual Floppy Disc Subsystem	12,300
	Input/Output	
22224-15	Magnetic Tape Transport	6,300
18224-15	Magnetic Tape Subsystem	8,275
22205-00	Modified ASR 33 with 16-Ft Cable	1,695
22230-00	Keyboard/Display Terminal	3,175
22077-20	Card Reader (285 cpm)	4,425
22107-06	Line Printer (120 cps; 60-150 lpm; 80 col)	4,950
22223-11	Paper Tape Reader (300 cps)	1,945
22223-60	Paper Tape Reader/Punch	5,625
14223-00	Paper Tape Peripheral Controller	600
14224-00	Magnetic Tape Controller	2,400
14566-01	Floppy Disc Controller	930
14629-04	I/O Distributor (for 1-4 parallel intelligent cables)	380
14629-14	I/O Distributor (for 1-4 serial or parallel intelligent cables, any mix)	445
14629-18	I/O Distributor (1-8 serial or parallel intelligent cables, any mix)	530
14631-11/01/ 02/03/04	Intelligent Cables	145
19001-00	Advanced BASIC	300
19001-10	Extended BASIC	400
19001-20	Extended Multiple User BASIC	500
20570-00	FORTRAN IV	1,700
19005-02/03	Real-time Executive for LSI-2 or LSI-3	500
19005-05	Real-time Executive for both LSI-2 & 3	750
19007-00	Operating System	2,000

*Available only in minimum order quantities of 5 units
*CAI systems are sold OEM, thus maintenance to the end-user is not on typical contract basis. See MAINTENANCE section

COMPUTER AUTOMATION LSI SERIES

REPORT UPDATE

Alpha LSI-3/05

Alpha LSI-3/05 minicomputers are now available in three series configurations designed to allow the user to move up through the Computer Automation product line. They are well-suited for control applications where system requirements are expected to expand. Typical LSI-3/05 configurations are as follows:

Series A — Naked Milli CPU, 10-Amp power supply, 3-slot chassis and an operator's console.

Series B — Naked Milli CPU, 15-Amp power supply, 5-slot chassis and operator's console.

Series C — Naked Milli CPU, 15-Amp power supply, 5-slot chassis and programmer's console.

With 256 words of semiconductor random access memory (RAM) and sockets to accommodate up to 8K words or with Read Only Memory (ROM), the lowest priced Series A model is $701; lowest priced Series B Model $829; and Series C lowest priced model is $1,012. Other configurations are available, some with standard chassis and up to 32K words of memory.

SOFTWARE MACHINES

Five disc operating systems used in conjunction with Computer Automation's Naked Mini computer have been introduced for the OEM market. Dubbed the Software Machines, the systems are designed to replace the company's previous disc operating products and to allow command inputs from a keyboard or from job files containing job control language statements. Discs can be loaded with a string of jobs that can be executed without operator attendance. Basically, the new configurations replace paper tape as the system I/O device with floppy disc. For the two smallest configurations, floppy discs also provide bulk storage for the system.

Each machine includes an Alpha LSI-2 minicomputer, core memory 16K or 32K words, dual floppy disc subsystem, ASR-33 TTY and operating system package with executive, Input/Output control system, disc file manager, assembler and macro assembler. Character-oriented text editing, line-oriented source program editing, linking/editing of object programs, alphabetizing/listing cross references of program symbols and other program debug and maintenance functions are supported.

The floppy disc operating system includes basic variables, TTY interface, autoload, real-time clock, power fail restart, and EIA RS-232 interface options as standard elements.

The following five models are currently available:

Standard DOS 10 — Alpha LSI-2/10, 16K words of core memory, dual floppy disc subsystem, TTY ASR 33;

Expanded DOS 10 — Alpha LSI-2/10, 32K words of core, line printer, dual floppy disc subsystem, TTY ASR 33, and FORTRAN IV package that supports ANSI FORTRAN X3.9 1966 language;

Standard DOS 20 — Alpha LSI-2/20, 16K words of core, line printer, cartridge disc system, dual floppy disc subsystem, and TTY ASR 33;

Expanded DOS 20 — Alpha LSI-2/20, 32K words of core memory, line printer, cartridge disc system, dual floppy disc subsystem, TTY ASR 33 and FORTRAN IV package;

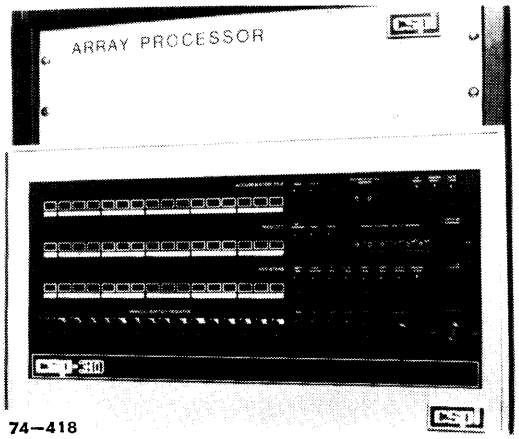
Standard DOS 60 — Alpha LSI-2/60, 32K words of core memory, line printer, cartridge disc system, dual floppy disc subsystem, TTY ASR 33, and FORTRAN IV package.

Deliveries are scheduled 30 days after the order is received.

PRICE DATA

Purchase prices for the basic models are as follows:

Standard DOS 10	$13,975
Expanded DOS 10	$23,975
Standard DOS 20	$29,975
Expanded DOS 20	$33,950
Standard DOS 60	$35,550



74—418

OVERVIEW

The Computer Signal Processors CSP-30 and CSP-125 are high-speed signal processing systems suitable for vibration analysis speech research, noise analysis, radar, sonar, and similar real-time signal detection and process control applications that require a fast Fourier Transform processor. The 16-bit computers can act either as stand-alone systems with their own peripheral subsystems, or as slave units to another computer. In either case, installations are usually highly customized, both as to hardware interfacing and software support.

Important elements of both systems are the 4001 and 4500 Array Processors, stand-alone peripheral processors that provide high-speed Fourier Transforms on data arrays. The console can be a Teletype or a CRT-keyboard, and additional peripherals include paper tape equipment, disc storage units, magnetic tape equipment, cartridge tape equipment, line printers, plotters, displays, analog/digital subsystems, and special interfaces. Memory size on the CSP-30 can range from 512 to 2,048 words of bipolar read/write memory and 4K to 128K words of core, while the CSP-125 can have from 1K to 32K words of bipolar memory and up to 128K words of core memory.

Both computers are extremely fast machines — in fact, the CSP-30 is the fastest on the market. Both use a memory interleaving technique to optimize memory access, and both can overlap (half cycle) memory accesses; this combination yields very fast access rates to core memory. The CSP-30 uses up to 2,048 words of bipolar memory with a 100-nanosecond cycle time (the same cycle time as the processor itself) and up to 128K words of core memory with 900-nanosecond cycle time. The CSP-125 has a slower cycle time, 125 nanoseconds, to handle a larger amount of bipolar memory — up to 32K words as well as up to 128K words of core memory. Other features increase processing speed — both memories can operate simultaneously and asynchronously, and memory can be optionally multiported and shared. Processor options, in addition to the 4001 and 4500 Array Transform Processors and memory multiporting, include hardware floating point and DMA (2 speeds). The 32 accumulators, hardware multiply/divide, power fail/restart, bootstrap ROM, eight levels of priority interrupt and four I/O channels are standard. The priority interrupt system can be expanded to 56 levels, and I/O channels can be added to accommodate 40 devices (including eight DMA devices).

The standard instruction set consists of 212 singleword instructions, 79 doubleword instructions, and 7 group instructions. Both indexed and multilevel indirect addressing are permitted; indexing and each indirect addressing level adds 100 nanoseconds on the CSP-30 and 125 nanoseconds on the CSP-125. Table 1 summarizes system specifications and lists some sample instruction execution times.

Software for both systems is identical. It includes an extended version of ANSI FORTRAN IV, two symbolic assemblers, tape and text editing programs, debugger, loaders, signal processing library, I/O drivers, and hardware diagnostics. One assembler operates in a stand-alone system, the other is a cross-assembler written in FORTRAN, designed to run on the main computer of a "slave" system. The FORTRAN IV package offers extensions, such as fixed-point data mode, unspecified data mode, implicit type declaration, mixed-mode arithmetic, literal constant and format conversion, special intrinsic functions, conditional compilation, multiple statements on a line, multiple replacement statements, comments attached to statements, source statement segmentation, array initialization, nonstandard returns from subroutines, set statement, free-field input, object code optimization and in-line assembly language.

The Signal Processing Library includes a large number of programs. Fast Fourier Transform programs include Radix-4 FFT, Radix 3 FFT Step, FFT related functions (auto/cross spectrum, convolution/correlation, cepstrum), Zoom FFT, complex multiply, complex magnitude squared, and complex magnitude. Also included are cosine/sine table interpolation, log of the complex magnitude, Base-2 Log, complex exponential generator, recursive filter, Integrate and dump filter, histogram, direct correlation, direct convolution, Hanning weighting predictive coding, and 1/3 octave filtering.

PERFORMANCE AND COMPETITIVE ANALYSIS

Computers like the CSP-30 and CSP-125 compete for what is now a limited market, limited partly by the cost of these customized high-speed systems. Computer Signal Processors sees only two real competitors in this market: Hewlett-Packard, which has a fairly slow signal processing system; and Time Data, which has a system intermediate in speed between the Hewlett-Packard and the Computer Signal Processing systems. Both companies are larger than CSPI, but neither has a system that operates at CSPI's speed. Users with high-speed

Table 1. CSP-30 and CSP-125: Specifications

SYSTEM	CSP-30	CSP-125
CENTRAL PROCESSOR		
No. of General-Purpose Registers	32 (14 index)	32 (14 index)
Addressing		
Direct (no. of wds)	255 or 1,023	255 or 1,023
Indexed (no. of wds)	32K	32K
Indirect (no. of wds)	32K (multi-level)	32K (multi-level)
Paging (no. of wds)	128K	128K
Instruction Set		
Priority Interrupt Levels	8-56	8-57
Interrupt Time (μsec)	0.6	0.75
MAIN STORAGE		
Word Size (bits)	16	16
Bipolar Memory		
Cycle Time (μsec)	0.100	0.125
Capacity (min-max wds)	512-2,048	4,096-32,768
Increment Sizes (wds)	256	4,096
Core Memory		
Cycle Time (μsec)	0.900	0.900
Capacity (min-max wds)	4K-128K	4K-128K
Increment Sizes (wds)	4K, 8K	4K, 8K
Parity	No	No
Protect	No	No
INPUT/OUTPUT		
No. of Programmed I/O Channels	4-32	4-32
No. of DMA Channels	0-8	0-8
Max DMA Transfer Rate (wds/sec)	1.4M or 3.3M (core); 10M (bipolar)	1.4M or 3.3M (core); 10M (bipolar)
INSTRUCTION TIMES (μsec)		
Add/Subtract	0.200	0.250
Multiply/Divide	1.000	1.250
Indirect/Indexed Addressing	0.100	0.125

requirements would gravitate toward CSPI, while users with lower-speed requirements would have to evaluate price/performance and the software capabilities of the three companies. Many such users would find slave configurations or perhaps the addition of just the 4000 series array processors (which are actively marketed as separately purchased subsystems that can be interfaced to many minis besides the CSP processors) to their own computers an adequate solution to their signal processing needs.

Computer Signal Processors has around 30 installations of the CSP-30 and CSP-125 systems, counting both slave and stand-alone configurations, with the CSP-30 system accounting for most of them. The first CSP-30 system was installed in May 1970, while the first CSP-125 was installed around June 1973. About 60 percent of these are government installations and 40 percent are in industry. Each installation is highly customized — no two are alike. The company, which was founded in 1968, was organized expressly to develop and manufacture digital signal processing systems. Manufacturers in the computer and aerospace industries, universities, laboratories, and several government agencies are numbered among their customers.

USER REACTIONS

In many cases, it was difficult to obtain user reactions because many research organizations using the CSPI systems were in some way connected with the United States government, even when they were private industrial concerns. A Canadian systems house, for instance, was using the system for a project for the United States government, and was not free to divulge what the system was being used for. They had been directed to buy the system by the United States government and had no idea what alternatives were considered. All they could say was that they were doing signal processing and they were responsible for their own software and maintenance.

A spokesman at one of the United States Air Force bases, however, was more at liberty to discuss the application, research on sound synthesis techniques and their applications to digital, narrowband voice communications. The system performed real-time voice processing using linear prediction methods of speech analysis. The system was chosen last year after a literature search that ruled out most available minis because of speed and most large computer systems because of cost. The real-time capability of the system was also one of its attractions. The CSP-125 was chosen over the CSP-30 because the slower 125-nanosecond system was more cost-effective, particularly with regard to memory. The hardware, which included 32K words of core, 8K words of bipolar memory and a 9-megabyte disc, was installed quickly and proved to be reliable, but this user had trouble debugging the coded software. This user now has a very successful Disc Operating System, as well as special-purpose applications software.

CONFIGURATION GUIDE

A basic CSP-30 stand-alone system consists of the CPU, 4,096 16-bit words of core memory and 512 16-bit words of integrated circuit (IC) memory, eight priority interrupt levels, a dual-deck magnetic tape, four fast I/O channels, an 8-device party-line controller, wired autoload, a control panel, and a power supply. A Teletype KSR 35 configures with the basic central processor to achieve a minimum system that sells for $77,850.

The basic CPU chassis can include up to 8 DMA channels, I/O expansion up to 32 channels, up to four core memory modules (4K or 8K words each), up to eight bipolar memory modules (256 words each), and up to 56 priority interrupt levels. Additional memory, up to 96K words, requires additional chassis (32K words each),

which can be multiported to allow access to several computers or to allow simultaneous operation of different memory modules.

The CSP-125 is identical to the CSP-30 in every respect except that the basic bipolar memory consists of 4,096 words expandable to 32,678 words in 4K-word increments, with bipolar and processor memory cycle time slowed to 125 nanoseconds to accommodate the increased capacity.

Input/Output

Four input/output data paths are supplied on the CSP-30 and CSP-125, one for each channel. Channel A, available on the basic system, is internally assigned as a party line, which can connect to eight peripheral devices to the central processor via peripheral device controllers. The remaining three channels (B, C, and D) can be connected to additional party line controllers or to high-speed devices. Although programming techniques determine data transfer rates, the maximum transfer rate on the party line is 500,000 16-bit words per second on the CSP-30 and 380,000 on the CSP-125.

In addition to the four input/output channels, provisions are made for up to eight optional direct memory access (DMA) ports, to allow data transfers directly between magnetic core memory and device controllers on an interleaved cycle-stealing basis, at transfer rates over 1,000,000 words per second. The DMA has dual-port capability, that is, one can be interfaced with each type of core storage (magnetic and integrated). The maximum transfer rate over a DMA channel connected to bipolar memory is 10,000,000 16-bit words per second on the CSP-30 and 7,500,000 16-bit words on the CSP-125.

Low-Speed Peripherals

- Teletypes. ASR and KSR 33/35; 10 cps.
- Data Terminal. Keyboard printer; 10, 15, or 30 cps.
- CRT Terminal. 24 lines, 80 char/line, 1,920 char total; 60 frames/sec refresh; 110-9,600 baud, 5 switch-selectable speeds; graphics option with 11,520-element resolution, 72 x 160 dot matrix.
- Paper Tape Reader. 300 cps; 5- to 8-level tape, EIA interface.
- Printers. 356-1,100 lpm; 64-char set; 80 or 132 cols.
- Printers-Plotters. 500 or 600 lpm; 7 x 9 and 5 x 7 dot matrix; 1.25 or 1.6 ips paper speed; 120 scans/sec plotting.
- Plotters. x-y plotter; 300 increments/sec; 0.1 to 0.25 mm increments; 8.5 x 11-in. or 11 x 17-in. paper; x-y recorder with 30 ips slew, local and remote pen lift.
- Graphic Displays. 8.5 x 11-in. displays; 13K or 40K points/sec; x and y 10-bit D/AS.

Mass Storage Peripherals

- Discs. Fixed-head disc with 128, 256, 512, or 1,024 tracks; 512K, 1M, 2M, and 4M-byte capacity; 8.5-msec avg access time; fixed-head disc with 16, 32, 64, or 128 tracks, 128K, 256K, 512K, or 1M-byte capacity, 16.7-msec avg access time.
- Magnetic Tape. 9-track, 800 bpi, 75 to 125 ips; controller handles up to 4 compatible slave drives; cartridge tape unit, 2 or 4 drives with integral controller, 900 bpi, 1,800 char/second, 300K-char cartridge.

Special Subsystems

- Analog/Digital. 100 MHz sampling, 16-256 single-ended inputs, 8-128 differential, 13-bit ADC; real-time 12-bit, 10-bit, or 14-bit system with variable sampling rates up to 250 KHz; high-speed 9-bit system with 1 MHz sampling; ultra high-speed 8-bit system with 2 MHz sampling.
- Array Processors. 4001 stand-alone for CSP-30, CSP-125, PDP-145, Data General Nova or Varian V73; 1,024 complex FFT in 5.0 msec, FFT, IFFT, complex multiply magnitude/phase, conversion, Hanning weighting; 4500 model same as 4001 but slower speed.
- Interfaces. XDS Sigma S Interface; Sigma Interface; XDS Sigma 7908 Interface; Dual Register Interface for PDP-11; Universal I/O Buffer for customer serial or parallel I/O.

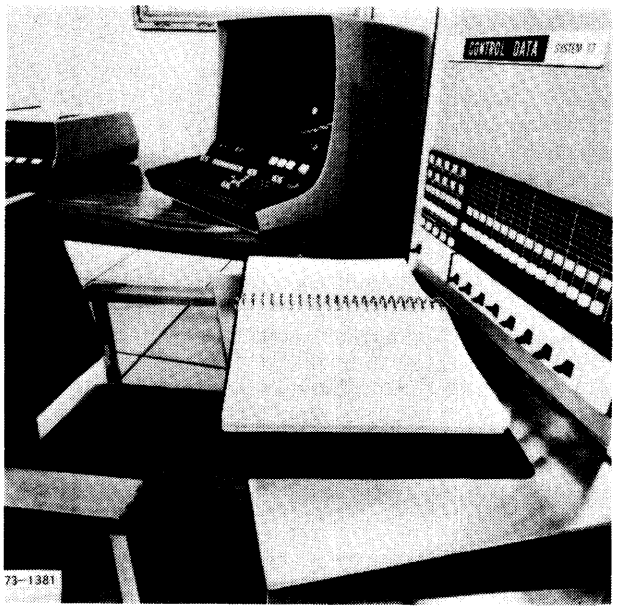
HEADQUARTERS

Computer Signal Processors, Inc.
209 Middlesex Turnpike
Burlington MA 01803

Model Number	Description	Purchase $
	Processor	
3001	Basic CSP-30 Includes 100 nsec CPU w/Hardware Multiply & Divide Memory Capability up to 128K of Core Memory and 2K of IC Memory 1.0-μsec Multiply for 16 x 16 Bits 32 Accumulators Power Failure Restart 4 I/O Channels (1 supplied with an 8-device party line controller) Autoload Capability (automatic bootstrap) 8 Levels of Priority Interrupt	35,000
3010	CSP-125 Includes 125 nsec CPU w/Hardware Multiply & Divide Memory Capability up to 32K of IC Memory 1.25-μsec Multiply for 16 x 16 Bits Otherwise Identical to CSP-30 Model 3001	38,000
	Processor Options	
3046	Direct Memory Access Controller	3,500
3050	Party Line Controller	1,500
3061	Priority Interrupt Controller	2,000
3011	Sample Rate Counter	1,500
	Processor Memory	
3216	Core Memory Module 8K	4,500
3217	Core Memory Module 4K	3,200
3226	IC Memory Module (256 words)	1,500
3125	CSP-125 IC Memory Module (4,096 words)	8,000
3221	Multiport or Extended Core Memory Bank	1,500
3222	Multiport Switch Module	1,500
3223	Multiport Control Module	1,500
3225	IC Memory Output Interface	1,500
	Discs	
2310	Disc Storage Unit and Controller (9.6/19.2-megabit capability)	17,800/ 21,500
2322	Disc Storage Unit and Controller (9.6/19.2-megabit capability)	24,500/ 28,800
	Buffers and Interfaces	
1020	Universal Input/Output Buffer	3,000
1050	Xerox Data Systems Sigma 5 or Sigma 7 Interface	20,000
1055	Xerox Data Systems Sigma Series Interface with Sigma Adapter	
	Basic	6,500
	Tester	2,500
	Cable Set	4,500
1060	Array Processor Interface (determined by computer used)	
1065	CSP-30 Dual Register Interface	4,500
	Teletypes and CRT Terminals	
2010	TTY ASR-33 Keyboard Printer and Controller (with paper tape reader and punch; 10 cps)	2,300
2020	TTY KSR-35 Keyboard Printer and Controller (10 cps)	3,500
2030	Data Terminal and Controller	3,000
2040	TTY ASR-35 Keyboard Printer and Controller (with paper tape reader and punch; 10 cps)	6,600
2050	CRT Terminal and Controller	3,000
2060	CRT Terminal and Controller with Graphics Option	5,400
2610	CRT Display and Controller	7,600
2620	CRT Display Unit and Controller	1,600
2615	CRT Storage Display and Controller	8,750
2630	CRT Graphics Display with Terminal and Controller	39,500 & up
	Paper Tape Equipment	
2130	High-Speed Paper Tape Reader and Controller	3,000
	Magnetic Tape Equipment	
2420	Digital Magnetic Tape Unit and Controller/74-125	15,500
2425	Slave Magnetic Tape Unit (all features same as 2420)	
2430	Digital Magnetic Tape Unit and Controller/10-45 (9-tracks, 0.6-in. interrecord gap; std recording format)	13,000
2435	Slave Magnetic Tape Unit (all features same as Model 2430)	
2449	Cartridge Tape Unit and Controller/Two (w/system)	5,500
	Later Add-on	6,900
2450	Cartridge Tape Unit and Controller/Four (w/system)	7,500
	Later Add-on	8,900
	Line Printers, Plotters, and Displays	
2520	Line Printer, Controller, and Buffer (80-col format)	12,000
2530	Line Printer, Controller, and Buffer (132-col format)	18,000
2540	Matrix Printer/Plotter and Controller (80 char/line)	12,900
2550	Matrix Printer/Plotter and Controller (132 char/line)	14,500
2605	X-Y Incremental Plotter and Controller	7,500
2607	X-Y Recorder	3,000
	A/D and D/A Converters/Filters	
1070	Analog to Digital Converter w/Multiplexor and Controller	4,500 & 500/8 ch
1040	RTIOCS -- Real-Time Input/Output Conversion System	6,500
1180	Aliasing Filter	2,600
1185	Variable Electronic Aliasing Filter	NA
1187	Variable Electronic Aliasing Filter	NA
1009	High-Speed Analog to Digital Converter/Controller (9-bit encoding)	7,500
1030	Ultra High-Speed Analog to Digital Converter/Controller (8-bit encoding)	11,000
	Accessories	
3092	Power Supply Expansion	400
3085	Maintenance Panel w/System	2,500
	Later Add-on	3,000
3086	Expansion Cabinet	1,200
3088	Console Cabinet	2,500
3089	Front Panel for Cabinet	300
	Software	
5010	Signal Processing Library	3,500
5030	FORTRAN Compiler	5,000
5040	Software Floating-Point Package	--
5050	Software for Plotter Output	500

CONTROL DATA CORP.

System 17 System Report



OVERVIEW

The CDC System 17 is a 16-bit minicomputer aimed at both OEM and end-user markets, particularly for industrial applications. The system and its predecessor, the CDC 1700, have been used in industrial control, data acquisition, hospital/medical, optical character recognition, graphics, communications, amusement and recreation, data entry, and supervisory control applications. Its primary orientation as a system is toward industry, however; CDC has sold large orders of these minicomputers to automobile manufacturers.

System 17 borrows much of its architecture and its software from the CDC 1700, but improves on the 1700 by offering lower cost peripherals. The I/O interfacing is somewhat different for the new peripherals, but optional channel adapters can be added to interface 1700 peripherals to System 17 (the 1500 analog/digital subsystem, for instance). Because the two systems are program compatible, the vast library of software developed for the 1700 is available to the System 17. Thus, three factors — cheaper peripherals, large tested software base, and the interface to the vast 1500 subsystem — make System 17 a strong contender in the minicomputer market.

Although System 17 has not embraced the microprogramming concept, it has made use of other popular new developments in minicomputer technology. The new processor uses MOS/LSI semiconductor memory, and thus offers a better price/performance ratio than the 1700.

System 17 is particularly attractive to end users. The policy of offering user-oriented, hardware/software applications packages for all CDC computers has been company-wide for a number of years.

Table 1 lists the mainframe characteristics.

PERFORMANCE AND COMPETITIVE POSITION

The System 17 places CDC in the best position it has been in for several years in the minicomputer market. Although CDC early recognized the need for real-time small computers and produced the 1700 line for that market, the company didn't follow up by developing minicomputer peripherals for the 1700 line. CDC interfaced a broad range of peripherals to the 1700, but they were generally the same peripherals CDC offered with its large computers and they were expensive. As minicomputer processor prices fell, it became apparent that minicomputers needed their own low-cost peripherals. Thus, the cost of peripherals for most minicomputer systems has dropped markedly in the past few years.

With the System 17, CDC introduced both an excellent, lower-cost processor and minicomputer-sized peripherals: magnetic tape, cartridge disc, printers, conversational display, card reader, and so on. System 17 retains the really fine logic designed into the 1700 line, and it can run all the 1700 software developed over the last eight years. In addition, CDC has many years of experience in real-time processing and has an impressive number of systems operating for varied applications.

One of the competitive advantages of System 17 is its interface to the 1500 analog/digital subsystem, which has a tremendous variety of components of all types, ranges, and speeds. The 1500 originally was designed for the 1700 system but continues to be expanded as a System 17 peripheral as well. One recent addition is the 1590 remote interface, which allows the 1500 to be located at a site remote from the System 17. This is an important addition to the product line; at the time of this writing, only MODCOMP and Digital Equipment had similar offerings.

HEADQUARTERS

Control Data Corp.
P O Box 0
Minneapolis MN 55440
(612) 853-8100

Table 1. CDC System 17: Mainframe Characteristics

Feature/Characteristic	
Central Processor	1784-1, 1784-2
Microprogramming	No
Control Memory	None
No. of Internal Registers	2 accumulators; 2 index
Addressing	
Direct (no. of words)	256
Indirect	Yes
Indexed	Yes
Instruction Set	Hardware/subroutine
Number	196
Decimal Arithmetic	No
Floating-Point Arithmetic	Subroutine (std); hardware (opt)
User-Microprogramming	No
Priority Interrupt System Levels	16
Main Storage	
Type	MOS/LSI
Cycle Time (μsec)	0.900 (1784-1); 0.600 (1784-2)
Basic Addressable Unit	1 word
Bytes/Access	2
Cache Memory	None
Min Capacity (bytes)	8,192 (std)
Increment Size (bytes)	8,192
Error Checks	Parity
Protection Method	Manual switches
ROM	No
Input/Output	
Programmed I/O	Yes (called AQ)
DMA Channels	Yes (called DSA) 1 std; 1 opt
Multiplexed I/O	No
Multiprocessing Adapters	Coupling data channel; also satellite coupler for CDC 3000 or 6000 systems
Max. Transfer Rate	
Within Memory (wds/sec)	278K (1784-1); 417K (1784-2)
Over DMA (DSA) (wds/sec)	1.1M (1784-1); 1.6M (1784-2)

The System 17 competes with the Digital PDP-11/40 and /45, the Data General Nova ECLIPSE line, the Hewlett-Packard 21MX Series, and Honeywell System 700. System 17 can be a strong competitor if CDC takes its own claims seriously and does offer users service rather than hardware. Real-time systems tend to require tailoring to fit a specific application, and the strong competitors in this market must be prepared to perform applications engineering and programming for users. A large market exists for minicomputers like the System 17, and CDC should be able to produce a number of hardware/software System 17 applications packages that will do well.

USER REACTIONS

Users contacted had previous experience with CDC systems, notably the 1700 Series. For them, the step to the 17 was a logical, orderly one; nevertheless, they first considered alternatives from other manufacturers.

Manufacturing

A manufacturer of chemicals and drugs obtained one of the first System 17s to use as a front end for its CDC 6400, with terminals connected to several real-time lab operations. This manufacturer already had a number of CDC 1700s in use in various capacities for process control. A competitive system closely examined was the DEC PDP-11. The System 17 was chosen because it had more software immediately useful to their purpose and it could be used to compile programs for the 1700s they already had. This manufacturer is now considering adding more System 17s for control applications.

The current front-end configuration includes a 1700 channel adapter, two tapes, two discs, CRT terminal, dot matrix printer, and 32K words of memory. The disc drives installed are 854 models; but this user is looking forward to CDC's new line of cartridge discs which use an electronic seek mechanism that is more reliable than current electromechanical ones.

This user found no problems with program compatibility between the 1700 and System 17. As for maintenance, the 1700s have been quite reliable, and he expects the System 17 to be even easier to maintain. This user stressed the excellence of the 1700 operating system, which is also used on the System 17. He noted that CDC has one of the largest software libraries for minicomputers.

Medical Systems

A medical systems house produces packages for admissions screening, intensive care, coronary care, operating room functions, and the like. About five years ago, this company selected the 1700 as the basis for its medical hardware/software packages because it was one of the few proven systems with nationwide maintenance. Also, CDC had a good FORTRAN package to make programming easier.

Experience with the 1700 has borne out expectations. The evolution to the System 17 is a natural step because of the complete software compatibility, lower cost, and greater reliability of the new system.

CONFIGURATION GUIDE

A basic System 17 includes a processor (either 1784-1 or 1784-2) and 4K words of MOS/LSI semiconductor memory. Both processor submodels include 16 interrupts, two index registers, DSA, parity, memory protect, and hardware multiply/divide as standard features. The difference between the two models is in the memory cycle time: 900 nanoseconds for the 1784-1 and 600 nanoseconds for the 1784-2.

Two enclosures are available. The first is required and houses the CPU, 32K words of memory, the DSA and AQ channel, a memory hold battery (providing power for eight hours in case of main power failure), and AQ/DSA expansion. Each 4K-word memory module is mounted on one circuit board. Up to 36 circuit boards, plus power supply and cooling equipment, are also housed in the CPU enclosure. Optional features are integral controllers for magnetic tape transport, cartridge disc unit, line printer, card

reader, card punch, paper tape reader, teletypewriter, and conversational display terminal. See Table 2 for specifications.

The second enclosure is required to add memory beyond 32K words. Full memory expansion to 64K words also requires a memory expansion module (1786-1).

Up to eight peripherals can connect to the DSA and AQ I/O channels. The 1785 channel expansion adapter is available in four models to expand the channel capacity.

- 1785-1 expands the AQ channel to handle up to eight additional devices.
- 1785-2 expands the DSA channel to handle up to eight additional devices.
- 1785-3 converts the AQ channel to the standard 1700 bus so the CDC 1700 programmed I/O devices can be connected to System 17.
- 1785-4 converts the DSA channel to the standard 1700 I/O bus so the CDC 1700 DSA devices can be connected to the System 17.

The System 17 can support all the peripherals designed specifically for it as well as peripherals available with the CDC 1700 line, like the massive 1500 analog/digital subsystem. Furthermore, a new controller allows connection of a remote 1500 subsystem over communication lines.

Table 2. CDC System 17: Peripherals

Device	Performance Characteristics
Discs	
856-2	1 fixed, 1 removable cartridge disc, 1.1M wds/disc, 4 drives/controller
856-4	Like 856-2, but 2.2M wds/disc
Magnetic Tape	
615-73	7-track, 556 or 800 bpi
615-93	9-track, 800 NRZI or 1,600 PE bpi
616-72	7-track, 556/800 bpi, 25 ips
616-92	9-track, 800 bpi, 25 ips
616-95	9-track, 800 bpi, 50 ips
Punched Card	
1725-1	100-cpm reader
1729-3	300-cpm reader
415	250-cpm punch
Paper Tape	
4021/4022	FACIT readers, 300 cps
4070 Series	FACIT punches, 75 cps
Terminals	
1711	33/35 KSR TTY, 10 cps
1713	33/35 ASR TTY, 10 cps
713-10	640- or 1,280-char CRT
274	Digigraphic console (a 1700 peripheral)
Printers	
1742-30	300 lpm
1742-120	1,200 lpm
713-120	30 cps
Analog/Digital	
1500	A/D, D/A subsystem; extensive subsystem with up to 15 "sub-subsystems" for low-level and high-level A/D, D/A, and digital control
1590-3	Remote interface for up to 100 D/A, A/D devices from Model 1500 subsystem
Communications	
1743-1	For 1 or 2 sync lines, to 19,200 baud
1743-2	For 8 async lines, to 9,600 baud
1718	CDC 3000/6000 interface
1716	Multiprocessor coupler
Other	
10336	Real-time clock

Table 3. CDC System 17: Software Systems

Characteristic	4K Assembly System	Utility System	Mass Storage Operating System
Assembler	Assembler	Assembler or Macro Assembler	Macro Assembler
Compiler	None	Tape FORTRAN	Mass Storage FORTRAN
Mass Storage Required	No	No	Yes
Minimum Configuration Required	4,096 wds	8,192 wds*	12,288 wds*
Core Storage Occupied by Resident Portion	750 wds	2,250 wds	8,673 wds (largest overlay)
Execute Batch Programs	Yes	Yes	Yes
Execute Control Programs	No	No	Yes
Multiprogramming	No	No	Yes
Program Library	No	Yes	Yes

Note:
*If the FORTRAN compiler is used, additional 4K words of core storage are required.

In addition, intercomputer couplers are available to interface it to the CDC 3000, CDC 6000, and Cyber 70 Series computers, or to link two System 17s together with a shared disc data base.

The System 17 is very modular, and CDC offers dozens of application-oriented configurations. Many of these are partially dependent on software requirements. Software packages and their requirements are listed in Table 3.

COMPATIBILITY

The System 17 is program compatible with the CDC 1704, 1714, and 1774. An intercomputer adapter allows the System 17 to operate as a front end for the CDC 3000, CDC 6000, and Cyber 70 Series computers; to communicate with CDC 1700 systems; and to use the CDC 1700 peripherals. In addition, hybrid A/D configurations incorporate an EAI 680 analog computer as a system component.

MAINTENANCE AND SUPPORT

CDC provides 24-hour service centers in 42 metropolitan areas in the United States. Preventive maintenance is provided during the primary maintenance period.

CDC provides training and education for customers at its education institutes. Other services include site planning, systems analysis, and consulting. FOCUS, the international Forum of Control Data Users formed in 1968, gives users opportunities to exchange ideas among themselves and CDC personnel. A special interest group has been formed for CDC 1700 users. A newsletter is published monthly to distribute information.

TYPICAL PRICES

Model Number	Description	Monthly Rental $ 1-Yr	Monthly Rental $ 2/3-Yr	Purchase Price $	Monthly Maint $
	CENTRAL PROCESSORS AND WORKING STORAGE				
1784-1	Processor with 4K words of 18-bit MOS memory, 900 nsec	347	258	14,175	100
1784-2	Processor (same as 1784-1 except 600-nsec memory cycle time)	373	364	17,325	121
	Systems Options				
1785-1	AQ Channel Expansion	27	26	1,050	11
1785-2	DSA Channel Expansion	27	26	1,050	11
1785-3	1700 AQ Channel Adapter*	69	67	2,625	16
1785-4	1700 DSA Channel Adapter*	42	41	1,575	16
	Memory				
1782-1	Memory Module (900 nsec, 4,096 wds)	84	82	3,150	31
1782-2	Memory Module (600 nsec, 4,096 wds)	90	88	4,200	36
	MASS STORAGE				
	Cartridge Disc				
856-2	Cartridge Disc Drive (1.1M wds on fixed, 1.1M wds on removable discs)	200	195	9,450	57
856-4	Cartridge Disc Drive (same as 856-2 except has 2.2M wds/disc)	315	307	13,125	67
1733-2	Cartridge Disc Controller (single DMA channel connection; absolute cylinder addressing; daisy chain capability; controls up to 4 856-2 or 856-4 drives)	174	168	5,775	31
	INPUT/OUTPUT				
	Magnetic Tape				
615-73	Magnetic Tape Transport (7-track, NRZI; 556 or 800 bpi)	174	168	5,775	68
615-93	Magnetic Tape Transport (9-track, PE with 1,600 bpi or NRZI with 800 bpi)	189	184	7,350	79
	Punched Card				
1729-3	Card Reader and Controller (300 cpm)	179	171	6,300	78
	Line Printer				
1742-30	Line Printer and Controller (300 lpm; 64-char set)	389	378	17,850	200
1742-120	Line Printer and Controller (1,200 lpm; 48-char set)	1,533	1,495	52,500	300
	Terminals				
	TTY				
1711-4	33 KSR	37	36	1,470	32
1711-5	35 KSR	74	72	3,150	39
1713-4	33 ASR	48	47	1,680	36
1713-5	35 ASR	116	111	5,040	97
	CRT				
713-10	CRT Console	63	62	2,095	13
711-100	CRT Expanded Memory	11	—	336	11
1781	Hardware Floating-Point Unit	255	NA	9,700	50
1743-1	Communications Controller (Sync, RS232C/ CCITT V.24)	70	NA	2,600	24
1743-2	Communications Controller (Async, RS232C/ CCITT V.24)	85	NA	2,950	24
1590-3	Remote Computer Interface Subsystem	175	NA	6,500	71
1566-20	D/A Conversion Unit	29	NA	1,063	19
1566-21/ 22/33	Conversion Unit	49	NA	1,800	28
10336	Real-Time Clock	30	NA	1,200	12
1720-1	Paper Tape Controller	55	NA	2,000	10
1732-3	Magnetic Tape Controller	180	NA	5,250	42
616-72	Magnetic Tape Transport (7-track, 556/800 bpi, 25 ips)	161	NA	6,000	61
616-92	Magnetic Tape Transport (9-track, 800 bpi NRZI/ 1,600 bpi PE, 25 ips)	191	NA	7,100	71
616-95	Magnetic Tape Transport (50-ips version of 616-92)	207	NA	7,700	77
1725-1	Card Punch & Controller (100/400 cpm)	660	NA	25,000	180

*To connect CDC 1700 peripherals.

OVERVIEW

The ECLIPSE® family of computers is Data General's most recent line of general-purpose minicomputers. ECLIPSE systems run the entire gamut of the Nova/Supernova line they replace, but they add a variety of features to increase speed and throughput; to enhance system reliability and error handling; and above all to expand system capabilities while maintaining compatibility with all Nova/Supernova models. With this line, Data General can compete more aggressively in its current markets and open up new ones. The extended processing power gives Data General's current customers a system to move up to.

The slower-speed (1 microsecond cycle) Nova 2 systems, announced in June 1973, overlapped all models of the Nova/Supernova line except the Nova 840 and the Supernova SC. The S/100 and S/200, the first two ECLIPSE computers, overlap these two systems as well as the rest of the Nova line. Nova 2s, however, are considerably cheaper for comparable configurations. Nova 2/4 is not available in single-unit quantities, however; it must be purchased in quantities of five units. The Nova 2/10 is available at the system level in single-unit quantities.

The ECLIPSE S/100 parallels the Nova 800, Nova 1200, and Supernova computer characteristics while the S/200 parallels the Nova 840 characteristics. Both the S/100 and S/200 outperform their predecessors and offer a superset of system enhancements: error checking and correcting (ERCC) memories composed of core or MOS semiconductor (SC) modules; 16-word bipolar cache memory on SC modules; up to 8-way interleaving of core memory modules, and up to 4-way interleaving of SC memory modules; superset of the Nova/Supernova instruction set to perform bit, byte, and word data manipulations and efficient context switching and stack operations; and optional Writeable Control Store for use-oriented microprogramming. The model 200 offers double user maps plus a data channel map in the mapping option to cut processor overhead in context switching. Table 1 summarizes system specifications.

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Table 1. Data General ECLIPSE: Mainframe Characteristics

MODELS	**S/100, S/200**
CENTRAL PROCESSOR	
Microprogrammed	Yes
Control Memory	ROM
No. of Registers	8 accs: 4 16-bit (2 also used as index regs) and 4 64-bit for fl. pt. arithmetic
Addressing No. of Wds	
Direct	To 64K bytes
Indirect	Multilevel
Indexed	Yes
Mapping	No (S/100; yes (S/200 to 256K bytes)
Overflow Entry	
Instruction Set	
Implementation	Firmware
Types	Single & doubleword
Number	86 std, 66 opt
Floating Point	Hardware option
Hardware Stack	Yes
Writable Control Store (256 56-bit words)	Opt, not software supported
Interrupts	
Levels	16 ext
Type	Hardware
MAIN STORAGE	
Type	MOS, core
Cycle Time, μsec	0.8 (core), 0.7 (MOS), 0.2 (cache)*
Basic Addressable Unit	Wd, byte
Bytes per Access	2
Cache Memory	MOS only
Capacity, bytes	
Min	16K (S/100), 32K (S/200)
Max	64K (S/100), 156K (S/200)
Increment Size, bytes	16K
Ports per Module	1
Error Checks	ERCC opt
Memory Protection	No (S/100); opt (S/200); dual user memory maps, 1 data channel mgs
Overflow Entry	
Memory Management	No (S/100); Yes (S/200)
Interleaving	Core; 8-way MOS 4-way
INPUT/OUTPUT	
Max Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate (MA2)	1,250K wds/sec

Note:
**Effective memory cycle time varies with type of memory and number of memory modules interleaved.*

Many of the ECLIPSE features enhance multiprogramming and multiprocessing in communications, text processing, and process control environments. Dual processors or up to 15 processors can attach to IBM systems while controlling 32 communication lines each; configurations are also available for front-end, message-switching, and network processing. Appropriate software support is provided for most options.

Initially, all software and peripherals for the ECLIPSE computers will be the same software and peripherals available for the Nova/Supernova. No new software has yet been developed to use the unique features of ECLIPSE to best advantage. Table 2 summarizes differences between ECLIPSE and Nova 2 Computers.

First deliveries of both the S/100 and S/200 are scheduled for February 1975.

COMPETITIVE POSITION

With its ECLIPSE Computer, Data General does not find itself in the same position vis-a-vis Digital Equipment's PDP-11 as it was in 1968 with its Nova vis-a-vis the PDP-8. At that time, Digital had no 16-bit computer. Data General capitalized on that fact and sold its 16-bit Nova aggressively and successfully in the OEM market against the 12-bit PDP-8. In 1970, Digital introduced the 16-bit PDP-11, which was new conceptually and architecturally. Digital "bit the bullet" on software because the PDP-11 was not compatible with any of its previous computers and all software had to be developed from scratch. In the meantime, Data General developed substantial system software for its Nova/Supernova line, added optional features, and developed the Nova 840, the true forerunner of the S/200. Until now, Data General has mostly sold the Nova/Supernova against the PDP-8, not the PDP-11. The PDP-11, however, has intruded more and more into PDP-8 territory. With the ECLIPSE, Data General is now tackling the PDP-11 as a competitor.

Two things are particularly significant about the ECLIPSE. First, it is upward compatible with the Nova/Supernova computers; thus the system has a substantial body of inherited software, and Data General is not faced with a massive system software development effort. Second, Data General has rejected the unified bus in favor of a distributed bus structure with the I/O bus separate from the memory bus. It appears Data General learned from Digital's experience. The PDP-11 suffered for a couple of years after its announcement because of its lack of software.

On another front, Data General has experienced some inroads into its own Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. The Digital Computer Controls company has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line, because the expandability of the system allows memory sizes equal to the Nova 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically, the popularity of the Nova/Supernova line has been part of Data General's problem, since the underestimating of demand meant that the company slipped behind schedule from

Table 2. Chief Differences Between ECLIPSE and Nova 2 Computers

COMPUTER MODEL	ECLIPSE S/100	ECLIPSE S/200	Nova 2 2/4	Nova 2 2/10
Packaging				
No. of Slots	7	16	4	10
No. of CPU Boards	2	2	1	1
16K-wd Module	No	No	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5
MEMORY				
Types	Core; MOS	Core; MOS	Core	Core
Max Size (bytes)	64K	256K	64K	64K
Cycle Time	0.8 Core 0.7 MOS 0.2 Cache	0.8 Core 0.7 MOS 0.2 Cache	0.8 or 1.0	0.8 or 1.0
Memory Management				
Protect				
CAPABILITIES				
Stack Processing	Yes	Yes	No	No
Multiply/Divide	Std	Std	Opt	Opt
Microprogrammed	Yes	Yes	No	No
ERCC	Opt	Opt	No	No

Table 3. Comparison of Floating-Point Processor Execution Times in Microseconds

Operation	ECLIPSE (core memory 4-way interleaved)	PDP-11/45 (core memory)	PDP-11/50 (MOS memory)	IBM 370/158(1)
Load	2.8	4.8	3.4	–
Store	2.0	4.8	3.4	–
Add/Subtract	2.4	6.5	5.4	2.0
Multiply	3.9	8.2	7.1	2.0
Divide	4.6	9.9	8.8	8.6
Add/Subtract (long)	2.4	—	—	2.2
Multiply (long)	7.1	14.2	12.3	3.6
Divide (long)	7.8	17.5	15.4	23.2

Note:
(1) Times assume instruction is in buffer 90% of the time.

time to time, and impatient OEM customers bought from the smaller company. This threat was earlier counteracted by the Nova 2 line which is competitive in price and comparable in speed to the D-116.

Although Data General has compared their floating-point processor's instruction execution times with those of the IBM System/370 Model 158 (see Table 3), the real competition for the ECLIPSE system as a whole will be from systems supplied by the minicomputer manufacturers: Digital Equipment, Hewlett-Packard, Interdata, MODCOMP, Varian Data Machines, Computer Automation, General Automation, and Microdata. All of these manufacturers except Computer Automation, which caters exclusively to the OEM market, produce a broad range of processing power in their computer lines. All have discovered gold in the midicomputer range, once sparsely populated and now getting congested, but none can supply the support required by a truly novice user. All supply system software, and the user must prepare the applications software.

The ECLIPSE extends the processing power of the Nova/Supernova line and gives Data General's customers a compatible system for upgrading. In addition, it retains the relatively new Nova 2 low end of the line for the OEM market. Initial comparison of the ECLIPSE floating-point processor execution times with those for the PDP-11/45 and 11/50 indicate the ECLIPSE is faster. (See Table 1.) The cache memory and interleaving of memory modules also increase throughput substantially. Context switching and multiprogramming on larger systems are facilitated by multiple user maps in the mapping unit, and extended operation macroinstructions that, for example, call a procedure and place relevant return information on the stack all in one instruction. These features are impressive and also necessary to make the ECLIPSE truly competitive with the PDP-11 because the PDP-11 is faster than it appears by looking at instruction execution times. The 2-address structure of the PDP-11 as well as the instruction set itself produce tight codes. Generally, fewer instructions are executed per task than on more conventional 1-address computers.

All in all, the ECLIPSE appears to be a well-conceived system from a company that has made few wrong moves in its short life. Also, the system's name "ECLIPSE" is refreshing (not a 3 in it anywhere) and perhaps prophetic. The system will certainly eclipse the Nova/Supernova and probably some competitors, but mostly it will win some and lose some to the PDP-11, HP 3000, MODCOMP I, II, IV, Varian 70, and Interdata 7/16 and 7/32.

MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in France (Paris), West Germany (Frankfurt), England (London), Canada (Hull), and Australia (East Hawthorne-Melbourne). Customer support includes up to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, software subscription service for automatic timely updates of software and documentation, and summary of available software for users not needing revisions. The Data General User's Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special ECLIPSE computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time and materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

COMPATIBILITY

The ECLIPSE computer is generally program-compatible with the Nova/Supernova line, given comparable configurations, but there are some restrictions. ECLIPSE computers implement multiply/divide, hardware floating point, and memory management options differently than Nova/Supernova. For the first two, the difference is chiefly a matter of coding which is easy to

change, but memory management is a little more difficult to alter, because of functional differences, such as double user maps. ECLIPSE also uses the codes for "no-load" and "no-skip" Nova options in the standard instruction set, so Nova programs with these instructions are not compatible and must be altered. A compatible program cannot contain the data channel increment, add-to-memory feature, or execution and I/O time-dependent subroutines.

Both computers use the same type of I/O bus structure, and all Nova/Supernova peripherals can attach to ECLIPSE computers.

CONFIGURATION GUIDE

ECLIPSE S/100, the smallest model, has a memory capacity ranging from 8K to 32K words; core and semiconductor memory modules can be mixed. The CPU has space for seven standard circuit boards. The CPU occupies two boards, and each 8K-word memory module occupies one board. The remaining slots can be used for additional 8K-word memory modules, I/O subsystem controllers, and certain processor options. The S/100, which is designed for instrumentation or control applications with modest requirements, is housed in a small 5.25-inch high chassis but it can be expanded with another 16-slot chassis.

The S/200 system is a larger system designed for medium to large scale end-user applications. The 10.5-inch high chassis can hold 16 circuit boards, and it can be expanded to include another 16-slot chassis. Minimum systems include CPU, 16K words of memory and console. This can be directly expanded up to 32K words; the Memory Allocation and Protection (MAP) option allows memory to be further expanded to 128K words (256K bytes).

The MAP option available only on the S/200 model adds 12 instructions and occupies a full printed circuit board. Other processor options, such as automatic program load, power monitor/auto restart and a real-time clock are available for both systems. The extremely fast hardware floating point processor (FPP) Data General recently introduced is also available; FPP occupies one board and adds 54 instructions to the instruction set. Another important option is Writeable Control Store, which allows users to microprogram their own instructions.

Either system can attach any of the peripherals previously available to the Nova/Supernova line. These include the wide range of high-speed, low-speed, special-purpose, and communications devices listed in Table 4.

Adapters allow the ECLIPSE systems to be configured into multiprocessor configurations. The interprocessor bus allows dual computer/shared disc systems to be configured for front-end and message switching systems needing redundant CPU. An interprocessor bus allows networks of up to 15 Data General computers (Novas, Supernovas, Nova 2s, ECLIPSES) to be interconnected. An IBM 360/370 adapter allows the ECLIPSE to be interfaced directly to an IBM system.

The various operating systems have different minimum configuration requirements. RDOS and MRDOS are the standard ECLIPSE operating systems but RTOS and SOS subsets can be used as well. Table 5 summarizes software system and includes the configuration required for each major package.

Table 4. Data General ECLIPSE: Peripherals

DEVICE MODEL	DESCRIPTION
DISCS	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K wds capacity
6000 Series	Nova discs (fixed-head), 128K, 256K, 512K, 768K wds capacity
4048A	Century 111, 3M wd capacity, IBM 2311 compatible
40578	Century 114, 12M wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M wds capacity
New	Data General, 45.9M-word capacity, like IBM 3330
Magnetic Tape	
4030 I-N	Wang Mag Tape Transports, 7/9-track, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-Drive versions
New	Data General Transports, 7-/9-track, 75 ips
Consoles	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
Paper Tape	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
Punched Card	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm

Table 4. (Contd.)

DEVICE MODEL	DESCRIPTION
Printers	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General Printer, 240, 300 lpm
Displays	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista, 20 lines, 80 char each
A/D, D/A Systems	
4032	Basic A/D interface, Models 4055 A/Q converters, 8 to 15 bits, multiplexors, 2 enclosures (128 single-ended channels, 64 differential)
4037	Basic D/A control, Models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters
4085	Wide range analog input, up to 512 channels, 13 to 15 bits
Plotters	
4017 A-D	CalComp 565 Drum or Rack Mountable, 563 Drum, and 502 Flatbed Plotters
4017E	General Interface Board
Digital	
4065	I/O Interface Subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Read-time clocks, 10/100/1,000 Hz frequencies
4040	General Interface Board
Communications	
4015	High-speed Controller 600-50,000 baud
4025	IBM 360/370 Interface
4038	Multiprocessor Communications Adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async, controller subsystem, up to 1,024 lines

Table 5. Data General ECLIPSE: System Software

PACKAGE	DESCRIPTION
RDOS	Realtime Disc Operating System, foreground/background multiprocessing, multiprogramming; requires 16K wds memory, S/100 or S/200 CPU, 2.5M disc, console
MRDOS	Mapped Realtime Disc Operating System, requires 24K wds memory, S/200 with MAP, 2.5M disc, console
RTOS	Small basic, real-time, executive, requires 4K wds of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette or mag tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV, runs under RDOS, MRDOS and SOS, requires 8K wds of memory, CPU, console

Table 5. (Contd.)

PACKAGE	DESCRIPTION
FORTRAN 5	Superset of FORTRAN IV, runs under RDOS or MRDOS, requires 28K wds of memory, CPU, console
ALGOL	Extended ALGOL 60, runs under RDOS or MRDOS, or stand-alone, requires 12K wds of memory, CPU, console
BASIC	2 versions, of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions require 4K, 8K and 16K wds of memory, respectively; CPU, console
Utilities	Text editor, library, loaders, debuggers

PRICE DATA

Model No.	Description	Purchase Price (1) $
S/100	Computer (microprogrammed CPU with capacity for 64K bytes of memory) with	
	16K Bytes Std Core	9,200
	16K Bytes ERCC Core	11,200
	32K Bytes Std Core	11,900
	16K Bytes Std SC	10,700
	16K Bytes ERCC SC	12,700
	32K Bytes SC	14,900
S/200	Computer (microprogrammed CPU with capacity for 256 bytes of memory) with	
	32K Bytes Std Core	16,300
	32K Bytes ERCC Core	19,300
	128K Bytes Std Core	32,500
	32K Bytes Std SC	19,300
	32K Bytes ERCC SC	22,300
	128K Bytes SC	44,500
	Memories*	
	16K-Byte Core	2,700
	16K-Byte ERCC Core	3,700
	16K-Byte SC Memory	4,200
	16K-Byte SC ERCC	5,200
	Representative Systems	
	Small Process Control System including:	46,600
	ECLIPSE S/100	
	64K Bytes ERCC Memory	
	Fixed-Head Novadisc	
	A/D Subsystem	
	PT Reader	
	Display Terminal	
	Remote Data Concentrator including:	33,350
	ECLIPSE S/100	
	48K Bytes of Memory	
	Communications Interfaces	
	Large Data Base Management System including:	186,700
	S/200 Computer	
	256K Bytes of Memory	
	2 3330-Type Disc Pack Drives	
	Line Printer	
	Card Reader	
	13 Display Terminals	
	Large Dual Processor System	263,000
	for message switching or front-end processing	
	2 S/200 Computers each with	
	256K Bytes of Memory	
	3330-Type Disc Pack	
	Fixed-Head Novadisc	
	2 Magnetic Tape Transports	
	2 Display Terminals	
	FORTRAN 5 System in Computation Environment	81,400
	S/200 Computers	
	96K Bytes of Core Memory	
	64K Bytes of SC Memory	
	Floating-Point Processor	
	Moving-Head Disc	
	Magnetic Tape Transport	
	Line Printer	
	Card Reader	
	Display Terminal	

Notes:
* *ERCC = Error Checking and Correcting.*
(1) Quantity discounts range from 10% to 40%.

HEADQUARTERS

Data General Corporation
Southboro MA 01772

DATA GENERAL CORP.
ECLIPSE Report Update

COMMUNICATIONS SUBSYSTEM

Data General now offers a new communications subsystem and software to support it.

The subsystem includes the following components: ALM-16, a 16-line asynchronous multiplexor; ALM-8, eight-line asynchronous multiplexor with full modem control; SLM-2, a two-line synchronous multiplexor; and DCU/50 data control unit for high-level communications throughput. Communications Access Manager (CAM) software provides line handling support.

The DCU/50 user-programmable communications controller performs character processing and line protocol functions in parallel with a central processor or a dedicated communications processor. The unit has a 2048-byte random access bipolar memory and fast instruction execution time of 600 nanoseconds for add and subtract and 900 nanoseconds for load-store. Maximum communications throughput is 48K characters per second. Additional DCU/50s can be interfaced to a host computer's DMA channel for higher throughput and heavy data communications traffic. One control unit can support multiple protocols and up to 256 mixed synchronous and asynchronous lines connected through the ALM and SLM multiplexors.

The Communications Access Manager software includes line handling support for various lines: local asynchronous lines, remote asynchronous lines with modem control, synchronous lines with or without modem control, and DCU/50-based communications facilities. The CAM software runs under Data General's RTOS, RDOS, and MRDOS operating systems; it has an interrupt service feature that allows it to reside on mass storage when communications tasks are not being performed.

The modular nature of CAM allows users with ALM-8, ALM-16, or SLM-2 multiplexors to add the DCU/50 controller without reprogramming the application. Portions of CAM can reside in the DCU/50, reducing the main CPU overhead for both instruction execution and character handling.

Line procedures include an asynchronous line teleprinter-oriented protocol and synchronous line BISYNC protocol. CAM provides for multi-drop lines using polled or select sequences, allowing easy system expansion. Protocols for unique I/O devices can be generated through a low-level interface incorporating user-written line procedures. A FORTRAN IV or FORTRAN 5 interface is available.

The COMGEN system generation program allows users to specify interactively standard variables such as line types, character size, control characters, buffer size, and time out intervals. Parameters for message assembly/disassembly, code conversion, and control character generation and detection can also be entered.

PRICE DATA

	Purchase Price $
DCU/50	3000
ALM-16	2640
ALM-8	2000
SLM-2	1500
Basic Subsystem (includes DCU/50 and software; ALM-16, SLM-2, data communications chassis, and cabling)	8940

IBM 2780 EMULATOR AND HASP WORKSTATION EMULATORS

Data General computers can now work as remote job entry terminals for IBM 360/370 computers via an IBM 2780 emulator and an IBM HASP workstation emulator with multileaving and interleaving. Both programs run under Data General's RTOS and RDOS operating systems; 16K words of memory are required for the HASP program to run under RTOS and 24K words are required for RDOS.

The HASP program features full multileaving for up to seven input and seven output data streams for maximum

use of multiple devices. Data block interleaving and data compression are performed for efficient data transmission. HASP can operate with disc, magnetic tape, video display, card readers, and line printers.

The 2780 and HASP programs are free of charge when ordered as part of a remote intelligent processing system. A minimum RTOS system that includes a processor with 16K words of core, A/N display terminals, and a line printer costs approximately $20,000. A minimum RDOS system requires an additional 8K words of memory and a disc drive; this system costs about $35,000.

OVERVIEW

Data General's Nova 2 line is a compact, low-cost replacement system for the Nova/Supernova line, chiefly in the OEM market. Nova 2 is functionally identical to the Nova/Supernova line architecture and compatible with all models except the Nova 840. The CPU has been redesigned to fit on a single circuit board; new low-cost core memory has been manufactured by Data General in 4K- and 8K-word modules that cycle at 800 nanoseconds and in a 16K-word module that cycles at 1,000 nanoseconds. Because Nova 2 is completely software and hardware compatible with the Nova/Supernova, it has a large body of tested facilities for support of many types of applications. Rock bottom prices, at least at this point in time, are possible because of the reduction in component size. This system unquestionably announces Data General's intention to continue vigorously competing in the OEM market, which in the past comprised around 50 percent of all installations.

Nova 2 has two submodels: the 2/4, a 4-slot system in a 5.25-inch high chassis weighing 50 pounds for a minimum system, and the 2/10, a 10-slot system in a 10.5-inch chassis weighing 110 pounds for a minimum system.

Nova 2 architecture, like the Nova/Supernova, is not microprogrammed, and it has a conventional bus arrangement. DMA and programmed I/O and a 16-level priority interrupt system are standard features. Up to 61 devices can be addressed but these can be multiplexed subsystems. Four accumulators, two of which are index registers, and 16 memory registers allow a variety of addressing modes. The instruction set allows a great many permutations of basic arithmetic and logical basic instructions so that several operations can be performed with one instruction. The memory bus is asynchronous, allowing different speed modules to be mixed on a system. In addition to manufacturing its own core, Data General has begun making a large number of its own peripherals, including discs, magnetic tape and cassette drives, printers, paper tape readers and CRTs. Table 1 summarizes system specifications.

Software for the Nova 2 includes a Real-Time Disk Operating System (RDOS), a Real-Time Operating System (RTOS), and a Stand-Alone Operating System (SOS); FORTRAN IV, FORTRAN 5 and ALGOL compilers; BASIC interpreters; three assemblers; cross assemblers for IBM 360/370, Univac 1100, and CDC 6000 systems; and a variety of utilities and applications.

Table 1. Data General Nova 2: Mainframe Characteristics

MODELS	
CENTRAL PROCESSOR	
Microprogrammed	No
No. of Registers	
Accumulators	4
Hardware Index	2
Memory	16
Addressing (wds)	
Direct	1,024
Indirect	32K
Indexed	Yes
Mapping	No
Instruction Set	
Implementation	Hardware
Number	202 (counting implemented sub-instructions)
Floating Point	Option
Hardware Stack	No
Writeable Control Store	No
Interrupts	
Levels	16
Type	Hardware
MAIN STORAGE	
Type	Core
Cycle Time, μsec	0.8, 1.0*
Basic Addressable Units	Word, byte
Capacity, bytes	
Min	8K
Max	64K
Increment Size (bytes)	8K, 16K, 32K
Ports per Module	1
Error Checks	Parity option
Memory Protection	No
Memory Management	No
Interleaving	Up to 8-way core, 4-way on MOS
INPUT/OUTPUT	
Max Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate	1,250K wds/sec

Note:
**Effective memory cycle time varies with type of members and number of memory modules interleaved.*

The Nova 2 systems were announced in June, 1973 and first delivered in 1973.

COMPETITIVE POSITION

Data General has experienced some inroads on its Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. The Digital Computer Controls (DCC) company has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line, because the expandability of the system allows memory sizes equal to the Nova 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically the popularity of the Nova/Supernova line has been part of Data General's problem; the company underestimated demand, slipped behind schedule from time to time, and as a result impatient OEM customers bought from the smaller companies. This competitive threat is counteracted by the Nova 2 line which is very competitive in price, comparable in speed, flexibility, and size.

The small size and reduced number of components work together to make the Nova 2 very competitive with one-board OEM minis and microcomputers from other manufacturers such as Computer Automation and General Automation. The 16K-word memory board allows the user more memory for a very small price increase over the minimum system and at prices lower than minimum systems of a year ago. This can save both OEM and end-user costs because of the ability to handle high-level languages in the larger memory, sometimes cutting programming time and costs by more than half.

The capabilities of the Nova 2 are expanded in Data General's compatible ECLIPSE® line. The ECLIPSE family of computers is Data General's most recent line of general-purpose minicomputers. The ECLIPSE systems run the gamut of the Nova/Supernova line that they replace, but with a variety of features added to increase speed and throughput; to add to system reliability and error handling; and above all to expand the flexibility of the system while maintaining compatibility with all Nova and Supernova models. With this line, Data General hopes to compete more aggressively in its former end-user markets while opening up new ones. The extended processing power gives Data General's current customers a system to move up to, and, as the line develops, they will undoubtedly find even more upward possibilities. OEM customers with greater speed, size, and checking requirements will be also interested in ECLIPSE. Table 2 highlights some of the chief differences between the Nova 2 and the ECLIPSE systems.

As the second largest minicomputer manufacturer, Data General has the worldwide service and support capabilities so important to many OEM manufacturers. These facilities are receiving increased emphasis, with two new software support services recently announced.

CONFIGURATION GUIDE

Data General introduced the Nova computers in 1973 as their OEM line. The minimum order for this equipment was five. To bring the price/performance advantages of the Nova 2 to the end user, Data General has announced end-user systems built around the Nova 2s, available in single quantities. These Nova 2 end-user systems now use the standard Data General operating systems.

The chief difference between the Nova 2/4 and 2/10 models is in packaging. The 2/4 is housed in 5.25-inch high chassis with four slots, while the 2/10 is housed in a 10.5-inch high chassis with 10 slots. The CPU in both cases is contained on a single circuit board, and single board modules are available for 4K words, 8K words,

Table 2. Chief Differences Between ECLIPSE® and Nova 2 Computers

COMPUTER MODEL	ECLIPSE S/100	ECLIPSE S/200	Nova 2 2/4	Nova 2 2/10
Packaging				
No. of Slots	7	16	4	10
No. of CPU Boards	2	2	1	1
16K-wd Module	No	No	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5
MEMORY				
Types	Core; MOS	Core; MOS	Core	Core
Max Size (bytes)	64K	256K	64K	64K
Cycle Time	0.8 Core 0.7 MOS 0.2 Cache	0.8 Core 0.7 MOS 0.2 Cache	0.8 or 1.0	0.8 or 1.0
Memory Management				
Protect				
CAPABILITIES				
Stack Processing	Yes	Yes	No	No
Multiply/Divide	Std	Std	Opt	Opt
Microprogrammed	Yes	Yes	No	No
ERCC	Opt	Opt	No	No

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and 16K words of core. The 16K-word module is available only in the slower memory, 1.0 microsecond cycle time, however. Different speed memory modules can be mixed on one system. Options for Nova 2 systems include:

- Hardware multiply divide.
- Hardware floating-point arithmetic.
- Turnkey console.
- Power monitor/auto restart.
- Automatic program load.

Both can attach an expansion chassis adding 16 more slots.

MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, the Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in Paris, France; Frankfurt, West Germany; London, England; Hull, Canada; and East Hawthorne-Melbourne, Australia. Customer support includes up to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software for users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special ECLIPSE computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high-priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

Minimum systems include 4K words of memory. These can be expanded up to 32K words of memory with console, peripherals, communication devices, and so on attached. Peripherals of all sorts are available, as noted in Table 3. Configuration requirements are basically determined by the operating system, language processors,

Table 3. Data General Nova 2: Peripherals

DEVICE MODEL	DESCRIPTION
DISCS	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K wds capacity
6000 Series	Nova discs (fixed-head), 128K, 256K, 512K, 768K wds capacity
4048A	Century 111, 3M wd capacity, IBM 2311 compatible
40578	Century 114, 12M wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M wds capacity
New	Data General, 45.9M-word capacity, like IBM 3330
Magnetic Tape	
4030 I-N	Wang Mag Tape Transports, 7/9-track, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-Drive versions
New	Data General Transports, 7-/9-track, 75 ips
Consoles	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
Paper Tape	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
Punched Card	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm
Printers	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General Printer, 240, 300 lpm
Displays	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista, 20 lines, 80 char each
A/D, D/A Systems	
4032	Basic A/D interface, Models 4055 A/Q converters, 8 to 15 bits, multiplexors, 2 enclosures (128 single-ended channels, 64 differential)
4037	Basic D/A control, Models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters

Table 3. (Contd.)

DEVICE MODEL	DESCRIPTION
4085	Wide range analog input, up to 512 channels, 13 to 15 bits
Plotters	
4017 A-D	CalComp 565 Drum or Rack Mountable, 563 Drum, and 502 Flatbed Plotters
4017E	General Interface Board
Digital	
4065	I/O Interface Subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Read-time clocks, 10/100/1,000 Hz frequencies
4040	General Interface Board
Communications	
4015	High-speed Controller 600-50,000 baud
4025	IBM 360/370 Interface
4038	Multiprocessor Communications Adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async, controller subsystem, up to 1,024 lines

and so forth which are used. Operating systems and their requirements are listed in Table 4.

Data General also offers a dual-processor shared-disc configuration using Nova 2/10s. Each processor has 32K words of memory, a real time clock, and a console terminal. The two CPUs are housed in a dual cabinet and connected by an interprocessor bus. They share a disc subsystem which can include anywhere from 2.5M to 200M words of storage.

The interprocessor bus consists of the following components:

- Buffer — Under control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors both request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — Carries the data for intercomputer communication.
- Dual one-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The Multiprocessor Communications Adapter (MCA) interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of one million bytes per second.

COMPATIBILITY

The Nova 2 Systems are software compatible, given comparable configurations, with all Nova/Supernova computers except the Nova 840. The line is also software

Table 4. Data General Nova 2: System Software

PACKAGE	DESCRIPTION
RDOS	Realtime Disc Operating System, foreground/background multiprocessing, multiprogramming; requires 16K wds memory, S/100 or S/200 CPU, 2.5M disc, console
MRDOS	Mapped Realtime Disc Operating System, requires 24K wds memory, S/200 with MAP, 2.5M disc, console
RTOS	Small basic, real-time, executive, requires 4K wds of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette or mag tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV, runs under RDOS, MRDOS and SOS, requires 8K wds of memory, CPU, console
FORTRAN 5	Superset of FORTRAN IV, runs under RDOS or MRDOS, requires 28K wds of memory, CPU, console
ALGOL	Extended ALGOL 60, runs under RDOS or MRDOS, or stand-alone, requires 12K wds of memory, CPU, console
BASIC	2 versions, of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions require 4K, 8K and 16K wds of memory, respectively; CPU, console
Utilities	Text editor, library, loaders, debuggers

compatible with the ECLIPSE line except for a few instructions relating to optional features, like signed hardware multiply divide.

Peripherals from all three lines are interchangeable.

PRICE DATA

Number	Description	Purchase $ (1)	Monthly Maint. $
	DATA GENERAL NOVA 2/4 & 2/10		
	CENTRAL PROCESSORS & WORKING STORAGE		
	Nova 2/4 Processors (4 accs; PIO bus; 17-level interrupt; DMA; 4 additional subassembly slots; rack mountable)		
8331	With 4K Words of Core Memory	3,500	40
8332	With 4K Words of Core Memory	4,000	52
8333	With 16K Words of Core Memory	5,600	64
8334	With 24K Words of Core Memory	7,600	96
8335	With 32K Words of Core Memory	9,100	108
	Nova 2/10 Processors (4 accs; PIO bus; 16-level interrupt; DMA; 10 additional subassembly slots; rack mountable)		
8351	With 4K Words of Core Memory	4,400	44
8352	With 8K Words of Core Memory	4,900	56
8353	With 16K Words of Core Memory	6,500	68
8354	With 24K Words of Core Memory	8,500	100
8355	With 32K Words of Core Memory	10,000	112
	Memories		
8300	Memory with (4K words)	2,000	20
8301	Memory with (8K words)	2,200	32
8302	Memory with (16K words)	3,500	44
	Processor Options		
8306	Power Monitor and Auto Restart	400	1
8307	Multiply/Divide	1,600	13
8308	Automatic Program Load	400	2
8020	Floating-Point Processor	4,000	32
	Packaged Systems		
	Nova 2/10 RTOS Systems		
	System A		
9001	Part 1 consists of 8358 Nova 2/10 Computer (with 16,384-word core memory in tabletop enclosure, 8306 power monitor and auto restart, 4007 I/O interface subassembly, 4010 Teletype/video display I/O interface and 4008 real-time clock)	9,150	102
900XA	Part 2 consists of a 4010A Teletype model 33ASR keyboard/printer (for 9001, 9002, 9003, 9004)	1,750	102
	Nova 2/10 SOS Systems		
	System A		
9005	Part 1 consists of 8353 Nova 2/10 Computer (with 16,384-word core memory and slides for rack mounting, 4007, 4010, 4011 paper tape reader control, 6013 high-speed paper tape reader and 4012 paper tape punch control)	11,000	135
	Part 2 consists of 4010A, 4012A High-speed Paper Tape Punch, and 1012F Single-Bay Rack Cabinet (for 9005, 9006)	5,100	135
	Nova 2/10 RDOS Systems		
	System A		

PRICE DATA (Contd.)

Model Number	Description	Purchase $ (1)	Monthly Maint. $
9011	Part 1 consists of 8355 Nova 2/10 Computer (with 4007, 4010, 4011, 6013, 4046 moving head disc control, 4047 moving head disc adapter and power supply, and 5 remaining slots in computer chassis)	19,450	237
90XXH	Part 2 consists of 4010A, 4047A Moving Head Disc Drive with 1.247 Million Words capacity; 4047C Disc Cartridge, and 1012F Single-Bay Rack Cabinet (for 9011, 9012)	7,900	257
	Dual Nova 2/10 System		
9022	Part 1 consists of 8355 Nova 2/10 Computer (with 8306, 8308, 4007, 4008, 4010, 4119, 4011, 6013, 4240 interprocessor bus, 4046, 4047, and 4 remaining slots in computer chassis)	22,600	510
9022A	Part 2 consists of 40101, 1065F Interprocessor Bus Cable, 4047B, 4047C and 1012G 2-Bay Rack Cabinet	13,400	510
9023	Part 3 consists of 8355 Nova 2/10 Computer 8306, 8308, 4007, 4008, 4010, 4240, 4046, and 4 remaining slots in computer chassis	18,850	510
9023A	Part 4 consists of 4010A, EC4047 Moving Head Disc Adapter and Power Supply Cable, and IC4011 Paper Tape Reader Control Cable	2,250	510

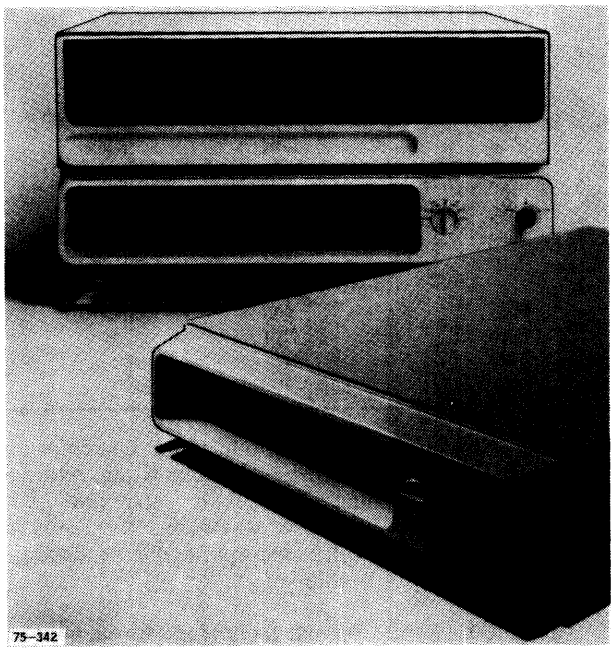
Notes
(1) Nova 2/4 is available only in minimum quantity orders of 5 systems.

HEADQUARTERS

Data General Corporation
Southboro MA 01772

DATA GENERAL CORP.

Nova 3 System Report



OVERVIEW

The Nova 3 line is Data General's most recent line of 16-bit minicomputers aimed primarily at the OEM (Original Equipment Manufacturers) market. Like the Eclipse line, Nova 3 extends the previous Nova/Supernova architecture to include stack processing and facilities for more efficient memory management, without loss of compatibility with all previous Nova systems. The Nova 3 line is compact like the Nova 2, but it is faster, less expensive and more versatile, and can support four times as much memory. The Nova 3 essentially replaces all of the Nova/Supernova line, with the exception of some of the larger configurations of the 830 and 840.

The main competitive challenge of the Nova 3 is toward neither the microcomputer (computer-on-a-board) segment nor the midicomputer segment of the market but rather it is toward the central OEM market that has been the mainstay of all minicomputer manufacturers. The popular Nova architecture is retained and extended by Nova 3. Thus, Nova 3 enters the market with a tried-and-true design and a body of proven software larger than that of any other 16-bit system in the marketplace. Best of all, Nova 3s are cheaper than any comparable Data General systems on the market and can use the 700-nanosecond MOS memories produced using Data General's own memory chassis. Table 1 compares the Nova 2, Nova 3, and Eclipse lines.

Like the Nova 2, the Nova 3 has two submodels designated by the number of slots that can be included in the main chassis. Model 3/4 has four slots, and it is housed in a half-size chassis, which is useful for applications requiring a small computer in a restricted space. Up to 32K words of memory can be included in the chassis by using two 16K-word memory boards. Model 3/12 has 12 slots, and up to 128K words (256K bytes) can be housed in the mainframe. But, memory beyond 32K words requires the memory management option. The 3/12 can also attach a 12-slot expansion chassis.

Nova 3 has all the features associated with the Nova/Supernova line plus extensions for stack processing and efficient memory management. Two hardware stack registers have been added to the usual Nova complement of 4 hardware registers, 1 program counter, and 16 autoincrement/autodecrement memory registers. Addressing modes include direct, relative, indexed, and multilevel indirect addressing in various combinations. The register-based stack addressing is on a last-in/first-out and random-indexed basis. The bus system includes separate I/O and memory buses with both standard-speed and high-speed modes on the DMA channels. Up to 61 devices can be addressed, with a supporting 16-level priority interrupt system. The Nova/Supernova instruction set has been expanded to include single-word PUSH/POP and multiword SAVE/RETURN stack instructions, memory management instructions, and a trap for undefined instruction codes. The trap allows user-defined instructions or emulation of the instructions unique to the Eclipse systems. Thus, Nova 3 can be made compatible with Eclipse.

All previous Nova/Supernova peripherals can be attached to the Nova 3, including discs, tapes, card and paper tape I/O, printers, analog/digital systems, plotters, terminals, communications subsystems, and a variety of other special peripheral devices and subsystems. Data General has recently redesigned its communications subsystems, adding modular programmable multiplexors that can operate from very low to very high speeds.

The MOS memory modules are made up of 4K-bit, n-channel, 20-pin MOS RAM chips manufactured by Data

HEADQUARTERS

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Table 1. Chief Differences Between Eclipse, Nova 2, and Nova 3 Computers

COMPUTER	Eclipse		Nova 2		Nova 3	
MODEL	S/100	S/200	2/4	2/10	3/4	3/12
PACKAGING						
No. of Slots	7	16	4	10	4	12
No. of CPU Boards	2	2	1	1	1	1
16K-wd Module	No	No	Yes	Yes	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5	5.25	10.5
MEMORY						
Types	Core; MOS	Core; MOS	Core	Core	Core; MOS	Core; MOS
Max Size (bytes)	64K	256K	64K	64K	64K	256K
Cycle Time, μsec	0.8 (Core) 0.7 (MOS); 0.2 (Cache)	0.8 (Core; 0.7 (MOS); 0.2 (Cache)	0.8 or 1.0	0.8 or 1.0	0.8 or 1.0 (Core); 0.7 (MOS)	0.8 or 1.0 (Core); 0.7 (MOS)
Memory Management	No	Opt	No	No	No	Opt
Protect	No	Opt	No	No	No	No
CAPABILITIES						
Stack Processing	Yes	Yes	No	No	Yes	Yes
Multiply/Divide	Std	Std	Opt	Opt	Opt	Opt
Microprogrammed	Yes	Yes	No	No	No	No
ERCC	Opt	Opt	No	No	No	No

Table 2. Data General Nova 3: Mainframe Characteristics

MODELS	3/4 and 3/12
CENTRAL PROCESSOR	
Microprogrammed	No
No. of Registers	
Accumulators	4
Hardware Index	2
Hardware Stack	2
Memory	16
Addressing (wds)	
Direct	1,024
Indirect	32K
Indexed	Yes
Mapping	Option on 3/12
Instruction Set	
Implementation	Hardware
Number	212 (counting implemented sub-instructions)
Floating Point	Option
Hardware Stack	Std
Writeable Control Store	No
Interrupts	
Levels	16
Type	Hardware
MAIN STORAGE	
Type	Core/MOS
Cycle Time (μsec)*	0.8, 1.0 (Core); 0.7 (MOS)
Basic Addressable Units	Word, byte
Capacity (bytes)	
Min.	8K (Core); 4K (MOS)
Max.	32K (3/4);128K (3/12)
Increment Size (bytes)	8K, 16K, 32K
Ports per Module	1
Error Checks	Parity option on MOS
Memory Protection	On 3/12 with MMU
Memory Management	On 3/12
Interleaving	Up to 8-way, core; 4-way, MOS
INPUT/OUTPUT	
Max. Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate (bytes/sec)	434K
DMA High-Speed Mode (bytes/sec)	2.2M, input; 1.66M, output

*Effective memory cycle time varies with type of memory and number of memory modules interleaved.

General at its Sunnyvale, California plant. The chips are assembled, wired, and packaged in Hong Kong, returned to Sunnyvale for testing, then incorporated into MOS memory modules at Southboro, Massachusetts. Texas Instruments 4K-bit chips will be incorporated in a substantial number of the Nova 3s shipped.

The CPU uses MSI bipolar technology throughout.

Data General offers the 700-nanosecond memory with or without parity. Parity is unavailable for the 800- and 1,000-nanosecond core memory modules. A battery back-up for power loss is also available for systems with MOS memory. Maximum memory capacity is 128K words. Memory expansion beyond 32K words requires the memory management unit, which provides two program maps and two data channel maps but no protection facilities. Data General Nova 3 software does not support dual program maps, thus these features are useful only for OEMs who write their own software.

Software for Nova 3 consists of the software available for the rest of the Nova line: Real-Time Operating System (RTOS), Real-Time Disc-Based Operating System (RDOS), and Mapped Real-Time Disc-Based Operating System (MRDOS). High-level languages include Assembler, Macro Assembler, ALGOL, Extended BASIC, FORTRAN IV, and FORTRAN 5. Table 2 lists the mainframe characteristics.

Nova 3 was announced in October 1975. Deliveries will begin in January 1976.

Competitive Position

Data General spokesmen use the term "vertical integration" to mean company manufacture and control of all the pieces in a Data General computer system. Manufacturing as many parts as possible allows the company to add value all along the way and to make money doing so. Data

General is selling the Nova 3 only in system packages; this discourages users from adding plug-compatible memories from independent manufacturers.

Data General spokesmen indicated that no plans are afoot to offer board-only or stripped systems. These spokesmen appear happy to let others fight for the low profits inherent in this market; they seem unconcerned that competitors will capture entry-level customers who may upgrade someday. Thus, competitors for Nova 3 are minicomputer *systems:* Digital PDP-11/04, 11/35, and 11/45; Hewlett Packard HP 21MX; Modular Computer Systems MODCOMP II; Interdata 7/16 and 7/32; General Automation GA-16 Series; and Digital Computer Controls 16 Series. Table 3 compares Nova 3 with the PDP-11/04, GA-16/330, PDP-11/45, and HP 21MX.

The PDP-11/45 is more powerful than Nova 3, and it is also considerably more expensive. Also, COBOL is available for the PDP-11/45 and currently unavailable for Nova 3.

The HP 21MX is slower than Nova 3 and also more expensive. Hewlett Packard systems are usually priced higher than those from other minicomputer manufacturers. The company generally does not play cost-cutting games but counts on its service, maintenance support, and software to justify higher prices. For example, IMAGE/2000, a data base management system similar to TOTAL, is available for the 21MX.

The GA-16/330 is somewhat slower than the Nova 3 and also more expensive. COBOL is now available for the GA-16 Series. Other members of the GA-16 Series, such as the GA-16/220, also compete with smaller configurations of the Nova 3.

Digital's PDP-11/04 is also very competitive for smaller Nova 3 configurations. It is a low-cost system that can be upgraded through the whole PDP-11 line.

On one hand, the Nova 3 is a relatively unexciting system because it offers nothing really new. On the other hand, Nova 3 is a very important system for Data General and for other minicomputer manufacturers because it does the same old things very well at a very attractive price.

The price/performance of the Nova 3/4 and 3/12 packages will be hard to beat. Data General knows the OEM market and likes to sell to it. The Nova 3 reflects both this knowledge and desire. Although the result isn't a masterpiece, it should satisfy the user who wants a solid system he can afford.

CONFIGURATION GUIDE

The Nova 3 line consists of two models that differ in the number of slots in the basic chassis. The number of slots determines the expansion capabilities of the basic system; thus, the Nova 3/4, with a 4-slot chassis, has been designed for small configurations, and the Nova 3/12, with a 12-slot chassis, is for large configurations. The 3/12 can support an expansion chassis that provides 12 additional I/O slots. Figure 1 shows the typical layout of the slots on a 3/12 system.

A minimum system includes 4K words of memory. Memory for Nova 3 can consist of 700-nanosecond MOS memory available in modules of 4K, 8K, and 16K words, or 800/1,000-nanosecond core memory available in modules of 8K or 16K words. Core cycle time is 800 nanoseconds for 8K-word modules and 1,000 nanoseconds for 16K-word modules.

The following options are available for the Nova 3:
- Memory mapping.
- Battery backup.
- MOS memory parity.
- Hardware multiply/divide (signed).
- Hardware floating-point arithmetic.
- Turnkey console.
- Power monitor/auto restart.
- Automatic program load.

Peripherals of all sorts are available, as noted in Table 4. Configuration requirements are determined by the operating system, language processors, and application programs. Operating systems and their requirements are listed in Table 5.

Data General also offers a dual-processor, shared-disc configuration using Nova 3. Each processor has 32K words of memory, a real-time clock, and a console terminal. The two CPUs are housed in a dual cabinet and are connected by an interprocessor bus. They share a dual-ported disc subsystem which can include anywhere from 2.5M to 200M words of storage.

The interprocessor bus consists of the following components:
- Buffer — Under the control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — These lines carry the data for intercomputer communications.
- Dual one-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The Multiprocessor Communications Adapter (MCA) interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of one million bytes per second.

Compatibility

The Nova 3 systems are software and hardware compatible with all previous Nova and Supernova systems, including the Nova 2. Software developed for Eclipse sys-

Table 3. Data General Nova 3 Compared with Major Competitors

	Data General Nova 3	Digital PDP-11/04	General Automation GA-16/330	Digital PDP-11/45(1)	Hewlett Packard HP 21MX
Word Length (bits)	16/16 + 1 parity	16	16/16 + 2 parity	16/16 + 2 parity	16
Inst. Times (μsec)					
Add	1.8	3.2	4.6	0.8-1.8	1.9
Multiply	6.9(2)	NA	21.2	3.6-4.7	12.8
Divide	7.5(2)	NA	20.3	7.5-8.6	17.0
Floating Pt. Add	7.7*	—	*	2.8-6.5*	22-54*
Floating Pt. Multiply	11.3*	—	*	3.0-8.2*	48-57*
Floating Pt. Divide	13.7*	—	*	3.0-9.9*	41-76*
Max. Memory (bytes)	64K/256K	56K	128K	253,952	512K
No. of GP Registers	4	8	16	16	4
Max DMA Rate (bytes/sec)	2M	2.8M	2M	2M	1.2M
Price, $					
CPU + Memory					
32K bytes	4,400	(3)	5,250	23,900	7,650
64K bytes	7,100	(3)	8,250	32,000	11,800
256K bytes	34,200	—	—	55,500(4)	36,150

* Optional, at extra cost. NA - Not available. — Not applicable.

Notes:
(1) The PDP-11/45 can use core, MOS, or bipolar memories; the first number is for bipolar memory and the second number for core memory. Price is for core memory.
(2) Operands are unsigned integers on std.
(3) Digital has not announced price of unbundled memory although the 11/04 can support 56K bytes. Price for 16K-byte system with 9-slot chassis is $3 545.
(4) Maximum memory is 253,952 bytes.

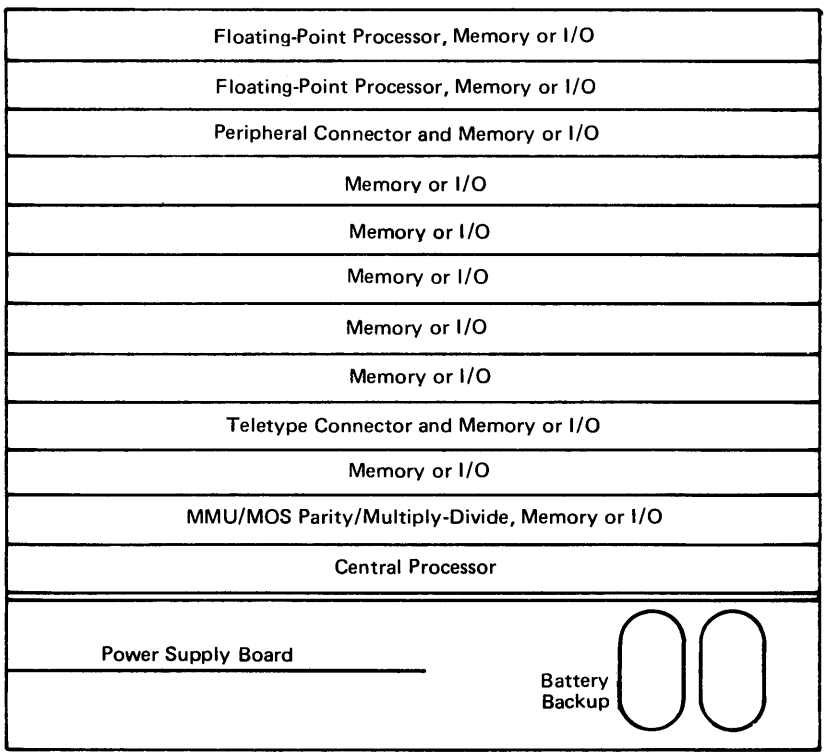

Figure 1. Nova 3/12 Slot Allocation

Table 4. Data General Nova 3: Peripherals

DEVICE MODEL	DESCRIPTION
Discs	
4019 A/B/C	Alpha Data (fixed-head); 64K, 128K, 256K-wds capacity
6000 Series	Nova discs (fixed-head); 128K, 256K, 512K, 768K wds capacity
4048A	Century 111; 3M wds capacity; IBM 2311 compatible
40578	Century 114; 12M wds capacity; IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge); 1.2/2.4M wds capacity Data General; 45.9M wds capacity; like IBM 3330
6030/6031	Data General diskettes; 31K wds capacity; dual/single drives
Magnetic Tape	
4030 I-N	Wang mag tape transports; 7-/9-track; 12.5/45/75 ips
4000 Series	Nova cassettes; 1-, 2-, or 3-drive versions
New	Data General transports; 7-/9-track; 75 ips
Consoles	
4010 A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
Paper Tape	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
Punched Card	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark sense card readers, 150/285/400/600/1,000 cpm
Printers	
4034A/B	Data Products 356/245 lpm; 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General printer; 240/300 lpm
Displays	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista; 20 lines, 80 char each
A/D, D/A Systems	
4032	Basic A/D interface, Models 4055 A/Q converters; 8 to 15 bits; multiplexors; 2 enclosures (128 single-ended channels, 64-differential)
4037	Basic D/A control, for 24 converters
4085	Wide range analog input; up to 512 channels; 13 to 15 bits
Plotters	
4017A-D	CalComp 565 drum or rack mountable; 563 drum, and 502 flatbed plotters
4017E	General interface board
Digital	
4065	I/O interface subassembly; 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools; 500-lpm feed
4008/4079	Real-time clocks; 10/100/1,000 Hz frequencies
4040	General interface board
Communications	
ALM-8	Async multiplexor for 4 or 8 lines; to 9,600 baud
ALM-16	Async multiplexor for 8 or 16 lines; to 9,600 baud
SLM-2	Sync multiplexor for 1 or 2 lines; to 56K baud
DCU/50	Communication control unit for up to 256 async and sync lines

Table 5. Data General Nova 3: System Software

PACKAGE	DESCRIPTION
RDOS	Real-time Disc Operating System, foreground/background multiprocessing; multiprogramming; requires 16K wds memory, CPU, 2.5M wd disc, console
MRDOS	Mapped Real-time Disc Operating System; requires 24K wds memory, with MAP, 2.5M disc, console
RTOS	Small basic, real-time, executive; requires 4K wds of memory, real-time clock, CPU console
SOS	Subset of RDOS for minimum stand-alone; non-disc systems; cassette or mag tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV; runs under RDOS, MRDOS, and SOS; requires 8K wds of memory, CPU, console
FORTRAN 5	Superset of FORTRAN IV; runs under RDOS or MRDOS; requires 28K wds of memory, CPU, console
ALGOL	Extended ALGOL 60; runs under RDOS or MRDOS, or stand-alone; requires 12K wds of memory, CPU, console
BASIC	2 versions of Dartmouth BASIC; 1 for single-user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions; require 4K, 8K, and 16K wds of memory, respectively, CPU, console
Utilities	Text editor, library, loaders, debuggers

tems can run on the Nova 3 by trapping Eclipse instructions that have not been implemented on the Nova 3 and emulating them in software. Peripherals common to Nova, Supernova, and Eclipse systems can be attached to the Nova 3.

Communications software includes emulators for IBM 2780 terminals and HASP workstations.

MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; 8 in Canada; 3 each in France, England, and Spain; 5 in West Germany; 2 in Australia; and 1 each in Austria, the Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in Paris, France; Frankfurt, West Germany; London, England; Hull, Canada; and East Hawthorne-Melbourne, Australia.

Customer support includes up to ten customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software to users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special Nova 3 computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high-priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

TYPICAL PRICES

Model Number	Description	Purchase Price $	Monthly Maint. $
	Nova 3/4 Computer, includes chassis with 4 slots and either MOS or core memory		
8478	With 4K words of MOS	2,600	38
8479	With 4K words of MOS with parity	3,700	36
8480	With 8K words of MOS	3,200	46
8481	With 8K words of MOS with parity	4,500	44
8482	With 8K words of core	3,700	50
8483	With 16K words of MOS	4,400	56
8484	With 16K words of MOS with parity	6,100	54
	Nova 3/12 Computer, includes chassis with 12 slots for memory or I/O controllers and either MOS or core memory		
8486	With 4K words of MOS	3,600	44
8487	With 4K words of MOS with parity	4,700	42
8488	With 8K words of MOS	4,200	52
8489	With 8K words of MOS with parity	5,500	50
8490	With 8K words of core	4,700	56
8491	With 16K words of MOS	5,400	62
8492	With 16K words of MOS with parity	7,100	60
8493	With 16K words of core	6,200	66
8494	With 32K words of MOS	8,100	102
8495	With 32K words of MOS with parity	10,800	98
	Memory Management Unit, 8533 Subassembly Board, 8530 Automatic Program Load, and 8531 Power Fail/Automatic Restart		
8496	With 32K words of core	9,700	110
	Configured Systems, Nova 3/12, with 8535		
8500	With 32K words of MOS and 8532 battery backup	11,400	127
8501	With 32K words of MOS with parity, 8536 Parity Control, and 8532 Battery Backup	13,900	124
8502	With 32K words of core	12,500	135
	Nova 3 Options		
8020	Floating Point Unit	4,000	32
8530	Automatic Program Load	400	2
8532	Battery Backup	500	10
8533	Option Subassembly	200	2
8534	Multiply/Divide	1,400	12
8535	Memory Management Unit	2,800	28
8536	Parity Control	500	5
8537	Expansion Chassis for 3/12 only	2,000	20

Note: Nova 3 uses the same peripherals as the other Nova computers.

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OVERVIEW

Data General's Nova and Supernova product line includes 10 Nova systems (Nova, Nova 800, 800 Jumbo, 820, 830, 840, 1200, 1210, 1220, and 1230) and two Supernova systems. The Nova/Supernovas are small-scale, general-purpose, 16-bit computers, oriented toward control, scientific, laboratory, and time-sharing applications.

All of the systems currently marketed are upward compatible and differ mostly in memory speed, price, and packaging. All use the same mass storage units, peripheral devices, and software. The Novas utilize core memories in their basic configurations but can support both read-only memory (ROM) and core memory on a single system. The Supernovas utilize core or read/write semiconductor memory in basic system configurations (a Supernova system with semiconductor memory is called Supernova SC). In addition, each can support a combination of ROM, core, and read/write semiconductor memories.

Core memory cycle time is 800 nanoseconds for the Nova 800, Nova 800 Jumbo, Nova 820, Nova 840, and Supernova, 1.0 microseconds for the 830, and 1.2 microseconds for the Nova 1200, 1210, 1220, and 1230. The Supernova SC has the fastest cycle time: 300 nanoseconds. The first Nova, which is available but no longer marketed, has a cycle time of 2.6 microseconds.

The original members of the product line were the Nova and Supernova systems. As the 1200 Series, 800 Series and Supernova SC were added to the line one at a time, they had clearcut differences in performance. However, Data General has responded to the needs of its user community by adapting options originally aimed at the top of the line (as it was defined at a particular point in time). In this way, most users could benefit.

The high-speed data channel is a case in point. Originally it was an option available only for the two Supernovas. This fact, coupled with the Supernovas' greater memory speeds, made them clearly the top of the line. Now differences between the Nova 800 and Supernova processors have been considerably leveled. In fact, the high-speed data channel is standard for all Novas (still optional on Supernova). The Nova 830 and 840 (which are 800 Jumbos with memory management and protection) are the only models able to expand main memory to 128K words through the new memory management and protection unit.

The memory for the 1200 line (cycle time: 1,200 nanoseconds per word) is available in modules of 4K, 8K, and 16K words. Memories for the 800 line are available in modules of 4K and 8K words for the Nova 800 and 820. The 8K-word module is also available for the Nova 840. The 16K-word module for the Nova 830 has a 1.0-microsecond cycle time.

In addition to 2K, 4K, 8K, and 16K core increments, Novas can increment core with 1K-word modules but Supernova cannot; on the other hand, read/write semiconductor memory increments of 256, 512, and 1,024 words are available only for the Supernova.

There are still a few differences among the 800, 1200, and Supernova Series other than memory speeds, but these are not as distinctive as the capabilities that set the Nova "mapped" 830 and 840 apart from the rest of the line. The memory allocation and protection option, available to all of the Supernova and Nova 800 Series but not to the Nova 1200 Series, functions in a limited way like the 830/840 memory management and protection unit by mapping up to 32K words of memory for time sharing. Tables 1 and 2 list current similarities and differences between Nova and Supernova processors.

The Dual Nova computer system is a dual-processor/shared-disc system, built around two or three standard Data General computers (Nova 1200 Jumbo and Nova 830 or 840), one moving-head or fixed-head disc, and the Real-Time Disc Operating System (RDOS).

The advantages of a dual-processor configuration are continual system availability even when one processor is down, plus shared program and data-base files. The first processor can gather and reduce incoming data and monitor real-time operations. The second processor, used in the background mode, can develop new programs or carry out batch processing. Using the Multiprocessor Communications Adapter (MCA), processors can access each other through the I/O bus.

Where high throughput and continuity are prime considerations, the dual-processor system can handle many communication lines and data rates that peak at unpredictable times. The first processor stores or forwards messages to the second processor for peak times. The second processor shares the message load (doubling throughput), handles peak data rates, and controls the switching if the

Table 1. Data General Nova and Supernova: Common Characteristics

PROCESSOR	
Power Monitor/Auto Restart	Opt
No. of Instructions	202
Hardware Registers	2
Memory Registers	16
Hardware Accumulators	4
Word Size (bits)	16
Decimal Arithmetic	No
Floating-Point Hardware	Opt
I/O	
Max Devices Addressable	62
Programmed I/O	Yes
DMA Channel	Yes
Interrupt Levels	16
MEMORY	
Min ROM (wds)	256
Max ROM (wds)	31,744
Parity	No
ROM increments (wds)	256; 512; 1,024
SOFTWARE	
Assemblers	3
DOS, RDOS, SOS, RTOS	Yes
Compilers	
FORTRAN	Yes
ALGOL	Yes
Interpreter	
BASIC	Yes

first processor is down. The second processor can also accumulate network statistics, compile management reports, and generate customer service charges.

In a time-sharing situation where common access to programs is needed yet file protection is required, each processor functions as an independent time-sharing system. All terminals can handle Extended BASIC.

For customer service scheduling, the first processor controls the terminals and gathers the customer service requests. The second processor analyzes the data, bills the customers, and performs engineering calculations in batch mode. It also aids the first processor in peak times.

Data General states that the Dual Nova is well suited for supervisory control, front-end processing, data acquisition, point-of-sale systems, hospital patient monitoring, and data entry.

Along with processor development, Data General continues to fill out its line of available mass storage units and peripheral devices and to enhance its software support for the Nova and Supernova. Currently, the firm offers a variety of models and well-integrated hardware and software packages for its minicomputer systems. The company began manufacturing peripherals with the introduction of the Novadiscs, which are a series of fixed-head disc drives with capacities ranging from 128K to 768K words. To date, Data General has added a series of cassette drives, magnetic tape drives, 6013 high-speed paper tape reader, and two CRTs (the 6010 and 6012) to its roster of in-house peripherals. The company also manufactures its own cores.

Data General has developed comprehensive software that will run on both the Nova and Supernova under two types of disc operating systems that have file handling capability. Both disc operating systems, DOS and RDOS, control relocatable assemblers; loader math library; BASIC, ALGOL and FORTRAN compilers; text editor; symbolic debugger; and command line interpreter. DOS was previously the basic operating system. The newer RDOS, a real-time disc operating system, has all of the facilities of DOS as well as foreground/background processing plus multiprocessor and shared disc capabilities. RDOS is now the basic operating system. Subsets of RDOS, called SOS and RTOS, are also available for small stand-alone systems without disc. All of the operating systems will support one of two BASIC interpreters, one for a single user and one for up to 32 time-sharing users. ALGOL 60, and FORTRAN IV can run stand alone or

Table 2. Data General Nova and Supernova: Differences between Models

Characteristic	Nova	Nova 800, 820, 800 Jumbo	Nova 830	Nova 840	Nova 1200, 1230	Nova 1210, 1220	Supernova	Supernova SC
PROCESSOR								
Auto Program Load	–	Opt	Opt	Opt	Opt	Opt	Std	Std
Total Subassembly Slots	7	7; 10; 17	17	17	7; 17	4; 10	7	11
MEMORY								
Capacity (K wds)	32	32	128	128	32	24; 32	32	32
Core Increments (wds)	1; 2; 4; or 8K	1; 2; 4; or 8K	16K	8K	1; 2; 4; or 8K	1; 2; 4 or 8K	2; 4; or 8K	2; 4; or 8K
Read/Write SC Memory Increments (wds)	–	–	–	–	–	–	–	256; 512; 1,024
Memory Protect	–	Opt	Opt	Std	–	–	Opt	Opt
Memory Management	–	–	Opt	Std	–	–	–	–
SPEED								
Core Cycle (μsec)	2.6	0.8	1.0	0.8	1.2	1.2	0.8	0.8
SC Cycle (μsec)	–	0.8	–	0.8	1.2	1.2	0.3	0.3
Interrupt Response Time (μsec)	40.0	11.0	–	11.0	17.8	17.8	9.8	9.8
Transfer Rates (K wds/sec)								
DMA	285	1,250	–	1,250	833.3	833.3	500	500
High-Speed Data Channel	–	1,250	–	1,250	–	–	1,250 (opt)	1,250 (opt)

under DOS or RDOS. RDOS also supports a macro assembler and Fortran 5 (a superset of ANSI FORTRAN, IBM Level H FORTRAN, and Univac FORTRAN V). FORTRAN 5 is designed to optimize a user's entire program so that its efficiency compares to a program written in assembly language.

Multiply/divide and floating point are options available to all processors either as hardware units or as software subroutines.

In addition, Data General provides three cross-assemblers to prepare Nova/Supernova programs on the IBM System 360/370, Univac 1108, and CDC 6600 computers. These assemblers are written in FORTRAN and are compatible with the Nova/Supernova extended assembler.

Data General announced the first Nova in September 1968 and the first Supernova in August 1969. Substantial price cuts for the Supernova were made in September 1970. In October 1970, Data General introduced the Nova 800 and 1200 and the Supernova SC memory modules. In May 1971, the Nova 800 and 1200 Jumbos (subsequently the designation for the 1200 Jumbo was changed to Model 1230) were announced. The Nova 820, 1210, and 1220 were announced on November 10, 1971. The Nova 840 was shown at the Fall Joint Computer Conference in December 1972. Recently, (fall 1974) Data General announced that the 830 combines new lower-cost memory modules in the 840 configuration.

COMPETITIVE POSITION

The Nova/Supernova line has been Data General's mainstay for the last few years. It has held its own against stiff competition from companies like Digital Equipment, Hewlett-Packard, General Automation, Honeywell, and Varian. Although the company introduced the microprogrammed Eclipse line in 1974 to replace the Nova/Supernova line and to extend the market upward for Data General computers, the company still plans to keep the Nova/Supernova line current for awhile. Thus Model 830 and a series of lower-cost memories have been introduced to reduce the cost of all systems.

In the development of its systems, Data General has consistently utilized the latest technology to improve the price/performance of its systems; all have the same basic logical design as the first Nova. Thus, all software developed for previous models is compatible with new models, even the new Nova 2 and Eclipse systems, which are compatible in most respects and thus can build on the Nova/Supernova software base. The firm steadily continues to develop system software, and the available software is substantial.

Data General has a large OEM and end-user customer base, which is necessary to support continued system development. An increasing number of small business computer manufacturers are using Nova/Supernova processors as the heart of their systems. In addition, the ROLM Corporation builds a Ruggednova for military applications, and licenses the Nova/Supernova software for it.

Data General claims to be number 2 in minicomputer sales and deliveries, having shipped more systems than any other manufacturer except Digital; the company has a firm grip on around 15 percent of the market. This sales record results from Data General's aggressive marketing combined with its ability to produce and deliver systems with attractive price/performance ratios. Data General markets its systems for all minicomputer applications.

A good mix of hardware/software is available for Nova and Supernova minicomputers. The peripherals equipment complement compares quite favorably to that of competitors (particularly noteworthy is the assortment of disc units, the communications subsystems, and the special peripherals associated with numerical control). The Novadisc was Data General's first peripheral; the company now also manufactures the 6013 High-Speed Paper Tape Reader, the 6010 and 6012 CRT Displays, magnetic tape drives, and the Novacassette.

Nova/Supernova's DOS and RDOS operating systems are versatile in their support of an assembler; BASIC, FORTRAN, and ALGOL compilers; and a command language interpreter. RDOS is noteworthy for its ability to handle dual processors combined with a shared-disc environment and multiprocessor networks.

Data General has experienced some inroads on its Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. Digital Computer Controls has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line because the expandability of the system allows memory sizes equal to the Nova 830 and 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically, the popularity of the Nova/Supernova line has been part of Data General's problem; underestimating demand caused the company to slip behind schedule from time to time in the past, and impatient OEM customers bought from the smaller company. This threat is really counteracted more by the Nova 2 (OEM) line, which is competitive in price and comparable in speed. Meanwhile, addition of the Eclipse line, extending into the upper end of the market, provides an attractive upward path for users who anticipate growing systems needs.

Thus, Data General's recent announcements at the upper and lower ends of the market, consistent with the continuing expansion of the Nova/Supernova hardware and software base, put the firm in an aggressive posture

across the entire range of the minicomputer market. Indications are that Data General can hold its own in the marketplace and gradually increase its share at the expense of the weaker, smaller minicomputer manufacturers.

User Reactions

The Data General users interviewed predictably exhibited a wide range of applications and systems sizes as well as a range of reactions to the system.

Installations included a software house with a number of accounting, inventory, order entry, and forecasting systems installed among its customers; a ship voyage accounting firm; a university physics laboratory; and an investment firm.

All users interviewed felt the system was very reliable. One OEM user, a software service bureau with a number of systems, remarked that he had "blown" only two 8K-word core boards in 2 years; other than that, he has had no downtime. Remarks about service showed more variety; several users of various size systems said it was fine; one user said it was excellent (2-hour response time during emergency), while another (small) user reported problems with slow response. The dissatisfied user remarked that several other small users in his area with down systems had occasionally come to "borrow" his system during off-hours. Although this added to his impression of slow service, he added that the system was very reliable and he had no complaints on that score.

User reactions to Data General software were generally positive. A user of RDOS Version III on three Nova 800s (32K words of core each) had previously used DOS 5 but switched operating systems because of the type of file-handling capabilities and the new editing commands; he was quite satisfied with the change. Other users had no complaints about the way Data General's software functioned. One small user, with a 12K-word Nova 1200 system without disc, mourned that Data General's software development appeared to be aimed at larger disc-based systems and nothing seemed to come in his direction. One user stayed with FORTRAN IV rather than buy the additional memory needed for FORTRAN 5; he said his application was I/O-bound not compute-bound, so he did not need optimized code.

CONFIGURATION GUIDE

A basic Nova/Supernova central processor includes four accumulators (two of which can be used as index registers); a single-line, 16-level priority interrupt system; a programmed I/O channel; and a direct memory access (DMA) channel. Supernova processors also include an automatic program load feature initiated from the console; automatic program load is an optional feature for the Nova 800 and 1200 Series. The basic processor includes only add and subtract arithmetic operations; hardware multiply/divide and floating point can be added as options. Each central processor unit is rack mountable or fits in a tabletop enclosure. Table 2 shows the differences in processor submodels.

Working storage for all the Nova/Supernova processors is provided by storage modules that can be added in any combination up to a maximum size of 32,768 words (131,072 words for the Nova 830 and the Nova 840 with a memory management and protection option). All use magnetic core memory except the Supernova SC, which uses semiconductor memory. In addition, read-only memory (ROM) modules are available in 256- to 1,024-word modules. ROM modules and core memory modules can be added in any combination, but total memory size cannot exceed 32,768 words without the memory management and protection option.

Up to 58 I/O devices can be connected to a Supernova and 61 to a Nova. All devices connect to the programmed I/O channel for the transfer of control information. Slow-speed devices such as console typewriters, punched card, paper tape, and line printers also use the programmed I/O channel for data transfers. High-speed devices, such as magnetic tape and disc, transfer data via the DMA channel or via the high-speed data channel if included in the system. Table 3 lists the various models of peripheral devices available.

Table 3. Data General Nova and Supernova: Peripherals

Device Model	Description
Discs	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K-wd capacity
6000 Series	Nova Discs (fixed-head), 128K, 256K, 512K, 768K-wd capacity
4048A	Century 111, 3M-wd capacity, IBM 2311 compatible
40578	Century 114, 12M-wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M-wd capacity
Magnetic Tape	
4030 I-N	Wang magnetic tape transports, 7/9-trk, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-drive versions
6020 Series	7/9-trk dual-head, 75 ips, up to 8 drives/controller
4080 Series	Cassette subsystem, 50K wds/cassette, single/dual triple transports, 7 to 8 transports/controller
Consoles	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
Paper Tape	
4011/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
Punched Card	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cps
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm
Printers	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps

Table 3. (Contd.)

Displays	
6010/6012	24 lines, 80 char each, local edit (6012)
4010	Infoton Vista, 20 lines, 80 characters each
A/D, D/A Systems	
4032	Basic A/D Interface, models 4055 A/Q converters, 8 to 15 bits; multiplexors, 2 enclosures (128-single-ended channels, 64 differential)
4037	Basic D/A control, models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters
4085	Wide-range analog input, up to 512 channels, 13 to 15 bits
Plotters	
4017 A-D	CalComp 565 drum or rack mountable 563 drum, and 502 flatbed plotters
4017E	General Interface Board
Digital 4065	I/O interface subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-Ipm feed
4008/4079	Real-time clocks, 10/100/1,000-Hz frequencies
4040	General Interface Board
Communications	
4015	High-speed controller, 600-50,000 baud
4025	IBM 360/370 interface
4038	Multiprocessor communications adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async controller subsystem, up to 1,024 lines

Dual Nova multiprocessor configurations are hardware and software supported. Each processor has 64K bytes of memory and an interprocessor bus for communication between computers. High-level languages and utility software are included. Under RDOS, both computers have on-line access to programs and data files. Hardware-multiplexed data paths allow access to the data base and programs by both processors. Each processor is independent, but both share the same disc data base.

Three types of disc storage available for the Dual Nova configuration are as follows:

- Fixed-head Novadiscs — 256K to 1,536K-byte capacity; up to 8 million bytes of Novadisc storage used for a Dual Nova configuration; provides fast access.
- Moving-head disc with cartridge drives — Removable cartridge model with 2.49 million-byte capacity; one fixed and one removable disc unit with 4.9 million-byte capacity; up to 20 million bytes shared in a Dual Nova configuration; convenient mass storage.
- Moving-head disc pack drives — 24.944 million-byte capacity; almost 200 million bytes accessible in a Dual Nova configuration.

Combinations of fixed and moving-head discs can be used in configurations. Maximum disc storage is obtained with eight moving-head disc packs (200 million bytes) and 8 million bytes of fixed-head storage.

Communication between the two processors is handled via the interprocessor bus. The bus consists of the following components:

- Buffer — Under control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors both request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — This part carries the data for inter-computer communication.
- Dual 1-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The MCA interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of 1 million bytes per second. These types of multiprocessor network configurations are software supported under RDOS.

Software packages and the minimum configurations required are listed in Table 4.

COMPATIBILITY

All Nova/Supernova processors are compatible and use the same instruction set as well as the same peripheral and mass storage devices. All currently available software can run on all the Nova/Supernova computers, if the processor can support the required configuration. Software for mapped systems, for instance, must run on an 830 or 840. Cross-assemblers are available so that users with an IBM System/360 or 370, Univac 1108, or CDC 6600 can utilize their more powerful processing capabilities to assemble Nova/Supernova programs. Nova 2 processors are completely compatible with the small processors at the low end of the line.

The Eclipse computer is generally program-compatible with the Nova/Supernova line, given comparable configurations; there are only a few restrictions. Eclipse computers have implemented multiply/divide, hardware floating point, and memory management options differently. In the first two cases the difference is chiefly a matter of coding, which is easy to change. But, memory management is more difficult to alter. Eclipse also uses the codes for "no-load" and "no skip" Nova options for the standard set, so Nova programs with these instructions are not compatible. A compatible program cannot

Table 4. Data General Nova and Supernova: System Software

Package	Description
RDOS	Real-time disc operating system, foreground/background multiprocessing, multiprogramming; requires 16K words of memory, CPU, 2.5M disc, console
RTOS	Small basic, real-time, executive; requires 4K words of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette, mag tape, card or paper tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV; runs under RDOS and SOS; requires 8K words of memory, CPU, console
FORTRAN 5	Superset of FORTRAN IV; runs under RDOS; requires 28K words of memory, CPU, console
ALGOL	Extended ALGOL 60; runs under RDOS or is stand-alone; requires 12K words of memory, CPU, console
BASIC	2 versions of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions; require 4K, 8K, and 16K words of memory, respectively, CPU, console
Utilities	Text editor, library, loaders, debuggers

contain the data channel increment, add-to-memory feature, or execution- and I/O-time-dependent subroutines.

All three computer lines use the same type of I/O bus structure; thus all Nova/Supernova peripherals can attach to Eclipse and Nova 2 computers.

MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in France (Paris), West Germany (Frankfurt), England (London), Canada (Hull), and Australia (East Hawthorne-Melbourne). Customer support includes 2 to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers that help users apply their systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software for users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special Eclipse computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. For a monthly charge, a factory service contract allows equipment to be rapidly fixed at a repair depot. On-call service contracts provide preventive maintenance checks and high-priority emergency service to the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSORS AND WORKING STORAGE		
4001	Nova Processor	3,950	34
	Nova Options		
4006	Power Monitor and Auto Restart	400	1
4022	External I/O Cable Connector	250	NC
4024	Expansion Chassis	1,850	10
4031	Multiply/Divide	2,000	16
	Nova Memories (16-bit words; 2.6-μsec cycle time)		
4003	4,096-Word Core Memory	3,650	28
4004	2,048-Word Core Memory	2,700	20
8016	8,192-Word Core Memory	4,100	32
	Nova 800 Processor		
8230	With 4K Words of Core Memory	6,600	53
8231	With 8K Words of Core Memory	8,000	64
8232	With 16K Words of Core Memory	11,200	99
8233	With 24K Words of Core Memory	14,400	134
8235	Jumbo, with 4K Words of Core Memory	7,450	60
8236	Jumbo, with 8K Words of Core Memory	8,850	71
8237	Jumbo with 16K Words of Core Memory	12,050	106
8238	Jumbo with 24K Words of Core Memory	15,250	141
8239	Jumbo with 32K Words of Core Memory	18,450	176
	Nova 820 Processors (with 7 additional subassembly slots)		
8253	With 4K Core Memory	6,100	63
8254	With 8K Core Memory	7,500	74
8264	With 16K Core Memory (2 8K modules)	10,700	109
8285	With 24K Core Memory (3 8K modules)	13,900	144
8286	With 32K Core Memory (4 8K modules)	17,100	179
	Nova 800/820 Processor Options		
8139	Turn-key Console	100	NC
8159	Turn-key Console	125	NC
8206	Power Monitor and Auto Restart	400	1
8207	Nova 800/820 Multiply/Divide	1,000	8
8208	Automatic Program Load	400	2
8209	Memory Protection and Allocation (for Nova 800 only)	3,500	28
8222	External I/O Cable Connector (for Nova 800 only)	250	NC
8224/5	Expansion Chassis	1,850	10
8281	Expansion Chassis (adds 10 I/O subassembly slots)	1,850	10
	Nova 800/820 Memories		
	Core Memory		
8268	4K Words	2,500	24
8269	8K Words	3,200	35
	Semiconductor Read-Only Memory		
8226/77	256 Words	900	9
8227/78	512 Words	1,450	13
8228/79	1,024 Words	1,950	20
	Nova 840 Processors		
8264	With 16K Words of Core Memory (expansion to 64K words)	16,530	134
8265	With 16K Words of Core Memory (expansion to 64K words; wiring only for memory management and protection; includes 2025 jumper card)	13,230	106
8290	With 24K Words of Core Memory (expansion to 64K words)	19,730	169
8291	With 32K Words of Core Memory (expansion to 64K words)	22,930	204
8292	With 40K Words of Core Memory (expansion to 64K words)	26,130	239
8293	With 48K Words of Core Memory (expansion to 64K words)	29,330	274
8294	With 64K Words of Core Memory (expansion to 80K words)	35,730	344
8295	With 80K Words of Core Memory (expansion to 128K words)	45,130	438
8296	With 96K Words of Core Memory (expansion to 128K words)	51,530	508
8297	With 128K Words of Core Memory	64,330	648
8298	With 24K Words of Core Memory (wired for memory management and protection only)	16,430	141
8299	With 32K Words of Core Memory (wired for memory management and protection only)	19,630	176
	Nova 840 Memories		
8269	Core Memory (8K words)	3,200	35
	Nova 840 Processor Options		
8206	Power Monitor and Auto Restart	400	1
8207	Multiply/Divide	1,000	8
8208	Automatic Program Load	400	2
8021	Memory Management and Protection Unit	3,500	28
8222	External I/O Cable Connector	250	NC
8224	Expansion Chassis (adds 7 I/O subassembly slots)	1,850	10
8283	Memory and I/O Expansion Chassis (provides 15 additional slots)	3,000	34
	Nova 830 with Memory Management and Protection Option		

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
8244	With 16K Words of Core Memory	12,650	NA
8245	With 32K Words of Core Memory	16,150	NA
--	With 64K Words of Core Memory	23,150	NA
--	With 16K-Word Memory Board (1.0-μsec cycle time)	3,500	
	NOVA 1200		
	Nova 1200 Processors		
8182	With 4K Words of Core Memory	5,100	40
8183	With 8K Words of Core Memory	5,950	52
8184	With 16K Words of Core Memory	7,550	64
8185	With 24K Words of Core Memory (1 16K module and 1 8K module)	9,550	96
8186	With 32K Words of Core Memory (2 16K modules)	11,050	108
8187	Jumbo with 4K Words of Core Memory	5,950	44
8188	Jumbo with 8K Words of Core Memory	6,800	56
8189	Jumbo with 16K Words of Core Memory	8,400	68
8190	Jumbo with 24K Words of Core Memory	10,400	100
8191	Jumbo with 32K Words of Core Memory	11,900	112
	Nova 1200/1210/1220 Memories •		
8120	4K-Word Core Memory	1,800	20
8121	8K-Word Core Memory	2,000	32
8117	16K-Word Core Memory	3,500	44
	Nova 1210 Processors		
8133	With 4K-Word Core Memory	4,000	40
8134	With 8K-Word Core Memory	5,400	59
8140	With 16K-Word Core Memory	7,000	71
8141	With 24K-Word Core Memory	9,000	103
8142	With 32K-Word Core Memory	10,500	115
	Nova 1220 Processors		
8153	With 4K-Word Core Memory	4,900	44
8154	With 8K-Word Core Memory	6,300	56
8165	With 16K-Word Core Memory	7,900	68
8166	With 24K-Word Core Memory	9,900	100
8167	With 32K-Word Core Memory	11,400	112
	Nova 1200/1210/1220/1230 Processor Options		
8106	Power Monitor and Auto-Restart	400	1
8107	Nova 1200/1210/1220 Multiply/Divide	1,600	13
8108	Automatic Program Load	400	2
8122	External I/O Cable Connector	250	NC
8124/5	Expansion Chassis (adds 7 I/O subassembly slots)	1,850	10
8139	Turn-key Console (provides start, continue, reset, and program load functions; for 1200 or 1210 series with 5.25-in. chassis)	100	NC
8159	Turn-key Console (same as 8139 but is for 1210 and 1220 series with 10.5-in. chassis)	125	NC
8181	Expansion Chassis (adds 10 I/O subassembly slots)	1,850	10
	Nova 1200/1210/1220 Memories		
	Semiconductor Read-Only Memory		
8126/77	256 Words	750	8
8127/78	512 Words	1,250	12
8128/79	1,024 Words	1,750	18
8001	Supernova Processor	5,600	54
	Supernova Options		
8006	Power Monitor and Auto-Restart	400	1
8007	Multiply/Divide	1,600	13
8008	Memory Allocation and Protection	3,500	28
8009	High-Speed Data Channel	950	9
8022	External I/O Cable Connector	250	NC
8024	Expansion Chassis (adds 7 additional slots)	1,850	10
8025	Supernova SC Memory Expansion Chassis	1,850	10
8003	4K-Word Core Memory	3,650	30
8015	8K-Word Core Memory	4,900	40
8012	1,024-Word Semiconductor Read/Write Memory	2,800	28
8013	512-Word Semiconductor Read/Write Memory	2,200	22
8014	256-Word Semiconductor Read/Write Memory	1,500	15
8015	8,192-Word Core Memory	4,900	40
8077	256-Word Semiconductor ROM	1,000	10
8078	512-Word Semiconductor ROM	1,550	14
8079	1,024-Word Semiconductor	2,050	21
	Option for All Nova/Supernova Processors		
8020	Floating-Point Processor	4,000	32
	Dual Nova 840 System		
9028	Part 1 consists of 8291 rack-mounted Nova 840 Computer (with 32,768-word core memory and memory management and protection unit, 8206 power monitor and auto restart, 8208 automatic program load, 4007 I/O interface subassembly, 4008 real-time clock, 4010 Teletype/video display I/O interface, 4119 precision crystal oscillator for 2,400 baud, 4011 paper tape reader control, 6013 high-speed paper tape reader, 4240 interprocessor bus, 4046 moving-head disc control, 4047 moving-head disc adapter and power supply, 4030 magnetic tape control, and 6 remaining slots in computer chassis)	36,550	784
9028A	Part 2 consists of 40101 20-Line, 80-Char Video Display, 1065F Interprocessor Bus Cable, 4047B Moving Head Disc Drive (with 2.494M-words capacity, 4047C disc cartridge, 4030J magnetic tape transport, and 1012G 2-bay rack cabinet)	19,300	784
9029	Part 3 consists of 8291 Rack-Mounted Nova 840 Computer (with 32,768-word core memory and memory management and protection unit, 8206 power monitor and auto restart, 8208 automatic program load, 4007 I/O interface subassembly, 4008 real-time clock, 4010 Teletype/video display I/O interface, 4240 interprocessor bus, 4046 moving head disc control, and 7 remaining slots in computer chassis)	28,700	784
9029A	Part 4 consists of 4010A Teletype Model 33 ASR Keyboard/Printer, EC4047 Moving-Head Disc Adapter and Power Supply Cable, IC4011 Paper Tape Reader Control Cable, IC4030 Magnetic Tape Control Cable and Major Portion of Supplied Software on Magnetic Tape	2,750	784

HEADQUARTERS

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DIGITAL COMPUTER CONTROLS INC.

16 Series System Report

OVERVIEW

The Digital Computer Controls "16 Series" consists of upward-compatible systems that range from microcomputer-sized systems to midicomputers. The earliest models of the series are the LSI/MSI D-116 systems, which started out as Nova replacements. Hardware options combined with new software soon allowed them to compete in a wider marketplace. The recent additions of the microprogrammed LSI D-216, D-316, and D-416 at the bottom of the line and the D-616 midicomputer at the top of the line have expanded competition across the entire range of the minicomputer market.

The success of the company's early approach to the minicomputer market was demonstrated fairly quickly after the firm was formed in 1970. D-112, the first product delivered in August 1970, was compatible with the Digital Equipment PDP-8. By the end of fiscal 1972, Digital Computer Controls (DCC) had delivered more than 400 D-112 systems, started production of the D-116, which was compatible with the Data General Nova 1200, and acquired several subsidiaries. Also, the company was profitable, in spite of the onset of litigation with Data General. To date, the company has delivered more than 750 D-112 systems and 5,000 D-116s. Deliveries of the first models in the new 16 Series began in the last quarter of 1975.

DCC's D-116 Series is program- and interface-compatible with the Data General Nova 1200 Series (Models 1200, 1210, and 1220); options available for the D-116 are similar to those available for the Nova 800 and Supernova systems. Table 1 lists the processor characteristics common to both the D-116 and the Data General Nova/Supernova. Table 2 compares DCC models with specific Data General systems. Both D-116 models use medium- and large-scale integrated circuits to produce a processor on a single circuit board. Core memory units are also compact; the 1,200-nanosecond core memory for the D-116 includes 16K words on a single board. A 16K-word memory board is unavailable for the higher-speed D-116H system — a maximum of 8K words of 960-nanosecond core memory is on a single board.

Table 1. Processor Characteristics Common to DCC 16 Series and Data General Nova/Supernova

PROCESSOR	
Power Monitor/Auto Restart	Opt
No. of Instructions	202
Hardware Registers	2
Memory Registers	16
Accumulators	4
Word Size (bits)	16
Decimal Arithmetic	No
Hardware Multiply/Divide	Opt
I/O	
Max Devices Addressable	62
Programmed I/O	Yes
DMA Channel	Yes
Interrupt Levels	16
MEMORY	
Min ROM (wd)	256
Max ROM (wd)	31,744
Parity	No
ROM Increments (wd)	256; 512; 1,024
SOFTWARE	
Assembler(s)	Yes
Mass Storage Operating System or Systems	Yes
Real-Time Executive or Operating System	Yes
Basic Interpreter(s)	Yes

The three low-end LSI systems, D-216, D-316, and D-416, are slower than the D-116; they are available as a computer-on-a-board with memory (15 x 15 inches) as well as a full-fledged minicomputer system. D-216 is available with 12K words of RAM and 4K words of PROM/ROM. D-316 supports up to 32K words of MOS RAM. D-416 is a core-only system with up to 32K words of memory. The D-316 or D-416 computer-on-a-board offers 32K words of memory along with the CPU, power monitor/auto restart, automatic program load, and a teletypewriter interface. Byte-parity checking is also standard on the D-316 MOS RAM.

As the new high-end system of the 16 Series, the D-616 can support up to 2M bytes of core or MOS RAM

HEADQUARTERS

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Table 2. DCC D-116 Series Compared with Data General Nova/Supernova

Characteristic	Nova	Nova 800, 820, 800 Jumbo	Nova 830, 840	Nova 1200, 1230	Nova 1210, 1220	Super-nova	Super-nova SC	DCC 116S	DCC 116H
PROCESSOR									
Auto Program Load	–	Opt	Opt	Opt	Opt	Std	Std	Opt	Opt
Total Subassembly Slots	7	7; 10; 17	17	7; 17	4; 10	7	11	4; 7; 10, or 17	4; 7; 10, or 17
Floating-Point Hardware	Opt	Opt	Opt	Opt	Opt	Opt	Opt	No	No
MEMORY									
Capacity (K wd)	32	65	128	65	24; 65	65	65	128	128
Core Increments (wd)	1,2,4	1,2,4	8K	1,2,4	1, 2, 4	2, 4, or 8K	2, 4, or 8K	4, 8, or 16K	4 or 8K
Read/Write SC Memory Increments (wd)	–	–	–	–	–	–	256;512; 1,024	–	–
Memory Protect	–	Opt	Std	–	–	Opt	Opt	Opt	Opt
Memory Management	–	–	Std	–	–	–	–	Opt	Opt
SPEED									
Core Cycle (μsec)	2.60	0.80	0.80	1.20	1.20	0.80	–	1.20	0.96
SC Cycle (msec)	–	0.80	0.80	1.20	1.20	0.30	0.30	–	–
Interrupt Response Time	40.00	11.00	11.00	17.80	17.80	9.80	9.80	–	–
Transfer Rates (K wd / sec)									
DMA	285	833	833	833.3	833.3	500	500	833.3	**833.3**
High-Speed Data Channel	–	1,250	1,250	–	–	1,250 (opt)	1,250 (opt)	No	No
Programmed I/O	Std	Std	Std	Std	Std	Std	Std	Std	Std

with a cycle time of 660 nanoseconds. To maintain high throughput, the D-616 memory modules have dual ports and are 2-way interleaved. Memory above 128K words is arranged in up to four external banks. A memory mapping and protection unit similar to that used for the D-116 is required for systems with more than 32K words of memory. Up to 128K words of memory can be housed in the mainframe chassis using a new 32K-word (64-byte) memory board.

The D-616 uses a separate I/O processor, so an I/O transfer rate of 3M bytes per second can theoretically be maintained concurrently with processing, if the I/O channel and the CPU are using separate memory modules. Table 3 compares the system specifications of all five models in the 16 Series.

DCC's peripherals closely parallel Data General's. Data General offers few items that are unavailable from DCC, although the latter's software is not yet comparable. Data General has an extremely large body of software, which is partly responsible for the popularity of the Nova/Supernova series; but DCC is working steadily to narrow the gap. DCC operating systems include MSOS (Mass Storage Operating System), IRIS (Interactive Real-Time Information System), and RTX (Real Time Executive); while language processors include extended FORTRAN IV ("FORTRAN 74"), Business BASIC, and assembly language. A COBOL compiler is scheduled for the end of 1975.

The steady expansion of its software base means that DCC can gain an increasing proportion of revenues from end users instead of marketing only to OEM manufacturers. The software base has grown substantially since the company's inception and now is at the point where 16 Series is a serious contender for the minicomputer dollar on its own merit.

DCC markets its systems directly through eight sales centers in the United States and through a number of sales representatives in the United States, Canada, Mexico, Europe, and other parts of the world. U.S. sales representatives include Datatron, Barnhill, Inland Associates, A & D Devices, Computer Complements, Deerland Distributers, Randal Data Systems, Rush S. Drake Associates, and Aloha Associates (Hawaii). Transword Data Systems markets the system in England and France; Aheam & Soper in Canada; Techmation in the Benelux countries; Teleprint in Germany, Austria, and Switzerland; Datatek in Finland; and Control Proceso Electronics in Israel, Greece, Turkey, and Iran.

In addition to the D-112 and 16 Series, DCC makes a memory expansion unit (add-on memory) that allows Digital Equipment's PDP-8L to be expanded from 4K to 32K words. DCC also produces a POS register and several other minicomputer-controlled devices.

COMPETITIVE POSITION

Without creating much of a stir, except perhaps in Data General's headquarters in Southboro, Massachusetts, DCC has quietly delivered over 5,000 D-116 computers. Customers include more than 250 OEMs and about 250 end users.

The D-116 has, to judge from the rate of deliveries, become one of the most popular minicomputers on the market. DCC claims it ranks third in number of minicomputer systems shipped per month; only Digital Equipment and Data General ship more. A large number

Table 3. DCC 16 Series: Mainframe Characteristics

Characteristics	D-116	D-216	D-316	D-416	D-616
CENTRAL PROCESSOR					
Microprogrammed	No	Yes	Yes	Yes	Yes
Control Memory	No	ROM	ROM	ROM	ROM
No. of Registers	4	12	12	12	12, with 4 used as index registers
Word Length	16 bits	16 bits	16 bits	16 bits	16 bits
Addressing					
Direct	To 64K bytes	To 32K bytes	To 64K bytes	To 64K bytes	To 64K bytes
Indirect	Multilevel	Multilevel	Multilevel	Multilevel	Multilevel to 2M bytes
Indexed	Yes	Yes	Yes	Yes	Yes
Mapping	Yes, to 256 bytes	Yes	Yes	Yes	Yes, to 2 million bytes
Instruction Set					
Implementation	Firmware	Firmware	Firmware	Firmware	Firmware
Types	Singleword	Singleword	Singleword	Singleword	Singleword, double-word at user option
Number	59	98	98	98	96 with 16 more opt
Floating Point	No	No	No	No	Hardware option
Hardware Stack	No	Yes	Yes	Yes	Yes
Instruction Execution Times (μsec)					
Fixed Point					
Add	0.96 or 1.2	1.6	1.6	1.6	0.66
Multiply	3.0 or 3.8	Times currently unavailable.			5.17
Divide	3.2 or 4.1			NA	16.7
Floating Point	NA	NA	NA	NA	NA at this time; FPP opt
Add	—	—	—	—	—
Multiply	—	—	—	—	—
Divide	—	—	—	—	—
Writable Control Store	NA	NA	NA	NA	Opt; 1K x 50 bits
Interrupts					
Levels	Multilevel	Multilevel	Multilevel	Multilevel	Multilevel
Type	Hardware & software	Hardware & software	Hardware & software	Hardware & software	Hardware & software
MAIN STORAGE					
Type	Core, MOS, RAM, PROM	RAM, PROM, ROM	MOS RAM	Core	Core, MOS RAM, or MOS RAM with error detection & correction
Cycle Time (μsec)	0.96 or 1.20	1.6	1.6	1.6	0.66 for any type
Basic Addressable Unit	Word or byte	Word or byte	Word or byte	Word or byte	Word or byte
Bytes/Access	1 or 2	1 or 2	1 or 2	1 or 2	1 or 2
Cache Memory	No	No	No	No	No
Capacity (bytes)					
Min	128K*	2K	8K	8K	8K
Max	8K, 16K, 32K	24K, 128K*	64K; 128K*	64K; 128K*	2M
Increment Size (bytes)		2K	8K	8K, 16K, 32K, 48K, 64K	8K, 16K, 32K, 64K
Ports/Module	1	1	1	1	2
Error Checks	No	No	Byte parity	No	Error detection & correction
Memory Protection	Yes*	Yes*	Yes*	Yes*	Yes*
Memory Management	Yes	Yes	Yes	Yes	Yes
Interleaving	No	No	No	No	Yes, 2-way
INPUT/OUTPUT					
Max Devices Addressable	60	60	60	60	62
Programmed I/O	Yes	Yes	Yes	Yes	Yes
DMA	Std	Std	Std	Std	Std, with 2 speeds
DMA Transfer Rate (bytes/sec)	833,300	1,250,000	1,250,000	1,250,000	Low-speed = 1.6M (input); high-speed = 3M (input)

*With Memory Management unit.

of DCC customers buy OEM and do not want to disclose their transactions, so the system has not received the attention from end users that would appear to correspond to its sales record. As of February 28, 1975, DCC's gross sales of $9,756,140 were up 56 percent and profits doubled over the previous fiscal year. The company now has 8 sales and 12 service offices.

Although DCC no longer emphasized the Series 16's compatibility with Data General's Nova 1200, the press release on the D-616 did compare its cost with the Data General ECLIPSE. The price has been set about 20 percent below the ECLIPSE for comparable configurations. Other 16-bit systems with memory of more than 1 million bytes and enhanced I/O throughput schemes include Digital's PDP-11/70. Some competitive minicomputer systems use a larger word size, such as 24 bits (Harris) or 32 bits (Systems and Interdata), allowing more memory to be addressed directly. Interdata handles compatibility problems with the companies, 16-bit lines through various hardware and software machinations.

DCC compares its smaller 16 Series systems to Computer Automation's LSI configurations. Prices are comparable for small systems, but the 16 Series systems are cheaper when larger memories are included. In the microcomputer marketplace DCC systems also meet board-level computers made by Digital Equipment. Data General's new Nova 3 systems are competing for the same market. At the time of writing, DCC has an advantage in the large amount of memory it can fit on one board, which may be of interest to OEM customers with size restraints. Digital Computer Controls also provides substantial software for its systems. In fact, the company may have COBOL on its systems before some other larger minicomputer manufacturers make it available for their systems. Digital Equipment already has COBOL for the PDP-11/45 and 11/70 and General Automation has it for the GA-16Series.

DCC's new systems are well conceived to be competitive at both the bottom and top of the minicomputer market. They also compete favorably with Data General's comparable offerings. With over 250 OEM customers as well as about that many end users, the company has a considerable base to provide stability.

Our interviews to date indicate the OEM customers are satisfied with DCC as a supplier because the company caters to the market in a flexible way in order to meet customer needs. As the company grows, flexibility will become more difficult. However, any company that can deliver 5,000 computer systems without fanfare must be considered a serious market force.

User Reactions

Key/Disc System Manufacturer. One of the larger D-116 users is the manufacturer of a popular key/disc entry system. This user, who purchases around 600 systems a year, switched from Data General to DCC for a number of reasons. First, this manufacturer started making its own memories and DCC would sell its processor without a memory; Data General required some memory with its processor. In addition, the long lead time for the popular Data General Nova systems was difficult to accept. Since this key/disc company wrote all its own software from scratch (one of its strong points in the key/disc market), the amount of available software was of no consequence. The key/disc manufacturer is very pleased with the way the arrangement has worked out. The DCC D-116 proved to be compatible mechanically and electrically; no software alterations were needed; service is good; and DCC's accounting department has been responsive to any problems that arose. In addition, this user feels that DCC is attuned to buyers' problems.

POS System Manufacturer. Another large user, a manufacturer of point-of-sale equipment, uses a D-116 in each store to control the local terminals directly and at the central supervisory site to communicate with all the controllers in the branch stores. This user switched from Data General to DCC for two reasons: price and the D-116 power supplies, which this user feels are the best it has seen. A careful comparison of the reliability of the Data General and DCC systems in terms of number of man-hours spent to fix defects was made shortly after delivery; both manufacturers were rated good to very good. Data General had the edge over DCC, but the difference in the cost of the few extra man-hours on repair did not equal the amount saved on the DCC systems. This manufacturer found a slight incompatibility in the memory interfacing between its equipment and the DCC memory boards, but adjustment was very minor. The CPU board, I/O board, interfacing, and software were all completely compatible.

Turnkey Graphics System Manufacturer. A supplier of turnkey graphics systems is using the D-116 as a controller that replaces the Nova used in earlier systems. This company has used six D-116s so far and has found no problems with the software originally developed for the Nova. Interestingly, this firm had written all its own software from scratch. The company turned to DCC as its supplier when Data General began having trouble meeting delivery commitments due to the unanticipated volume of business in Novas and Supernovas (the demand for the 800 is apparently particularly out of line with projections). DCC promises faster deliveries and has lived up to commitments. Most of the graphics systems use 32K words of core and an assortment of discs and other peripherals to support the displays. This user was quite happy both with the way the system performed and with service — the only complaint was that the racks for the tape drives bent because they were not sturdy enough for the weight they held.

CONFIGURATION GUIDE

The basic 16 Series processors differ in number of boards required by CPU and memory; some can be purchased at the board level without a chassis. The number of boards per system are as follows:

- D-116S or H — CPU on one board, core memory on additional boards: the 116S uses 1.2-microsecond core and 116 H uses 0.98-microsecond core.
- D-216 — CPU and memory on one board.
- D-316 — CPU and memory on one board.
- D-416 — CPU and memory on one board.
- D-616 — CPU on one board, Writable Control Store and floating-point processor on a second board, memory on additional boards.

The models also use different memory modules. D-116S or H supports 4K to 128K words of core memory available in 4K-, 8K-, and 16K-word increments. D-216 includes 1K to 16K words of memory consisting of 1K to 12K words of MOS RAM available in 1K-word increments and up to 4K words of PROM or ROM available in 512-word increments. D-316 includes 4K to 32K words of core memory in 4K-word increments with byte parity. D-416 includes 4K to 32K words of core memory in 4K-, 8K-, 16K-, 24K-, and 32K-word increments. D-616 supports 4K to 1M words of core or MOS memory; MOS can include error correction and detection facilities. Memory management is required for D-116 systems with more than 32K words of memory. The D-616 houses memory above 128K words in separate cabinets.

All systesm can be housed in standard chassis 19 x 23 inches, 5.25 or 10.5 inches deep, with 4, 7, 10, or 17 (16 for the D-616) slots for options, memory, and peripherals. The D-216, D-316, and D-416 can also be ordered as stand-alone boards.

Systems are available as rack or tabletop models and with or without a programmer's console or a turnkey console. Power supply can be either 115 or 220 volts AC.

D-116 processors differ somewhat from the other models in basic specifications. The newer models have more registers, an added vectored interrupt system, more instructions, and microcoded I/O routines. The D-616 has multiported memory and a separate I/O subsystem to enhance system throughput for multiple users. Table 3 compares specifications for the five 16 Series models. All systems have both programmed I/O and DMA channels as standard features.

Up to 60 I/O devices can be connected to a D-116, D-216, D-316, and D-416 computer, while up to 62 can be connected to a D-616. If the Memory Management option is connected to the D-116, it takes up three I/O slots. All peripheral devices connect to the programmed I/O channel for transfer of control information. Slow-speed devices, such as console typewriters, punched card, paper tape, and line printers also use the programmed I/O channel for data transfers. High-speed devices, such as magnetic tape and disc, transfer data via the DMA channel. Table 4 lists individual peripheral devices supplied by DCC.

Especially important interfaces (aside from those for communications) include a multiprocessor adapter for

Table 4. DCC 16 Series: Peripherals

Model No.	Description
Terminals	
116410 Series	Teletype Models 33, 35, & 38 ASR & KSR
116424 A/B	A/N displays (4,000/1,600 char; 25 or 12 lines by 80 chars to 9,600 baud)
116480/82/84	A/N displays (1,600 char; 12 lines by 80 char; to 9,600 baud or 15,000 char/sec; models with various interfaces)
116481/83/85	A/N displays (like 116480/82/84 models but 3,200 char; 24 lines by 80 char)
116486/87/89	A/N displays (4,000 char; 25 lines by 80 char, various speeds and interfaces; some both upper- and lowercase)
Paper Tape	
116411B	300-cps reader
116412B	75-cps punch
116412D	Combination 300-cps reader, 75-cps punch
Punch Cards	
116416 Series	150-, 300-, or 600-cpm readers
116416E	300-cpm mark-sense reader
116435A	150-cpm punch
Printers	
116434 Series	60-, 125-, 300-, 600-lpm printers
116460	30-cps printer
Plotters	
116417A/B	Drum plotter (300 steps/sec; 0.01/0.005-in. or 0.1-mm steps)
116417C	Drum plotter (300 steps/sec with 0.01-in. or 0.1-mm steps; 200 steps/sec with 0.01-in. steps)
116417D	Flatbed plotter (300 steps/sec; 0.01/0.005/0.002-in. or 0.05/0.1-mm steps)
116417E	Incremental plotter (300 steps/sec; 0.01/005-in. or 0.25/0.1-mm steps)
Discs	
116418	Flexible disc (128K wd/cartridge; up to 3 drives/controller)
116447	Removable 2315-type cartridge disc (1.2M wd/cartridge; up to 4 drives/controller)
116447B/D	1 fixed, 1 removable (2315-type) cartridge disc (2.4/5M wd/cartridge; 2/4 drives/controller)
116452	Disc pack drives (40M or 80M bytes; up to 8 drives/controller; CDC discs; dual computer access option; 30-msec access; 600K-wd/sec transfer rate)
Magnetic Tape	
16430 Series	NRZI tape drives (7- or 9-trk; 12.5, 24, 45, or 75 ips)
116430 Series	PE tape drives (9-trk; 1,600 bpi; 45 or 75 ips)
116461	Cassette drive (up to 125K wd/cassette)
Process I/O	
116455 Series	A/D & D/A subsystem (up to 64 single-ended (32 differential) inputs with 8/10/12/13/14/15 bits; or up to 16 single-ended together with 2 D/A, or 8 D/A)
116456 Series	D/A conversion subsystem (up to 24 D/A converters with 8/10/12/13/14 bits)
116466	Digital I/O (16 input, 16 output lines)

Table 4. (Contd.)

Model No.	Description
Communications & Local Interfaces	
116462/116415	Single-line interfaces (async/sync)
116425	IBM 360/370 programmable interface
116426	16-line async multiplexor
116427	4-line voltage interface (EIA RS2326)
116428	4-line current interface (for local teletypewriter)
116431 Series	8-line async line units (for either voltage or current loop interfaces)
116438	Multiprocessor communications adapter (for up to 15 16 series computers)
116450	Teletypewriter junction panel (for up to 16 teletypewriters or displays)
116451	Modem junction panel (for up to 16 lines)
116472	Auto calling unit (up to 4 dialer interfaces)
116475	4-line sync unit (up to 250K baud)

up to 15 processors and an IBM System/360 or 370 interface that allows the DCC computer to be adapted to front-end processing.

Software packages vary in the minimum configurations they require. Table 5 lists the important packages with their configuration requirements.

COMPATIBILITY

The DCC D-116 family is fully compatible with the Data General Nova 1200, 1210, and 1220 minicomputers; it is not completely compatible with the Nova 800 or the Supernova. Software requirements for the D-116s are identical with those for the 1200 series, and interchangeability is maintained even through the subassembly level. Peripheral interfaces are also compatible.

D-216, D316, D-416, and D-616 are all upward compatible with the D-116 systems. Even the smallest of those models have instructions that are unavailable to the D-116. They are also upward compatible with each other; that is, the D-216, D-316, and D-416 are directly compatible, while the D-616 is upward compatible with the less powerful systems.

All 16 Series systems use the same peripherals.

MAINTENANCE

DCC provides three basic types of service contracts for purchased systems (DCC systems are not leased): on-call maintenance, an extension of the factory warranty, or the services of a dedicated on-site service engineer. The on-call contract provides regular preventive maintenance plus on-site emergency repairs for a fixed monthly charge. The warranty extension contract provides repairs at an authorized service center for a fixed monthly charge that is approximately half that of the on-call contract. The third contract provides the full-time prime-shift services of a trained customer engineer. DCC also offers noncontract service on-site or at a factory service center.

Table 5. DCC 16 Series: Basic System Software

Package	Description
Interactive Real-time Information System (IRIS)	Modular data base management and time sharing system; requires 16K wd of memory, disc, paper tape I/O, real-time clock, teletypewriter or keyboard/display
Mass Storage Operating System (MSOS)	Combines real-time executive with file manager; requires 12K wd of core, 1 mass storage device (cartridge or floppy disc, magnetic tape), ASR 33; supports FORTRAN IV, single-user BASIC
Real-Time Executive (RTX)	Multitask monitor, priority-oriented task scheduling; requires 4K wd of memory (resides in less than 2K), real-time clock, teletypewriter or keyboard/display
FORTRAN IV	Extension of ANSI FORTRAN X 3.9-1966 specifications; includes real-time extensions of ISA S61.1/1972 Industrial Computer System FORTRAN Procedures; FORTRAN 74; core-resident version requires 8K wd of memory; MSOS version (disc resident) 8K wd also
Business BASIC	Upward compatible with Dartmouth BASIC; requires 8K wd of memory, TTY control, 1 teletypewriter for single user; allows up to 5 users concurrently; requires 8K wd of memory, TTY control, and 1 teletypewriter for multiusers
Relocatable Assembler	2-pass assembler with third opt verification pass; requires 8K wd of memory, TTY
Editor	Allows user to create, modify, list, and punch source files; requires 8K wd of memory
Octal Debug	Relocatable: requires 4K wd of memory, TTY
Extended Debug	Incorporates symbolic I/O, extensive tracing; requires 4K wd of memory, TTY
D-116 Loader	Loads assembler or debug object tapes
1200 Series Absolute Loader	Used to load absolute object tapes generated by 1200 Assembler; requires TTY or paper tape reader

TYPICAL PRICES

Model Number	Description	Purchase Price $
D-116/4	Central Processor (with 4 slots & core memory)	
	4K Words	2,975
	16K Words	4,580
	32K Words	7,285
D-116/7	Central Processor (with 7 slots & core memory)	
	4K Words	3,640
	16K Words	5,255
	32K Words	7,950
D-116/10	Central Processor (with 10 slots & core memory)	
	8K Words	4,125
	32K Words	8,020
	64K Words	16,470
D-116/17	Central Processor (with 17 slots & core memory)	
	8K Words	6,130
	32K Words	10,020
	128K Words	29,270
D-216/0	Central Processor Board with RAM (incl. power monitor/auto restart, auto program load, multiply/divide, TTY interface)	
	1K Words	1,800
	8K Words	2,700
	12K Words	3,300
D-216/4	Central Processor (with 4 slots & RAM)	
	1K Words	2,700
	8K Words	3,600
	12K Words	4,200
D-216/7	Central Processor (with 7 slots & RAM)	
	1K Words	3,000
	8K Words	3,900
	12K Words	4,500
D-216/10	Central Processor (with 10 slots & RAM)	
	1K Words	3,300
	8K Words	4,200
	12K Words	4,800
D-216/17	Central Processor (with 17 slots & RAM)	
	1K Words	4,000
	8K Words	4,900
	12K Words	5,500
D-316/0	Central Processor with Board & RAM (incl. power monitor/auto restart; auto program load, multiply/divide, TTY interface)	
	4K Words	2,000
	20K Words	4,400
	32K Words	6,200
D-316/4	Central Processor (with 4 slots & RAM)	
	4K Words	2,900
	20K Words	5,300
	32K Words	7,100
D-316/7	Central Processor (with 7 slots & RAM)	
	4K Words	3,200
	20K Words	5,600
	32K Words	7,400
D-316/10	Central Processor (with 10 slots & RAM)	
	4K Words	3,500
	20K Words	5,900
	32K Words	7,700
D-316/17	Central Processor (with 17 slots & RAM)	
	4K Words	4,200
	20K Words	6,600
	32K Words	8,400
D-416/0	Central Processor with Board & Core Memory (incl. power monitor/auto restart, auto program load, multiply divide)	
	4K Words	2,400
	32K Words	6,000
D-416/4	Central Processor (with 4 slots & core memory)	
	4K Words	3,400
	32K Words	6,900
D-416/7	Central Processor (with 7 slots & core memory)	
	4K Words	3,700
	32K Words	7,200
D-416/10	Central Processor (with 10 slots & core memory)	
	4K Words	4,000
	32K Words	7,500

TYPICAL PRICES (Contd.)

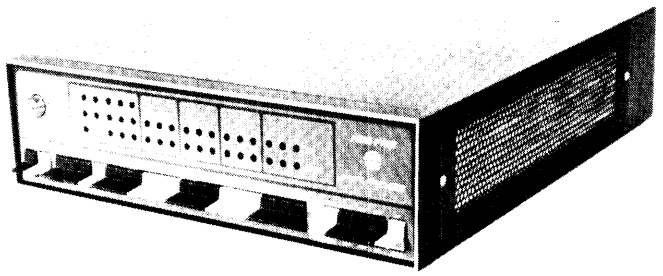
Model Number	Description	Purchase Price $
D-416/17	Central Processor (with 17 slots & core memory)	
	4K Words	4,700
	32K Words	8,200
D-616/4	Central Processor (with 4 slots & RAM or core memory; incl. power monitor/auto restart, auto program load; 616880 memory expansion & protection unit in 48K-word or larger configurations)	
	4K Words	5,660
	32K Words	12,540
D-616/6	Central Processor (with 6 slots & RAM or core memory)	
	4K Words	5,960
	32K Words	12,840
D-616/10	Central Processor (with 10 slots & RAM or core memory)	
	4K Words	7,080
	32K Words	13,960
	128K Words	41,480
D-616/16	Central Processor (with 16 slots & RAM or core memory)	
	4K Words	7,880
	32K Words	14,760
	128K Words	42,280
D-616/4	Central Processor (with 4 slots & RAM with error detection & correction; (incl. power monitor/auto restart, auto program load; memory expansion & protection unit in 48K-word or larger configurations; memory capacity beyond 128K words available)	
	4K Words	7,260
	32K Words	16,540
D-616/7	Central Processor (with 6 slots & RAM)	
	4K Words	7,560
	32K Words	16,840
D-616/10	Central Processor (with 10 slots & RAM)	
	4K Words	8,680
	32K Words	17,960
D-616/16	Central Processor (with 16 slots & RAM)	
	4K Words	9,480
	128K Words	55,880
	Processor Options	
116806	Power Monitor & Auto Restart	325
116807	Hardware Multiply/Divide	1,430
116808	Automatic Program Load	325
116810/216810/ 316810/416810	High Current Power Supply	150
116880	4-User MEU	3,500
216811/316811	Battery Backup	400/750
216812/316812/416812	Backplane Assembly	175
216818/316818/416818	Voltage Interface	150
616807	Multiply Divide (signed/unsigned)	500
616811	Battery Backup	200/750
616880	4-User MEU	2,000
616813	User Microprogram PROM	500
616815	Floating Point Processor	3,000
616816	Writable Control Store	4,200
616817	Decimal Arithmetic Processor	3,000
	Memory Options	
116883	4K-Word Core Memory (960 nsec)	1,800
116885	16K-Word Core Memory (960 nsec)	3,180
116803	4K-Word Core Memory (1.2 μsec)	1,800
116875	16K-Word Core Memory (1.2 μsec)	3,180
116876	PROM Memory	1,525
116877	RAM Memory	1,225
216881	512-Word PROM	125
616857/616847	256K-Words Core; 256 Words RAM	71,120
616838	512K Words RAM with EC	191,440
616853	16K Words Core	4,420
616842	8K Words RAM	2,260
616835	32K Words RAM with EC	11,840
	Mass Storage	
116418	Flexible Disc Control Interface	1,000
116418A	Flexible Disc Control	1,350
116466	Cartridge Disc Control	3,500
116447A	Cartridge Disc Drive (1.2M words)	5,900

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $
116447B	Cartridge Disc Drive (2.4M words)	6,450
116447D	Cartridge Disc Drive (5M words)	6,950
116452	40/80-Megabyte Disc Control	6,700
116452-1	Dual Access	1,000
116452A	40-Megabyte Disc Drive	12,500
116452B	80-Megabyte Disc Drive	22,800
116452C	40-Megabyte Disc Pack	800
116452D	80-Megabyte Disc Pack	975
	Input/Output	
116411	Paper Tape Reader Control Interface	675
116411B	Paper Tape Reader	1,450
116412	Paper Tape Punch Control Interface	560
116412B	Paper Tape Punch	2,000
116412D	Combination Reader/Punch	3,175
116430	NRZI Magnetic Tape Control	3,500
116430-1	Phase-Encoded Magnetic Tape Control	4,200
116430C/D	Magnetic Tape Transport (9-trk, 45 ips)	5,500
116430E/F	Magnetic Tape Transport (7/9-trk, 12.5 ips)	4,000
1164301	Magnetic Tape Transport (9-trk, 75 ips)	8,500
116461	Cassette Loader II	1,850
116414	I/O Interface Board	200
116416	Card Reader Interface	700
116416A	Card Reader (300 cpm)	2,950
116416C	Card Reader (600 cpm)	4,100
116416D	Card Reader (150 cpm)	2,000
116416E	Mark-Sense Card Reader (300 cpm)	4,295
116434	Card Punch Control	850
116435A	Card Punch (100 cpm)	14,250
116424A	Video Display (25 lines, 80 char/line)	3,000
116480	Video Display (12 lines, 80 char/line)	1,405
116434A	Printer (60 lpm)	2,950
116434B	Printer (125 lpm)	6,000
116434D	Printer (300 lpm)	8,500
116460A	Character Printer (30 cps)	2,725
116434E	Printer (600 lpm)	13,900
116410B	Teletype Model 33 KSR	1,300
116410D	Teletype Model 35 ASR	4,475
116410F	Teletype Model 38 ASR	2,500
116417	Plotter Control Interface	1,250
116417A	Drum Plotter	6,850
116417D	Flatbed Plotter	25,500
116417E	Incremental Plotter	5,000
	Clocks	
116408	Real-Time Clocks	325
116468	Programmable Interval Timer	600

A service agreement provides on-site maintenance service, parts, and preventive maintenance. Basic monthly maintenance charge 9:00 a.m. to 5:00 p.m. Monday to Friday is 1% of the list price of the equipment as stated in the price list in effect: 8-hour service Saturday is charged at 25% additional; 35% additional for 16-hour service 7 days a week, and 75% additional for 24-hour service Monday to Friday, 80% for Saturday, and 85% for Sunday. Additional charges are made for equipment located over 100 miles from a service center.

DIGITAL COMPUTER CONTROLS
DCC-16 Series System Report Update



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OVERVIEW

When Digital Computer Controls (DCC) announced the new computers in its "16 Series," D-216, D-316, D-416, and D-616, a 516 model was conspicuously absent. The older D-116/S and H models fit in price and performance into the void in the new 16 Series. Apparently, the D-116 models were selling briskly, and DCC felt no pressure to announce replacements for them.

On November 7, however, a Delaware Chancery Court order permanently enjoined Digital Computer Controls, Inc. from using the logic design of Data General's NOVA® 1200 for any purpose other than maintenance and from using NOVA 1200 and DCC's D-116 logic drawings for manufacturing minicomputers substantially identical to the NOVA 1200. The injunction was suspended to give DCC a chance to appeal but the company was ordered to post a bond of $500,000. DCC posted the bond on November 10 and announced its intention to appeal the court decision. Data General originally brought the trade secrets suit against DCC in 1971. If the decision for Data General is upheld, a jury trial will determine the damages DCC must pay Data General.

In the meantime, DCC announced the MOD 5, the D-116 replacement in the new 16 Series line. The MOD 5 is available in two core memory versions and one MOS memory version. The MOD 5/S uses core memory with 1.2-microsecond cycle time; the MOD/H uses core memory with 1.0-microsecond cycle time; and the third MOD 5 model uses MOS memory with 0.8-microsecond cycle time. Table 1 compares the mainframe characteristics of the MOD 5 to the D-116H and the Data General NOVA 3. The prices for the MOD 5/S are identical to the D-116 prices. The MOD 5/H CPU costs $100 more than the MOD 5/S CPU. The MOD 5 is upward compatible with the D-116 and totally compatible with the rest of the new 16 Series line. The MOD 5 has the extended instruction set of the new 16 Series. Delivery of the MOD 5 is 60 days ARO (After Receiving Order).

COMPETITIVE POSITION

Although the MOD 5 was hurriedly introduced, it was obviously planned as part of the 16 Series line. It offers more performance than the D-116 but at the same price. In today's market, the MOD 5 will compete with the Data General NOVA 3 rather than the older NOVA 1200, the system involved in the Data General suit. The MOD 5 core versions are more expensive than the NOVA 3 for systems configured with 32K or 64K bytes of memory. The MOD 5 costs less than the NOVA 3 for systems with 256K bytes. Prices for the MOD 5 MOS memories have not been announced. Table 1 compares MOD 5 with NOVA 3 and the D-116H.

The MOD 5 implements both signed and unsigned multiply and divide in firmware. NOVA 3 implements only unsigned multiply and divide. NOVA 3 can use the same floating-point processor as the rest of the NOVA line. Initially, MOD 5 does not offer a floating-point processor.

HEADQUARTERS

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(201) 575-9100

Table 1. Digital Computer Controls MOD 5 Compared to 116 and NOVA 3 Computers

	MOD 5/S	MOD 5 (RAM)	MOD 5/H	D-116H	NOVA 3
CPU					
Technology	MSI, T^2L	MSI, T^2L	MSI, T^2L		MSI bipolar
Number of Instructions	76	76	76	39	39 + 31*
Number of Registers	8	8	8	4	4
Number of Interrupt Levels	62	62	62	16	16
Instruction Execution Times, μsec					
Add/Subtract	1.2	1.6	1.0	1.0	0.7
Unsigned Multiply	3.8	NA	3.0	3.0	5.8
Unsigned Divide	4.1	NA	3.2	3.2	6.7
Signed Multiply	10.0	NA	8.4	—	—
Signed Divide	28.4	NA	23.1	—	—
Floating-Point Arithmetic					
Add/Subtract	—	—	—	—	7.7
Multiply	—	—	—	—	11.3
Divide	—	—	—	—	13.7
Stack Facilities	Yes	Yes	Yes	No	Yes
Memory					
Technology	Core	MOS	Core	Core	MOS
Word Length	16	16	16	16	16
Cycle Time, μsec	1.2	0.800	1.0	0.960	1.0
Parity	No	1 bit/byte	No	No	Opt
Memory Protect	Opt	Opt	Opt	Opt	Opt
Memory Management Unit	Opt	Opt	Opt	Opt	Opt
Capacity, words					
Min	4K	4K	4K	4K	4K
Max	128K	128K	128K	128K	128K
Input/Output					
Number of Devices	62	62	62	62	61
DMA Max					
Xfer Rate, words/sec					
Input	833,333	1,250,000	1,040,000	1,040,000	1,000,000
Output	625,000	1,000,000	750,188	695,000	—
Price, CPU + Memory, $					
32K bytes	4,580	NA	4,680	4,580	4,400
64K bytes	7,285	NA	7,385	7,285	7,100
256K bytes	29,270	NA	29,370	29,270	34,200

The MOD 5 implements three stacks, while NOVA 3 implements one stack. MOD 5 is available in four chassis sizes: four-slot, seven-slot, 10-slot, and 17-slot. NOVA 3 is available in a four-slot chassis or a 12-slot chassis. Expansion chassis are available for additional peripheral controllers or for additional memory for NOVA 3.

Although DCC initially marketed its systems as software and peripherals compatible with the NOVA 1200, this has been soft-pedaled in recent years. DCC has developed its own software for the D-116. But, DCC has delivered 6,000 D-116 systems, so the Delaware court decision is extremely important to both DCC and Data General. If the decision is upheld, a jury could award Data General substantial damages. The decision could also have consequences throughout the computer industry. A number of other "look-alike" systems are around, notably the Amdahl 470V/6 and at least two well-advertised replacements for the IBM 1130 — General Automation 18/30 and Digital Scientific Meta 4.

Although the Data General-Digital Computer Controls case is based on special circumstances, the court decision did rule on a broad issue when it enjoined DCC from using NOVA 1200 logic diagrams for anything other than maintenance. Whatever the outcome may be, DCC certainly will discontinue production of the D-116 as quickly as possible and begin delivering the MOD 5.

TYPICAL PRICES

Equipment	Purchase Price, $			
Mod 5 CPU, System with Memory, words	Mod 5/4	Mod 5/7	Mod 5/10	Mod 5/17
4K	2,945	3,640	3,700	5,410
8K	3,365	4,055	4,125	6,130
16K	4,580	5,255	5,320	7,330
24K	6,220	6,890	6,955	8,960
32K	7,285	7,950	8,020	10,020
48K	—	—	13,770	15,770
64K	—	—	16,470	18,470
128K	—	—	—	29,270

Processor Options	Purchase Price, $
Mod 5 CPU, H option	100 for each CPU
Firmware signed and unsigned multiply and divide	700
Power Monitor and Auto-Restart	325
Hardware Unsigned Multiply and Divide	1,200
Automatic Program Load	325
MEU (Memory Expansion and Protection Unit) Backplane	50
High Current Power Supply (increases current capacity)	150
For 10-slot chassis	490
4-User MEU Unit	3,500

Equipment	Purchase Price, $
Memory, words	
1/1.2-μsec Cycle Time	
4K	1,800
8K	2,000
16K	3,180
Expansion Chassis	
6-Slot	1,350
15-Slot	1,650

DIGITAL EQUIPMENT CORP.

Super-8

OVERVIEW

If the automobile business were not in the doldrums, one could imagine going into a showroom on a Saturday afternoon and driving out in a "Super-8." The Super-8, however, is Digital's latest implementation of the PDP-8/A. A parallel processor that performs all fixed- and floating-point arithmetic operations in hardware makes the Super-8 super. The PDP-8/A processor performs system management and input/output operations. The Super-8 adds 64 instructions to control the arithmetic processor, which has direct access to memory and can address 32K words.

The arithmetic processor uses three data formats for operands and results: 24 bits for fixed-point arithmetic and a 24-bit or 60-bit fraction with a 12-bit exponent for floating-point arithmetic. The Super-8 can run ANSI-compatible FORTRAN IV programs under the OS-8 operating system.

The Super-8 performs calculations much faster than any previous PDP-8 model. Typical instruction execution times are as follows:

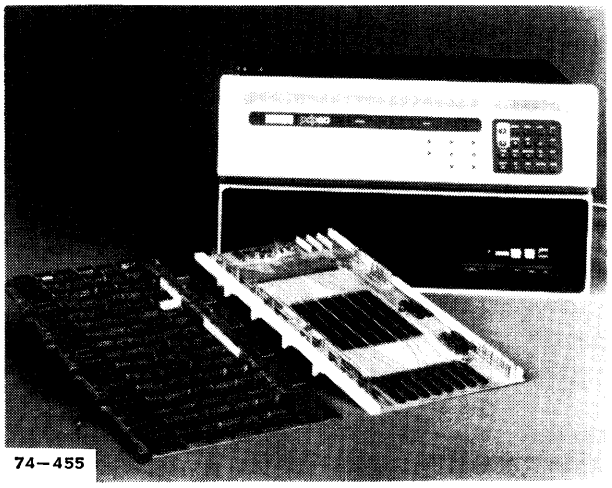
Instruction	Execution Time, μsec.
Fixed-point (24-bit operands)	
Add	10.5
Floating pt. (24-bit fraction)	
Add	30.0
Multiply	37.5

The PDP-8/A computers already in the field can be upgraded to a Super-8. Two circuit boards must be added to a PDP-8/A-400 to convert it to a Super-8. Other systems must first be upgraded to PDP-8/A-400.

Cost of the Super-8 with 8K words of core memory is $5995. First deliveries are scheduled for April 1976.

DIGITAL EQUIPMENT CORPORATION

PDP-8/A, 8/E, 8/F, and 8/M


74-455

OVERVIEW

The PDP-8 family of computers were the first computers on the market that combined the small size, processing power, and low cost now associated with the whole class of systems termed "minicomputers." Since Digital's original introduction of the PDP-8, the company has continued to develop this 12-bit line, adding new memories, new processors, new peripherals, and a programmable general-purpose register and changing from the positive external bus on earlier models to an internal OMNIBUS®. The OMNIBUS saves space and eliminates back-panel wiring by allowing all system modules (including memory and the CPU) to communicate over the same bus, with the result that any module can be located anywhere along the bus. Because the PDP-8 continues to be popular, a large body of all types of efficient software is being accumulated, resulting in even more user interest. As a result of this developmental cycle, there are more installed PDP-8s than all other minicomputers put together.

The current PDP-8 models, the 8/A, 8/E, 8/F, and 8/M, can all expand the basic memory to 32K words. The 8/E is the top of the line, with all options and peripherals available for expansion of the basic system. The 8/F is a physically smaller 8/E with lower initial power requirements and somewhat less internal expansion capability. The 8/M is basically an 8/F geared to the OEM market. The 8/A is a new MOS system with a compact 1-board CPU for even greater savings to OEM users.

The 8/E-8/F-8/M models use core modules with a 1.2/1.4-microsecond cycle, while the 8/A uses MOS modules with a 2.3/2.8-microsecond cycle. All can attach ROM and PROM modules; all can attach the same peripherals, use the same software, and perform the same functions.

® Registered trademark

Peripherals of every variety are provided for the PDP-8: conventional I/O units for cards and paper tape, including a mark-sense card reader; DECtape or cassette tape as mass storage for small systems, and industry-standard tape for larger storage requirements; fixed- and movable-head disc subsystems for larger systems; terminals, CRTs, and plotters; special-purpose subsystems to handle A/D, D/A, and digital I/O for data acquisition and control applications; and a fairly broad range of communication interfaces for data communication environments.

More than 700 programs are DEC-supported for the 8/A, 8/E, 8/F, and 8/M. Many of these programs were developed by DEC and many by users who also contribute programs to the DECUS (Digital Equipment Corporation Users' Society) software library. Available software includes general operating systems (CAPS — 8-cassette Operating System, RTS-8 Real-Time Operating System, OS-8), a variety of special-purpose operating systems (LAB-8/E, PHA-8, INDAC 8, EDUSYSTEMS, TS8/E time-sharing, COS 300 commercial, and others). Language facilities include BASIC, FORTRAN, ALGOL, FOCAL (a compact interactive language similar to BASIC), DIBOL (a commercial language similar to COBOL) and assemblers. Special application software is available for communication, typesetting, industrial data acquisition, numerical machine control, education, graphic displays, and a variety for scientific laboratory instrument control. The comprehensive OS/8 operating system is an excellent system for combining interactive processing and batch processing; resident core requirements can be as little as 256 words of memory.

History

In 1965, Digital Equipment Corporation (Digital) delivered the first member of its largest family of computers, which has grown to include Models PDP-8, 8/S, 8/L, 8/I, 8/E, 8/F, 8/M, and 8/A. Related members include the LINC-8 and PDP-12. Only the PDP-8/E, 8/F, 8/A, and 8/M and the PDP-12 are in production. All other family members are "traditional" products, that is, products Digital services and maintains but no longer produces. Generally, Digital retrofits new software and peripheral devices to the traditional products in the line. Returned machines are refurbished and sold at prices competitive with those for newer products.

The first PDP-8 went against the trend toward big, complex, expensive computer systems with massive software. It had a short word length (12 bits), modular memory of 4K to 32K words, a 1.5-microsecond cycle time, simple instruction set, flexible I/O structure, and an $18,000 price tag. The system lent itself to many scientific and control applications that did not require the power of the computers supplied by the large manufacturers. PDP-8 sold briskly; over 25,000 computers from the family have been installed to date. Its popularity proved there was a large market for this type of computers, now called minicomputers. In 1966, the PDP-8 was followed by the

PDP-8/S, a slower, smaller, cheaper version of the PDP-8 with a curtailed I/O capability. The 8/S was a highly successful system extending the market to users who did not need the PDP-8's speed. It cost about $9,000 less than the PDP-8.

The PDP-8/S was followed by the PDP-8/I and PDP-8/L in 1968. The PDP-8/I was a redesigned PDP-8 using TTL integrated circuit modules to duplicate the functional capabilities of the PDP-8. PDP-8/I was physically smaller and about $5,000 lower in price than the PDP-8. PDP-8/L was designed primarily for the OEM market. System expansion capability was removed from the PDP-8/L processor chassis, and expansion modules had to be added to the PDP-8/L system before additional core memory and I/O devices could be connected. Originally the PDP-8/L core memory capacity was limited to 8K words, subsequently raised to 12K words, and eventually increased to 32K words, the same as for the other PDP-8 processors. The basic PDP-8/L sold for about $5,000 less than the PDP-8/I.

PDP-8/E, first delivered in 1970, is a slightly faster, more compact, more modular, less expensive version of the PDP-8/I, but with more system configuration flexibility in the lower range where the processor can operate as a sophisticated controller. In addition, the PDP-8/E has features not available on previous PDP-8 models: ROM (read-only-memory) in 256-word modules, an OMNIBUS, additional instructions, and an improved EAE (Extended Arithmetic Element) option. A minimum configuration PDP-8/E can include a processor, a 4,096-word core memory, a minimum control console, and a power supply. The PDP-8/F and 8/M, first delivered in 1970, are smaller, less expensive versions of the 8/E. The 8/F is marketed as an end-user system, while the 8/M is directed toward the OEM market.

Because the 8/E is flexible in the lower ranges, price differences for basic systems of the three core-based models do not show the wide differences found among earlier models. The lowest-priced, minimum configuration 8/E costs little more than minimum configurations for 8/F and 8/M. Prices for the 8/E and 8/F include a programmer's console, while the 8/M price includes only an operator's console. Prices for PDP-8/Ms with PROM memory and operator's console, however, are considerably less. The PROM includes 256 words of read/write memory for each 1K words.

The new PDP-8/A, first delivered in December 1974, departs from the 8/E, 8/F, and 8/M in a number of ways, while essentially retaining both hardware and software compatibility. The PDP-8/A has a CPU with MSI circuitry engineered to fit on a single board, and it uses 1K-, 2K-, or 4K-word MOS memory modules. Both the CPU and memory have slower cycles than the 1.2-microsecond 8/E, 8/F, and 8/M: 1.5 microseconds for the PDP-8/A CPU, 2.0 or 2.3/2.8 microseconds for MOS RAM, 1.5 microseconds for core and ROM, and 3.4 microseconds for PROM. Moreover, the PDP-8/A does not yet have an option corresponding to the Extended Arithmetic Element (EAE), but it is currently under development. These differences may present compatibility problems with some time-dependent or EAE programs and interfaces but, generally speaking, all of the PDP-8 software is available to the 8/A, including the OS-8, RTE-8, and CAPS-8 operating systems. The PDP-8/A minimum prices are well under $1,000 for board only systems; for a CPU and 1K word RAM, unit prices are $895 for a single system and $537 for 100 or more; "boxed" systems with chassis, power, battery back-up for MOS modules and 1K-4K words of memory are in the $1,745 to $1,995 range.

COMPETITIVE POSITION

Despite the proliferation of different minicomputers on the market, the PDP-8 family remains a significant system in Digital's product line and in the entire minicomputer field. It is a dynamic system because Digital keeps the price competitive with new models that reflect current technology, such as the recent addition of the PDP-8/A with its 1-board CPU and MOS memory. Digital also continues to add extensive system and applications software, and interfaces to it almost all of the broad range of mass storage and peripheral devices the company produces. Probably the PDP-8's strongest points in the current market are its enormous body of available software and its wide variety of peripherals. Although other systems have faster cycle times and more efficient hardware architecture, the PDP-8's software is so highly developed that it has circumvented most hardware limitations. The user sees only a highly flexible system that has software on hand for the most diverse applications.

To some extent the low end of the PDP-11 line competes with the PDP-8 for the OEM, process control, communications, and data acquisition markets.

The PDP-11, of course, can be expanded to a powerful system that competes with some of the general-purpose commercial processors. The more extensive communication offerings on the PDP-11 partly reflect the convenience of the 16-bit word in communication networks using standard 8-bit bytes. On the other hand, the PDP-8's 12-bit word is handier for interfacing some types of analog/digital equipment that frequently has 10-bit precision.

Quite apart from inherent characteristics of the two systems, the fact remains that the PDP-8's proven software makes it competitive with many other systems, including the PDP-11, for applications requiring minicomputers of its size.

Its position is doubly unique in that it has the largest share of the market of any single system, and yet it is the only 12-bit system that still retains any sizeable share of the market at all. Other manufacturers have concentrated on 16-bit (or 8-bit or 32-bit) systems that compete more directly with the PDP-11.

At the very lowest end of the market, the PDP-8/A and Digital's MPS both compete for those users who want a 1-board CPU. This market has seen much activity recently due to the new compact memories using both core and semiconductor technologies and advances in microprocessor development. General Automation, Computer Automation, and Data General have all produced 1-board systems that are upward compatible with their major computer lines; consequently, these small systems can take advantage of a body of tested software. All of these are 16-bit systems. Although most of the competing systems have higher performance than the 8/A and some can even fit 1K or 4K words of memory on the CPU board, the 8/A still retains the advantage of its fabulous software base. For users who are not interested in the software, Digital offers the MPS based on the Intel-8 microprocessor, with processor and 1K memory on a board. The MPS has only a Teletype and console for peripherals, and it is not compatible with Digital's other systems, but a PDP-8 cross assembler provides for program development.

USER REACTIONS

We interviewed a number of PDP-8 users, representing several models and a variety of applications. Without exception, all quoted the reliability of the system as one of its strong points. One user waxed enthusiastic on this subject and then said he didn't want to sound like an advertisement, but he had only experienced 1.5 hours of downtime since he obtained the system a year ago. These users also agreed uniformly on the quality of Digital's service organization and the ease with which the system could be fixed. Response to emergency calls was always prompt.

One user, who is a Digital employee, bought a computer for his own use and chose the PDP-8/E partly because he could just remove a module and carry it to a parts depot instead of having an expensive maintenance call. He has not been able to take advantage of this feature yet, however, because in the 1.5 years he has had the system, the only thing he had to fix was a burned-out lamp on the console, which he replaced himself.

Remarks from several users illustrate the maxim that nothing succeeds like success ("to him who has, more will be given," and so forth). One newspaper installation that has been using three PDP-8s (two PDP-8/S computers and one PDP-8/I) since 1968 for classified section updates, justification, and interfacing to an offset printing press would still choose the PDP-8 because so many PDP-8 installations are successful in that industry.

The chemistry department of a university bought its first PDP-8 system to teach majors how to use the computer in research projects; the PDP-8 was chosen because the department was new to minicomputers and Digital could give them the support needed to develop the software and maintain the hardware. A manufacturer of spectrometers chose the PDP-8 as the control component for a number of reasons. Highest on his list was the size of Digital's sales and service organization, which allowed the spectrometer company to market its systems internationally without worrying about maintenance for the computer component.

The breadth of hardware offerings was a factor mentioned particularly among scientific users. The chemistry department mentioned earlier felt this was important because future expansion might take on unknown directions. An independent consulting service developing an inexpensive system for analysis of chromosomal aberrations needed the fully software-supported digitizer/writing tablet/spark pen combination. A PDP-8 at the center of a rapidly expanding system for monitoring pacemakers will have to handle up to 1,000 special terminals by next year. The department ordered a second PDP-8 with computer tape to process complete medical records instead of the abbreviated versions currently used.

Almost all users stressed the variety of software available as a powerful factor in selecting the PDP-8. The spectrometer manufacturer wanted a maximum number of routines to choose from so that he had a minimum amount of work to do himself. The Digital employee wanted an efficient high-level language on a 4K machine and was attracted by the FOCAL interpreter. The chemistry department wanted as much help as possible because of its inexperience.

A high school implementing a computer-related mathematics program needed an inexpensive system that could provide the BASIC language. Only the newspaper was not taking advantage of Digital's software; a software house developed the software six years ago, at the time of the initial acquisition.

Last, but hardly least, was the cost of the system. The PDP-8 has remained competitive in price and won the previously-mentioned high school math department contract by bidding to a set of specifications. Price was also an essential element to the laboratory programming for chromosomal aberrations. The big problem here was not how to detect, analyze, and interpret, but how to make the procedure cost-effective enough to become a widely available service. Competitive pricing was quoted as a factor of varying degrees of significance to each of the users.

CONFIGURATION GUIDE

All basic PDP-8/E, 8/F, and 8/M computers use the same KK8-E Central Processor, power supply, chassis, and OMNIBUS with 20 quad bus slots. Basic systems also include memory modules, mounting, and an operator interface (either an operator's or programmer's console) and TTY control combinations. The PDP-8/E has two sets of submodels with identical specifications: one set has an on-site warranty and one set has a factory warranty. In addition, all submodels on all processors can connect to 115- and 230-volt power sources.

Memory can expand in increments of 4,096 words for core and 256 words for ROM on the 8/E, 8/F, and 8/M.

ROM and core memory can be intermixed in any desired combination, but a memory extension control is necessary when total memory exceeds 4,096 words. Maximum memory on all current PDP-8 systems is 32,768 words.

A basic PDP-8/E, 8/F, or 8/M computer uses eight to 11 of the 20 standard OMNIBUS quad slots in the basic system: central processor, five slots; programmer's console (if included), one slot; 4K-word memory, three slots or 8K-word memory with extension control, four slots; and Teletype control (if included), one slot. The operator's panel on 8/M systems does not require an OMNIBUS slot.

All 8/E, 8/F, and 8/M processors can optionally attach an Extended Arithmetic Element (EAE) and a Floating-Point Processor (FPP). Both are high-speed asynchronous hardware modules that attach to the OMNIBUS like peripheral devices. EAE performs division, multiplication, and other mathematical functions, and FPP performs floating-point and double-precision arithmetic. Both EAE and FPP increase processor throughput indirectly, because OS/8 systems equipped with these modules greatly expedite FORTRAN IV compilations and runs.

A basic 8/E system can be expanded within the main chassis through the BE8A OMNIBUS expander, which adds 18 more usable slots. In addition, a BA8 System Expander Box allows the OMNIBUS to be expanded by 18 more slots outside the chassis. The BA8 itself can be expanded by 18 additional slots for a maximum of 76 slots per 8/E system. Because the 8/F and 8/M models have smaller chassis, the internal expansion option is not available to them, and these models can expand only up to 56 slots through an external BA8 expanded to full capacity.

The PDP-8/A fits on a single 15 by 8.5-inch "hex" size board, housed in an eight-slot chassis. It can attach its own version of almost all 8/E, 8/F, and 8/M options and all of the same peripherals, except the KE8-E Extended Arithmetic Element, the AD8-E Extended Arithmetic Element, the AD8-E Analog-to-Digital Converter and MUX control, and the AM8-EA MUX and preamplifiers. The slower memory cycle of the PDP-8/A CPU (1.5 microseconds) may affect certain time-dependent PDP-8/E interfaces. Autostart is a standard feature which must be switched off if the 8/A's own power-fail/auto restart option is included.

The PDP-8/A uses 1K-, 2K-, and 4K-word MOS memory modules with 2.0 or 2.3-microsecond read and 2.8-microsecond write cycles; each module requires one slot. A special 1.5-microsecond core board is also available for the 8/A. Like the 8/E, 8/F, and 8/M, the PDP-8/A requires the KM8-A extended option board to expand memory beyond 4K words. The KM8-A also includes the PDP-8/A's power fail/auto restart option, time share control to distinguish between user and monitor modes, and a bootstrap loader. ROM memory can be added in 1K-, 2K-, or 4K-word increments, and PROM is added in 1K-word increments. Both ROM and RAM can be included on a system.

The DKC8-AA option board adds a Serial Line Unit, a Parallel I/O interface, a 100-Hertz crystal-controlled real-time clock, and a programmer's console control. The KC8-AA programmer's console is newly designed for the 8/A, with a 5 by 4-inch key pad and LED octal readouts.

The PDP-8/A-100 is offered in three packaged models that differ in the type of memory used, slots available, and power supply. The 8/A-100 is a 10-slot system, with either a 20 amp, ± 5 volt power supply, or a 1 amp, ± 15 volt power supply, battery backup for the entire system for 1 to 7 minutes, operator's panel, and chassis. Memory can be the same ROM, RAM, and PROM modules discussed for the 1-board system.

The PDP-8/A-200 is a 12-slot system with the same power options as the 8/A-100, but it has a 1-hour battery backup for the memory only. All other basic system components are the same as the 8/A-100, except that the 8/A-200 has the option of attaching a 4K-word MOS board using 4K chips with a 2.0 microsecond cycle.

The 8/A-400 system is a 12-slot system like the 8/A-200, but with 25 Amp, ± 5 volt power, no battery backup and core memory. The core board, with a 1.5-microsecond cycle time, is not compatible with the 8/E, 8/F, and 8/M systems.

No bus extensions are allowed for any of the PDP-8/A systems. Mainframe specifications are given in Table 1.

A variety of standard peripherals can be attached to any PDP-8. These are summarized in Table 2. There are some limitations on the numbers of special interfaces that can be attached to any PDP-8. Only one KA8 external interface for positive I/O devices need be attached per system. This interface can handle all traditional positive I/O bus devices. A maximum of 12 Data Break (DMA) Interfaces are allowed, with one interface per device. Up to eight DB8 Interprocessor buffers or DR8 12-channel buffered digital I/O interfaces can be attached. The maximum number of KL8-E or J Serial Line Interfaces per system is 17.

Each DB8-E interprocessor buffer allows two or more PDP-8s to exchange data. The sending computer loads the buffer from the accumulator and sets a flag in a receiving computer. Transfers are one word at a time as the receiving computer senses the set flag.

Digital has a specially-priced prepackaged system for use with the OS/8 operating system. This includes a PDP-8/E with memory extension control and time-share option, 8K or 16K words of core memory, cassette bootstrap loader, dual drive cassette system, disc cartridge system, DECwriter data terminal with a parallel interface and freestanding cabinet.

Each major software package has minimum configuration requirements. Table 3 summarizes PDP-8's system software and the configuration requirements of the major packages.

COMPATIBILITY

Generally, the various members of the PDP-8 family are compatible with comparable configurations from one model to the next. In some cases, however, users' software must be reprogrammed for an improved optional feature, such as the PDP-8/E EAE (Extended Arithmetic Element), which differs significantly from previous EAE options. This option uses some of the instruction codes previously available for microcoding the Operate instructions.

The Positive I/O Bus Interface allows peripherals originally designed for the PDP-8/I, 8/L, and 8/S systems to be attached to the OMNIBUS on the PDP-8/E, 8/F, and 8/M. Because the PDP-8/A uses an OMNIBUS similar to the 8/E and it can attach the Positive I/O Bus, nearly all PDP-8 peripherals can attach to the 8/A. Exceptions are the A/D converter and its related MUX. The 8/A is slower than an 8/E, and also does not have an EAE like the 8/Es. These may create some compatibility problems with time-dependent programs and interfaces.

Table 1. Digital Equipment PDP-8: Mainframe Specifications

MODEL	8/E, 8/F, 8/M	8/A
CENTRAL PROCESSOR		
Microprogrammed	No	No
No. of CPU boards	5	1
No. of Registers	5	5
Addressing		
Direct	256	256
Indirect	1 level to 4K	1 level to 4K
Indexed	1 level "auto index"	1 level "auto index"
Instruction Set		
Number (std; opt)	56; 72	56
Extended Arithmetic	Yes, option	No
Decimal Arithmetic	No	No
Floating Point	Hardware option	Hardware option
Priority Interrupt Levels	1	1
MAIN STORAGE		
Type	Core	MOS; core
Cycle Time (μsec/wd)	1.2; 1.4 (2 accesses)	2.3 read, 2.8 read/write (MOS); 1.5 (core)
Basic Addressable Unit	12-bit wd	12-bit wd
Bytes/Access	2 (6-bit)	2 (6-bit)
Min Capacity (wds)	4K	1K
Max Capacity (wds)	32K	32K
Increment Size (wds)	4K; 8K	1K; 2K; 4K
Ports/Module	1	1
Parity	Option	Option
Protect	Software or ROM	Software or ROM
Memory Management	To 32K	To 32K
ROM		
Use	Program protection	Program protection
Capacity (wds/module)	256	1K-32K/system
PROM	1K-wd module	1K-wd module
INPUT/OUTPUT		
Programmed I/O	Yes	Yes
DMA Channels (no.)	1-12	1-12
Multiplexed I/O	No	No
Data Break (for positive I/O devices)	Option	Option
Max DMA Transfer Rate (wds/sec)	833,333	333,333 (MOS), 833,333 (core)

MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks in the United States and worldwide, numbering more than 1,500 engineers.

Table 2. Digital Equipment PDP-8: Peripherals

MODEL NUMBER	DESCRIPTION
DISCS	
DF32/DS32	Fixed Disc, 32K wds/drive, 4 drives/controller
RF08/RS08	Fixed Disc, 262K wds/drive, 4 drives/controller
RK8/RK05	Disc Cartridge System, 1.6M wds/drive, 4 drives/controller
MAGNETIC TAPE	
TC08/TU56	DECtape, 8 drives/controller
TD8/TD8-E	Dual DEC cassette, 75K-byte capacity/cassette, 8/system
TM8/TU10	7- and 9-trk DEC MAGtape drives, 8 drives/controller
CARDS	
CM8	Optical Mark Card Reader, 300 cpm
CR8	Punch Card Reader, 300 cpm
PAPER TAPE	
PR8	Reader
PP8	Punch
PC8	Combination Reader/Punch
PRINTERS	
LS8	Dot Matrix Printer, 165 cps
LE8	Line Printers, 173-356 lpm
LS01	Printer for VT8 Display, 165 cps
TELETYPEWRITERS	
LT33/LT35	ASR & KSR Teletypes, 10 cps
LA30	DECwriter, 30 cps
DISPLAYS	
VT8	Alphanumeric and Graphics Display
VC8/VR14, VR20	Plot Display, Subsystem, B & W or 2-color display
VT05	A/N Terminal 1,440 Char (72 x 20)
PLOTTERS	
XY8 Series	CalComp 565, 563, and Houston Instruments DP-1, DP-10
TERMINALS	
RT01	Numeric Data Entry Terminal, 16-digit display
RT02	Alphanumeric Data Entry Terminal, 32-digit display
WRITING TABLETS	
VW01 Series	Tablets, 4 multiplexors/control
COMMUNICATIONS	
KL8 Series	Async Line Interface, 110-2,400 baud models
DP8	Sync Modem Interface
DC08	ACU and 10-channel Multiplexor
PROCESS I/O	
AD8	10-bit Subsystem, up to 16 chan
AD01	10-bit Subsystem, up to 32 chan
AF04A	Integrated Digital Voltmeter, to 128 chan
AFC8	Low-Level Differential Analog Input Subsystem, up to 128 chan
AA50	Digital-to-Analog Subsystem, up to 6 chan
UDC8	Digital I/O to 192 digital pts

Aside from 46 sales and service locations in the United States, Digital has five offices in Canada, six in Australia, five in Germany, six in the United Kingdom, three in Brazil and one or two each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, Netherlands, New Zealand, Norway, Phillipines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicomputer manufacturers have traditionally aimed at somewhat "self-sufficient" users, requiring considerably less software support and applications programming assistance than the large commercial system users, this picture is changing, as evidenced by Digital's recently-added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour shifts. An on-site engineer can be hired if requirements are critical, or a user can buy an on-call service or set up his own maintenance staff.

Table 3. Digital Equipment PDP-8: Software

PACKAGE	DESCRIPTION
OS-8	Standard PDP-8 operating system for batch and interactive processing, requires 8K-wd memory, cassette I/O and bootstrap, disc, and DECwriter terminal
RTS-8	Real-Time multiprogramming system
CAPS-8	For small cassette-based system, requires 4K-wd memory, 2 TU-60 cassette drives, teletypewriter
TS8/E	Time-sharing system for up to 17 users, requires 8K-wd memory, KM8-E Interface
COS-300	Commercial operating system, requires 8K-word memory, discs, console, printer; can operate in foreground/background mode
BASIC	9 different packages: EDU System 10, 20, 28, 30 versions using OS/8, CAPS-8, LAB 8/E, Industrial real-time BASIC, Dartmouth BASIC. Various requirements range from 4K-12K-wd memories, all require LT33-D or LA30-P terminals, some require PC8-E, others require RK8-E disc, TU56 tape, or DECtape
FOCAL	Interactive language for small computers, requires 4K-wd memory, LT33-D terminal
FORTRAN, FORTRAN IV	FORTRAN in stand-alone or OS/8 versions, FORTRAN IV for OS/8, all require 8K-wd memory, PC8-E, LT33-D or LA30-P terminals, OS/8 versions read disc
DIBOL	COBOL-like language for 8K-wd system under OS/8
ALGOL	From DECUS; ALGOL 60 subset of ALGOL-8
Assemblers	PAL III or PAL C/Macro-8 require 4K-wd memory, and LT33-D terminal; SABR stand-alone, OS/8, PAL-8, CAPS-8, PAL-C, and OS/8 SABR need 8K wds of memory
Utilities	4 Symbolic editors, 3 floating-pt package, libraries, editors, loaders, debuggers, diagnostics, many others
EduSystems	For hands-on classroom use with BASIC or FOCAL single-user to 8 users and batch versions (several versions)
Typeset-8	Several typesetting systems for justifying, hyphenating, etc.
COGO-8	For interactive graphics control, requires 16K-wd memory, OS/8, 2 DECtape drives, DECwriter
LAB-8	Signal Averaging System for 8/E with 10-bit A/D, 10-bit plot display controller, clock, lab panel, and ASR-33
Communications	Programs for concentration, message switching, data collection, remote batch

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	SYSTEMS		
STD8E CA/CB	Packaged Hardware/Software System RK8-E Cartridge Disk System TA8E DECcassette with dual drives PDP-8/E Central Processor (8K words) Decwriter MI8-EL Bootstrap for DECcassette H960-BC Cabinet OS/8 Operating System on Cassette	18,000	232
STD8E CC/CD	Same as STD8E-CA/CB Except with 16K Words of Memory	20,000	275
LAB8E-05	The LAB8E-05 PDP-8/E-PA Tabletop PDP-8/E (4K memory) H945-AA Laboratory Data Panel (tabletop) LT33-D ASR-33 Teletypewriter and Punch AD8-ES 10-Bit A/D Converter VC8-E 10-Bit Point Plot Display Controller DK8-ES Real-Time, Programmable Clock LAB8E Software Kit	9,760	117

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
LAB8E BA/BB	Laboratory System for General Purpose Computing PDP-8/E-NE/NF Central Processor (8K-wd core memory; terminal control) LT33-DC/DD ASR 33 Terminal AD8-EA A/D Converter AM8-EA 8-Channel MUX and Preamps AM8-EC Control Panel DK8-ES Programmable Clock, Schmitt Triggers, and Front Panel VC8-E Scope Controller H945-AB/CB Cab Mounting Panel H960-BB/CB Cabinet LAB8E Software Kit	13,470	151
OS/8-10	Complete Hardware/Software System PDP-8/E1AE Central Processor (8K-wd core memory) DECwriter Terminal MR8-EC Bootstrap Loader TD8-EM Dual DECtape Drives H967-BA Cabinet H952-HA Table OS/8 System Software	14,400	161
LAB8E-15	System PDP-8/E-NE — Rack-Mountable PDP-8/E; 8K Memory less Teletype Control PC8-E — High-Speed Paper Tape Reader/Punch DECwriter — Terminal H945-AB — Laboratory Data Panel; Rack Mountable VC8-E — 10-Bit Point Plot Display Controller AD8-EA+AM8-EA+AM8-EC — 10-Bit A/D Converter; 8-Chan Multiplexor DK8-ES — Real-Time Programmable Clock VR14 — 7 x 9in Point-Plot CRT H960-BB — 19in Freestanding Cabinet QF060-AB — LAB8E Paper Tape Software Kit	20,000	202
LAB8E-25	System PDP-8/E-NE — Rack-Mountable PDP-8/E; 8K Memory less Teletype Control BE8-A — 20-Quad-Slot OMNIBUS Expander DECwriter — Terminal H945-AB — Laboratory Data Panel (rack mountable) VC8-E — 10-Bit Point-Plot Display Controller AD8-EA — 10-Bit A/D Converter; 8-Channel AM8-EA/EC — Multiplexor DK8-ES — Real-Time Programmable Clock VR14 — 7 x 9in Point-Plot CRT MR8-EC — 256-Word OS/8 Read-Only Memory TD8-EM — OMNIBUS DECtape Control and Dual DECtape Drive H952-HA — Programmer's Table H960-BB — 19in Freestanding Cabinet OS/8 Software Kit; OS/8 Extension Kit; OS/8 LAB-8/E Software Kit	22,600	218
	CENTRAL PROCESSORS AND WORKING STORAGE		
8A100-AC/AD	ROM Machine (with KK8-A CPU, 1K MS8-AA RAM memory; operator's panel and combination power supply, chassis, and OMNIBUS with 10 slots)	1,745	NA
8A100-AK/AL	Same as 8A100-AC/AD (except 4K RAM memory)	2,600	NA
8A100-FA/FB	Same as 8A100-AC/AD (except 1K PROM memory)	2,375	NA
8A200-AK/AL	RAM Machine (with KK8-A CPU; MS8-BA 4K RAM memory; operator's panel and combination power supply, chassis, and OMNIBUS with 12 slots)	1,995	NA
8A400-EM/EN	KK8-A CPU (with MM8-AA 8K core memory; operator's panel KM8-E memory extension control and combination power supply, chassis, and OMNIBUS with 12 slots)	2,795	43
8A400-BM/BN	CPU (with 8K core memory, 1 1KK8-A CPU; MM8-AA 8K core memory; operator's panel and KM8-AA extended option board)	2,995	44
PDP-8/E-AA/AB*	Computer (4K-core memory and Teletype control; rack mountable; slides included) KK8-E Central Processor MM8-E 4K Core Memory KC8-EA Programmer's Console KL8-E Console Teletype Control Combination Power Supply, Chassis, and OMNIBUS with 20-Quad Bus Slots	4,490	53
PDP-8/E-AE/AF*	Same as PDP-8/E-AA (except MC8-EJ 8K core memory and memory extension control)	5,650	74
PDP-8E-AS PDP-8E-AT	Same as PDP-8/E-AE (except with MM8-EJ 8K core memory added for total of 16K)	7,670	117
PDP-8/F-AH/AJ	Same as PDP-8/E-AA (with KC8-EA replaced by KC8-FL programmer's console)	3,990	53
PDP-8/F-AK/AL	Same as PDP-8/F-AH (except with memory extension control and MM8-E core replaced by MC8-EJ 8K core memory)	5,150	74

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
PDP-8/F-AS/AT	Same as PDP-8/F-AS (with MM8-EJ 8K core memory module added for total of 16K)	6,870	117
PDP8M-MH/ MJ (OEM)	CPU (with 4K core (includes KK8-E CPU, MM8-E 4K core memory; KC8-M operator's panel and combination power supply, chassis, and OMNIBUS with 20 quad bus slots)	3,200	NA
PDP8M-MK/ ML (OEM)	Same as PDP8M-MH/MJ (except with MC8-EJ 8K core memory and control)	4,000	NA
PDP8M-DH/ DJ (OEM)	Same as PDP8M-MH/MJ (except with programmer's console and KL8-E console Teletype control)	3,800	53
PDP8M-MM/ MN (OEM)	CPU with 1 MR8-FB 1K PROM Memory with 256 RAM	2,750	NA
	PROCESSOR OPTIONS		
KE8-E	Extended Arithmetic Element (EAE)	1,200	5
KP8-E	Power Fail Detector and Auto Restart	270	2
FPP12-AB	Floating-Point Processor (24 + 12 bits; supporting software requires min OS/8 configuration)	8,500	51
FPP12-AE	Double-Precision Option for FPP12-AB only (provides 60 + 12 bits capability)	2,700	16
	PDP 8A OPTIONS		
DKC8-AA	I/O opt board (includes real-time clock, 100 Hz, fixed frequency; programmer's console control, I/O interface; 12-bit parallel I/O; async serial line unit; switch selectable baud rates)	500	8
KM8-AA	Extended option board (includes memory extension and timeshare control; power fail/auto restart; bootstrap loader; switch selectable)	500	8
MR8-SL	PROM Loader	2,625	21
KC8-AA	Programmer's Console for 8/A	400	8
KC8-AB	Remote programmer's console for 8/A	550	8
KM8-E	Memory extension and Timeshare	350	2
MR8-AS	ROM Blasting (programming) Set-up Charge	150/order	—
MR8-AT	ROM Blasting Service	100/board	—
	PROM MEMORY		
MR8-FB	1K-wd PROM Memory (with 256-word RAM memory)	995	—
MR8-EC	256-wd OS/8 ROM (for TD8-E Systems)	900	5
MR8-SL	PROM Loader with cables	2,625	21
	PDP-8/A Memory Options reading		
MS8-AA	1K Semiconductor Random Access Memory (RAM) for 8/A 100)	480	NA
MR8-AA	1K Semiconductor Blastable Read-Only Memory (ROM for 8/A 100, 200, 400)	480	NA
MR8-FB	1K UV Erasable Reprogrammable Read-Only Memory (PROM for 8/A 100, 200, 400)	995	NA
MS8-BA	4K Random Access Memory (RAM for 8/A 200)	895	NA
	MEMORY OPTIONS		
	CORE MEMORY		
MM8-EJ	8K-Core Memory Expansion	3,900	
MM8-E	4K-Core Memory Expansion	2,500	
KM8-E	Memory Extension & Time-Share Control	350	
	READ-ONLY MEMORY		
MI8-E	Hardware Bootstrap Loader	540	
MR8-EC	256-Word OS/8 ROM and Bootstrap for TD8-E Systems	860	
	MASS STORAGE		
	Discs		
DF32-DP/EP	Fixed-Head Disc File and Control; 32K Wds; Controls up to 3 DS32-D Disc Expanders	7,000	32
DS32-D/E	Disc Expander (32K wds)	4,000	16
RK8-EA/EB	Disc Cartridge System (controller and 1.6M-wd drive; supports up to 3 addl RK05 drives)	7,900	74
RK05-AA/BB	Disc Cartridge Drive (1.6M wds)	5,100	64
RK05K-8	Disc Cartridge	99	—
	INPUT/OUTPUT		
	Interfaces		
KA8-E	External Interface for Positive I/O Devices (max 1/system)	270	3
KD8-E	Data Break Interface (max 12/system)	540	3
DR8-EA	12-Channel Buffered I/O Interface	540	5
	CLOCKS		
DK8-EA	Fixed Interval Clock, Line Frequency	270	2
DK8-EC	Real-Time Clock (fixed interval; crystal frequency)	320	2
DK8-EP	Real-Time Clock (programmable)	700	3
DK8-ES	Programmable, Real-time Clock (with 3 Schmitt triggers and control panel)	1,350	5

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
	TERMINALS		
	All Terminals Require KL8-JA Interface		
LT33-CC/CD	KSR 33 Keybd	1,400	32
LT33-DC/DD	ASR 33 Sync	1,850	37
LA36-CA/CB	DECwriter Data Terminal (300 cps; 132-col; 96-char uc/lc; 110, 150, & 300 baud)	1,850	
VT05B-AA/AD	A/N Display with Keybd	2,795	23
VT50-AA	DECscope Video Terminal	1,250	22
	CARD READERS		
CM8-FA/FB	Optical Mark Card Reader and Control (300 cpm)	5,290	53
CR8-FA/FB	Punched Card Reader and Control (300 cpm)	4,860	53
	PAPER TAPE		
PC8-E/EA	Combination Paper Tape Reader/Punch and Controls (rack mountable)	3,900	37
	LINE PRINTERS		
LS8-FA/FB	Line Printer and Controller	5,615	58
LV8-BA/BB	Electrostatic Printer/Plotter	11,770	53
LE8-VA/VD	Line Printer and Controller	9,900	72
LE8-WA/WD	Line Printer and Controller	11,900	72
	MAGNETIC TAPE		
TA8-AA/AB	DECcassette System	2,990	40
TD8-EH	OMNIBUS DECtape Control and Single DECtape Drive	4,000	32
TD8-EM	OMNIBUS DECtape Control and Dual DECtape Drive	5,500	42
TM8-EA/ED	DEC Magtape Drive and Controller (9-track)	10,745	101
TM8-FA/FD	DEC Magtape Drive and Controller (7-track)	12,500	101
	PLOTTERS		
XY8-E	Plotter Control Module Only	540	8
XY8-EK/EL	Incremental Flatbed Plotter and Control	3,995	23
XY8-EH/EJ	Incremental Flatbed Plotter and Control	3,995	23
	GRAPHIC DISPLAYS		
	DISPLAYS		
VC8-E	Point-plot Display Control	1,185	11
VR14	CRT Display (7 x 9in point-plot)	3,240	19
	DATA COMMUNICATIONS		
KL8-JA	Async Serial Line Interface	425	11
KL8-M	Modem Control Interface (for Bell 103 and 202 modems)	400	5
H308	Null Modem Adapter (needed when a modem is not used)	65	—
DP8-EA	Sync Modem Interface (for Bell 201 modems)	1,620	11
DP8-EB	Sync Modem Interface (for Bell 300 modems)	2,000	11

— Not Applicable
NA Not Available
NC No Charge

HEADQUARTERS

Digital Equipment Corp.
146 Main St.
Maynard MA 01754
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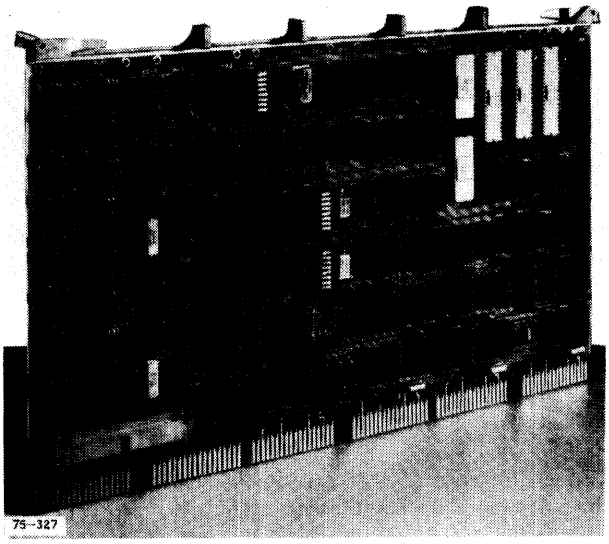
DIGITAL EQUIPMENT
PDP-8 System Report Update



Digital's KL8-A Four-Channel Multiplexor

MS800 or System 800

Four-Channel Multiplexor

The KL8-A, a four-line serial asynchronous multiplexor for the PDP-8/A, offers partial modem control for three lines and full modem control for one line. The multiplexor gives small PDP-8/A systems multiple-terminal capability; it allows them to operate as a miniconcentrator, intelligent terminal, or cluster controller. The KL8-A includes a 32-character silo (First In, First Out receive buffer) and a branch addressing scheme to provide vectored interrupts for the four lines. Only one PDP-8/A OMNIBUS slot is needed for the KL8-A.

Purchase price is $995, and the unit is available 60 days after the order is received by Digital.

System 800 (or MS800) Announced

System 800 is a new PDP-8/A computer package for the OEM market for office computers. The system is housed in a desk with a dual floppy disc drive unit, and it operates under OS/8 control. The processor features power fail/auto restart, real-time clock, and both a serial and parallel I/O interface. Memory capacity is 8K or 16K 12-bit words. The system can be configured with the VT50 Series of Digital's video terminals or with the LA36 DECwriter terminal printers. ROM-based diagnostics are automatically run to check out the system each time it is turned on.

The system is designed to operate as a stand-alone system or as a remote station in a computer network.

Two models are currently available:

- MS800-A with 8K words of memory; priced at $8,995.
- MS800-B with 16K words of memory; priced at $9,995.

Quantity discounts are available for both models. Deliveries are scheduled for 60 days after receipt of order.

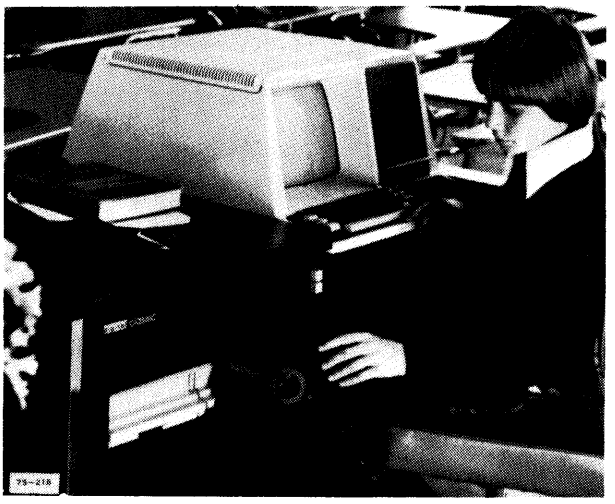
CLASSIC™ and CMS/I

Three entry-level hardware/software packages are based on the PDP-8/A: the DEC Datasystem 300 series for business data processing, CLASSIC™ (Classroom Interactive Computer) for educational institutions and CMS/1 (Computational Minicomputer System) for construction, civil, aerospace, and other engineers within departments of companies or government agencies. The packages are built around a PDP-8/A processor with core memory, dual diskette drives, VT50 display system and PDP-8 software. Table 1 shows CLASSIC and CMS/1 characteristics. The DEC Datasystem 300 series is covered in Small Business Computers, report number 140.3451.080.

TM Trademark of Digital

CLASSIC consists of a PDP-8/A with 16K words of core memory; a VT50 CRT console with keyboard and printer; dual diskette drive unit; and OS/8 operating system with BASIC. The system has no standard options other than FORTRAN IV and the CLASSIC Curriculum #1 and Applications #1 software packages.

The Curriculum #1 package is for secondary schools. It includes computer-aided instruction (CAI) programs for up to 97 texts in mathematics, social science, science, and business studies.



Digital's CLASSIC

The Applications #1 package is primarily for higher-education institutions (above 12th grade). It includes user-submitted programs in FORTRAN and BASIC for three major application areas: mathematics, statistics, and business. Programs are designed for students as well as teachers.

CMS/1 consists of a PDP-8/A with 16K words of core memory, VT50 CRT console with keyboard and display, dual diskette drives (capacity of 670,000 characters), and OS/8 operating system with both BASIC and FORTRAN IV. Optional features include a second diskette drive, an electrolytic printer for the VT50 console, LA36 DECwriter II, and COGO (Coordinate Geometry) applications software. Both the CMS/1 and CLASSIC systems will be delivered 180 days after receipt of order.

The CLASSIC and CMS/1 systems are aimed at markets that Digital has traditionally served well. Major competition comes from Hewlett-Packard and Data General.

Since older Digital EDU systems and engineering systems cost considerably more than CLASSIC and CMS/1, they usually had to be timesharing systems for institutions or engineering departments of companies to justify their cost. Many more schools and engineering departments can afford a CLASSIC or CMS/1 system because the cost is low. In fact, schools may even be able to afford multiple CLASSIC systems within a single classroom. Individual engineers may have personal computers. Undoubtedly, the computers to people ratio will increase.

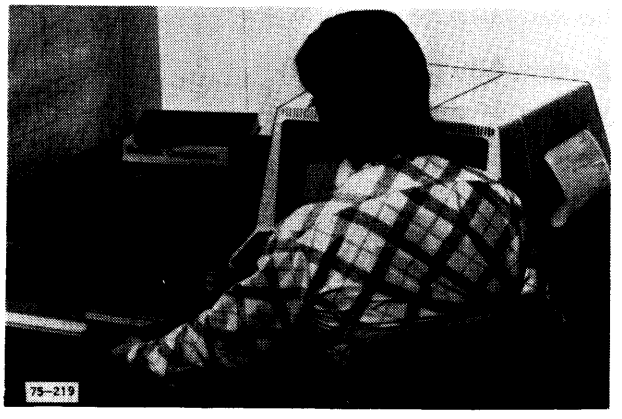
Furthermore, Digital is marketing CLASSIC and CMS/1 as total systems, with applications software drawn from the DECUS (Digital Equipment User Society) library. These software packages, developed by PDP-8 users, have been put together into coherent applications modules which the company will now support.

The PDP-8 is unique in the minicomputer industry in the amount of applications software that has been programmed for it. Much of that software resides in the DECUS library. Furthermore, Digital has long nurtured and supported DECUS, which is also unique among user's groups because of its organization and vitality. Thus, more user software will undoubtedly be added to the DECUS library.

CLASSIC and CMS/1 are well-thought-out systems, which are based on Digital's strengths. They are aimed at markets that Digital knows well, and use hardware compatible with the PDP-8 (the longest-lived minicomputer), for which an almost endless source of software is available. The systems are tightly bundled, for Digital at any rate, to keep the system cost so low that competitors will have a hard time meeting it. Furthermore, by moving system cost downward, the company considerably increases the market for these systems. Thus, the CLASSIC and CMS/1 systems appear to be ideal Digital products and destined for success.

Unbundled PDP-8/A

Digital's PDP-8/A-100 and PDP-8/A-400 processors are now available on a board-by-board, building-block basis. The PDP-8/As were unbundled so they could be used in such applications as optical character recognition,



Digital's CMS/1

Table 1. Digital Equipment PDP-8: CMS/1 and Classic

Characteristic	CMS/1	CLASSIC
CPU	PDP-8/A	PDP-8/A
Memory		
Type	Core	Core
Size	32K char*	32K char*
Cycle Time		
Diskette	2 or 4 drives	2 or 4 drives
Use	Mass storage	Mass storage
Capacity	670,000 to 1.34M	670,000
Speed	NA	NA
Disc Storage		
Type	—	—
Capacity	—	—
Average Access time	—	—
Console		
Keyboard	Typewriter kybd, numeric pad, & 24 function keys	Typewriter kybd, numeric pad, & 24 function keys
Display	12 lines, 80 char each	12 lines, 80 char each
Printer	Opt	Std
Line Printer	30 cps DECwriter II	No
DATA COMM	No	No
Data Entry	Console	Console
Software		
Operating System	OS/8	OS/8
Language	BASIC; FORTRAN IV	BASIC; FORTRAN IV
Applications	Applications Package with COGO (opt)	Applications #1 (opt #1 (opt)
Minimum Price $	12,000	7,900
First Delivery	180 days ARO	180 days ARO

Notes:
Using standard interchange format
* 6 bits

patient monitoring, and communications, with low-end computing requirements.

The basic semiconductor-memory configuration includes the central processor, 1K-word semiconductor RAM, 2K words of ROM, and a 6-slot OMNIBUS™. This configuration sells for $1,830 in single quantities and for $1,309 in quantities of 20. The typical core configuration includes the CPU with 8K words of core, memory extension, time-share control, bootstrap loader, power-fail/auto-restart, and the 6-slot OMNIBUS.

AD8-A Analog-to-Digital Subsystem

The AD8-A, a compact analog-to-digital converter subsystem, is now available for use with all the PDP-8 minis. The converter subsystem consists of a 10-bit analog-to-digital converter, 16-channel multiplexor, and a sample-and-hold circuit. Programming for the new model is compatible with the AD8-E analog-to-digital converter now available. The unit is supported under LAB8/E paper tape software, and the OS/8 operating system under BASIC. The maximum program control sampling rate is 28K Hertz. The input range is program-selectable for unipolar (0V to +5V) or bipolar (-2.5V to +2.5V) operation. The AD8-A is priced at $1,000 for a single unit and $710 in 20-unit quantities.

RX8 Floppy Disc System

Digital has also introduced RX8, a new low cost floppy disc system for the PDP-8. The system has a capacity of 256K bytes or 128K 12-bit words and an average access time of 483 milliseconds. RX8 is available in single- and dual-drive configurations and is supported by extensive diagnostic and operating system software.

RX8 data operations are handled in either byte mode or 12-bit word mode. Preformatted industry-compatible diskettes with 77 tracks, 26 sectors per track are used with the system, which fits into a standard 19-inch rack. Only the head contacts the surface during reading and writing, prolonging disc life. RX8 can be used for input-output or, for small configurations, as random access files.

A single disc configuration sells for $2,900 and a dual-disc drive for $3,900. Diskettes for the model cost $40 for 5-diskette lots or $75 in 10-diskette lots. The RX-8 subsystem is available 30 days after the order is received.

RTS/8 Real-Time Operating System

The RTS/8, an event-driven, a real-time operating system, is now available to run on a minimum configuration with only 4K words of main memory; a memory-resident executive requires less than 700 words of core or semiconductor memory.

A PDP-8 with only 12K words of memory can support a full foreground/background system. Real-time events can be controlled and programs developed concurrently via the OS/8 operating system.

RTS/8 controls up to 63 tasks on a fixed priority basis. Tasks can be stored in memory or on disc and swapped in when needed. Support tasks provide for a variety of peripherals, including analog-to-digital devices, discs, magnetic tape, printers, and monitor units.

The new operating system is memory efficient and reduces software development costs, according to Digital. It supports features such as dynamic task scheduling, multiprogramming, multiple buffered I/O, intertask communication, on-line operator control, and foreground/background processing. The small size of the RTS/8 executive permits the operating system to be used in cost-sensitive applications.

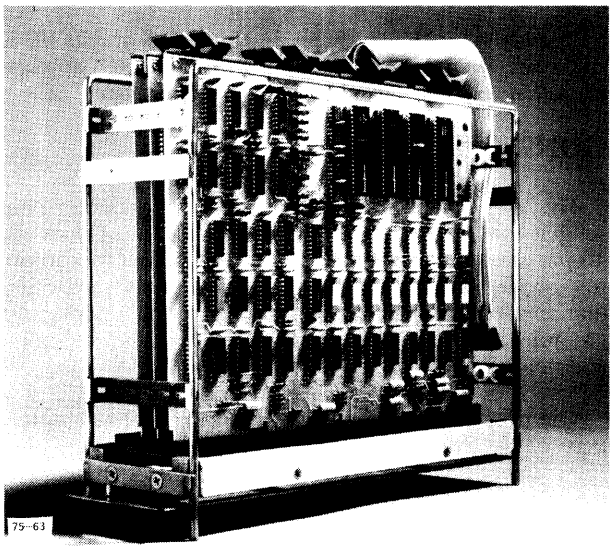
The price of RTS/8 is $500 for a single-user license. RTS/8 and OS/8 together cost $750. For OEM customers, a multi-use license is available.

PRICE DATA

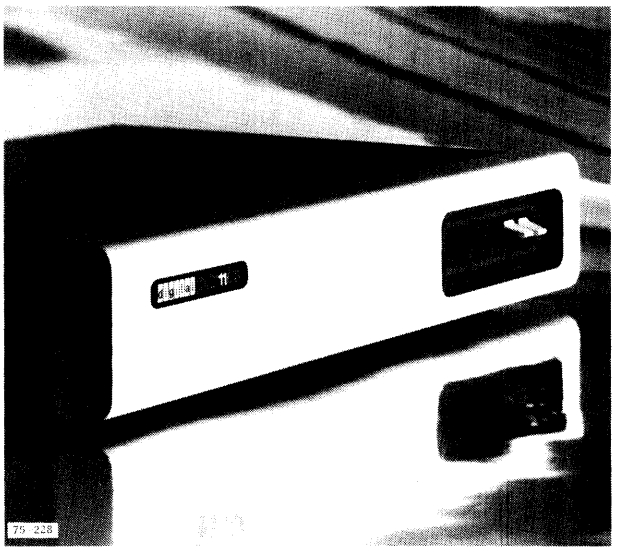
Identity	Purchase Price $	Monthly Maint. $
CMS/1	12,000	115
Copier(1)	500	
Second Diskette Drive	3,500	
CMS/1 Applications Package (one-time charge)	395	
CLASSIC	7,900(2)	115
FORTRAN IV option (one-time charge)	700	
Curriculum Package #1 (one-time charge)	395	
Applications Package #1 (one-time charge)	395	

Notes:
(1) Unavailable as separate item.
(2) Non discountable; also available under 5- to 7-year full payout lease.

DIGITAL EQUIPMENT CORPORATION
LSI-11 System Report



Digital LSI-11



PDP 11/03

OVERVIEW

With the introduction of the LSI-11, Digital continues to reaffirm the company's policy of providing more computing power at less cost. This new entry in the popular PDP-11 product line (over 17,000 installed) occupies a unique position; it is a microcomputer that implements the PDP-11/40 instruction set and offers the performance of the PDP-11/05. In quantities of 100, an LSI-11 processor with 1200-nanosecond processor cycle time, I/O bus, 4K-word MOS random-access memory (RAM), real-time clock, single-level interrupt, and power fail/auto restart for stand-alone operation costs $684. All components are mounted on one 8.5 by 10-inch board. A core LSI-11 is available configured on two 8.5 by 10 inch boards. Purchase price for the core version in 100-unit quantities is $983. The LSI-11 microcomputer is aimed at OEM or large volume end-user markets.

Digital has also announced a boxed version of the LSI-11 aimed at single unit users. Called the PDP-11/03, the system contains a processor with 4K words of MOS RAM memory, a serial interface, power supply, rack mountable enclosure and an operator's front panel; it is available in both 115 and 230VAC models. A configuration with core memory is also available. The purchase price of the MOS RAM boxed configuration is $2,495 while the price of the core 11/03 is $2,925. Table 1 lists mainframe characteristics.

The KD11-F, the LSI-11 processor, is contained on four 16-bit, N-channel metal oxide semiconductor chips, manufactured by Western Digital, an independent calculator manufacturer. The processor contains eight general purpose registers. Extended arithmetic, serial line interface module, parallel line interface mode, and four expansion memory modules are available options. The bus structure is similar to the PDP-11 UNIBUS in that the highest priority device is located closest electrically to the microcomputer, but the LSI-11 bus and the PDP-11 bus are not compatible. A paper tape operating system, resident as a basic utility, provides the software for the LSI-11. Programs can also be developed on other PDP-11 systems via an Emulator package that runs on the PDP-11/35 and 40. The first LSI-11 deliveries have already been made.

COMPETITIVE POSITION

The LSI-11 system is aimed at the OEM market and high-volume end users. It is designed for easy interfacing to machines, instruments, and terminals. Digital expects to penetrate markets in business, communications, education, health, industrial control, laboratory automation,

HEADQUARTERS

Digital Equipment Corp.
Components Group
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Marlborough MA 01752
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Table 1. Digital Equipment Corporation LSI-11: Mainframe Characteristics

MODELS	
CENTRAL PROCESSOR	KD11-F
Microprogrammed	Yes
No. of Registers	6 general, 1 stack pointer, 1 program counter
Addressing (no. of wds)	
Direct	32K
Indirect	32K
Indexed	32K
Mapping	No
Instruction Set	Same as PDP-11/40
Implementation	Microcode
Types	Singleword
Number	400
Floating Point	Opt
Hardware Stack	Yes
Instruction Execution Times (μsec)	
Fixed Point	
Add	3.5 (reg to reg); 12.0 (memory to memory)
Multiply	24-64 (memory to reg)
Divide	78 (memory to reg)
Floating Point(1)	
Add/Subtract	42.0
Multiply	52-92
Divide	151
Writable Control Store	No
Interrupts	
Levels	1
Type	Hardware
Processor Cycle Time	1.2 μsec
MAIN STORAGE	
Type	RAM; core; PROM/ROM
Speed	350 nsec access time (RAM); 900 μsec cycle time (core); 40 nsec access time (PROM/ROM)
Basic Addressable Unit	Byte/word
Bytes/Access	2
Cache Memory	No
Capacity (bytes)	
Min	8K (RAM); none (core); none (PROM/ROM)
Max	64K (RAM); 64K (core); 8K (PROM/ROM)
Increment Size (bytes)	2K/8K (RAM); 8K (core); 512K/1K (PROM/ROM)
Ports/Module	1
Error Checks	No
Memory Protection	No
Memory Management	No
Interleaving	No
INPUT/OUTPUT	
Max Devices Addressable	No practical limit (4,096)
Programmed I/O	Yes
DMA	Yes
DMA Transfer Rate	833K wds/sec
Price	$634 in quantities of 100

Note:
(1) Two-word operands.

process control, and transportation. The boxed PDP-11/03 is aimed at individual end-users.

Although the LSI-11 uses the PDP-11/40 instruction set, it is a horse of another color. The LSI-11 offers a challenge more to the microcomputer manufacturers, such as INTEL, than to minicomputer manufacturers. Only Computer Automation with its Naked Mini/Milli systems competes in this market. Thus, Digital has chosen to halt the microcomputer encroachment on the low end of the minicomputer market by expanding the processing power of the PDP-11 line downward.

The LSI-11 is slower than minicomputers and its I/O is rudimentary. It is ideal, however, for dedicated applications that require power but relatively low speed.

CONFIGURATION GUIDE

The Western Digital metal oxide semiconductor chip set that contains the LSI-11 central processor includes one 40-pin control chip, one 40-pin data chip, and two 40-pin microcoded microms (microcoded read-only memories) that emulate the PDP-11/40 instruction set. A socket for an optional fifth chip to implement extended fixed-point and floating-point arithmetic is provided.

The processor contains eight general purpose registers that can serve as accumulators, index registers, autoincrement registers, autodecrement registers or as stack pointers for temporary data storage. Registers are not usually dedicated. Register 6 serves as the hardware stack pointer and indicates the address of the last entry in the stack; register 7 is the program counter, indicating the address of the next instruction to be executed. The upper 4,096 addresses are reserved for peripheral device addressing. Memory addresses are structured in the remaining 0-28K with addresses from 0-376 reserved for traps and interrupt vector locations. The processor cycle time is 1.2 μ sec.

Both Direct Memory Access (DMA) and Programmed I/O (PIO) transfers can take place. The transfer rate over DMA is 833K words/second.

Basic memory is a 4K-word MOS RAM, but expansion memory modules are also available: 4K-word core memory, 1K-word static RAM, 4K-word dynamic RAM, and 4K-word programmable read-only memory (PROM/ROM) available in 256- and 512 word increments. Memory cycle time is 350 nanoseconds for the RAM version and 900 nanoseconds for the core.

The microcomputer can support two I/O modules and four expansion memory serial interface modules. The I/O modules are the DLV11 serial module and the DRV11 parallel module.

The DLV11 provides for 20mA current loop or EIA interfaces. Jumper-selectable transmission rates (50 to 9,600 baud) and codes are available. The DLV11 is pin, signal, and software compatible with the DL11C interface available on other PDP-11s.

The DRV11 is a general-purpose, 16-bit parallel interface between the LSI-11 bus and a peripheral device. The DRV11 is pin, signal, and software compatible with the DR11-C available for the other PDP-11s.

Software consists of a paper tape operating package. It includes an assembler, an editor to create and modify ASCII source files for input to system programs, loader, on-line debugging package, and I/O executive. Programs can also be developed on other PDP-11 systems via an Emulator package that runs on the PDP-11/35 and 40, which have instruction sets identical to the LSI-11. The configuration must include a PDP-11/35 or 11/40 processor with 16K-word memory, memory management control option, disc storage, paper tape reader/punch or cassette tape, and printer or CRT terminal.

The LSI-11 I/O bus is not compatible with the UNIBUS although it is functionally similar in that I/O device registers are addressed as memory locations. The device located closest to the microcomputer has the highest priority.

Currently, only serial devices, such as a Teletype unit, can interface to the LSI-11 as a peripheral device. Special devices can connect to the parallel interface. Digital will provide more I/O interfaces in the future for other devices such as mass storage units.

Initially, the LSI-11 must be program loaded from ROM, from a host computer, or from a mass storage device supplied with a turnkey system.

TYPICAL PRICES

Model Number	Description	Purchase Price - $*
	Processors	
PDP-11/03	System includes 16-bit silicone gate N-channel, MOS LSI processor with memory, serial interface, power supply, rack mountable enclosure, operator's front panel	2,495
	With 4K words core memory	2,925
KD11-F	Microcomputer Module System (includes CPU; 4K x 16 random access memory; 16-bit I/O port; power fail/ auto restart; real-time clock input; automatic priority interrupt arbitration; vectored interrupt handling; 8.5 x 10-in. board)	990
KD11-J	Same as KD11-F except with multiple board configuration of two 8.5 x 11-in. boards	1,536
	Memory	
MRV11-AA	PROM/ROM Memory Unit (includes 31 IC sockets; accepts 256 x 4 or 512 x 4 fusible link memory device; accepts masked ROM device; max capacity to 4K x 16)	175
MSVII-A	1K x 16 Random Access Memory (static RAM)	475
MSVII-B	4K x 16 Random Access Memory (dynamic RAM)	625
MMVII-A	4K x 16 Core Memory	625
	Processor Options	
H9270	Backplane Assembly	175
KEVII	Extended Arithmetic Chip	125
MRV11-AC	Fusible Link Unprogrammed PROM Chip (512 x 4 array size)	35
	Interfaces	
DRV11	Parallel Interface Unit	195
DLV11	Serial Interface Unit	235
	Software	
QJV10-AB	Paper Tape Software Package (includes editor, assembler, loader, debugging package (ODT); input/output exerciser (IOX))	100
QPV10-AE	Emulator Software Package (runs under RT11 on PDP-11/34/40 system; includes editor, assembler, linker, debugging program, load package, save package, execute package)	500

*Quantity discounts available. Prices quoted are for quantities of 1-49.

DIGITAL EQUIPMENT CORP.

LSI-11 System Report Update

The PDP-11/03 is an end-user, boxed version of the LSI-11 microcomputer. Both MOS/RAM and core memory configurations are available. The PDP-11/03, which includes the LSI-11 processor, 4K words of MOS/RAM memory, serial interface, power supply, rack-mountable enclosure, and operator's panel, costs $2,495. The comparable core memory version costs $2,925.

Options available for the PDP-11/03 include an extended arithmetic chip, serial line interface module, parallel line interface module, and four expansion memory modules: 4K-word RAM, 1K-word RAM, 4K-word PROM/ROM, and 4K-word core. The unit measures 3½ by 19 by 13½ inches and weighs 35 pounds. First delivery was in September 1975.

The MU/11V03 Microcomputer Timesharing System

NEW MICROCOMPUTER TIMESHARING SYSTEM MU/11V03

The MultiUser/11V03 is a transportable, programmable system that can support up to four users simultaneously. Users can write and execute programs in BASIC, FORTRAN IV, or MACRO assembly language, all of which run under the RT-11 real-time operating system. Programs developed on the MU/11V03 can run on any PDP-11 System. Terminals can be located up to 25 feet from the system with basic hardware. Connection to remote terminals requires a DFOL interface.

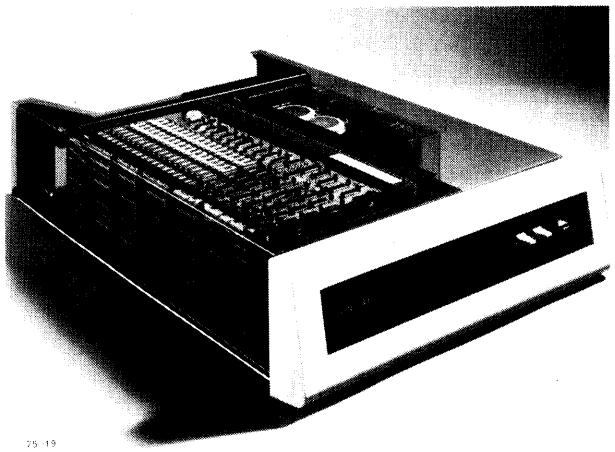
The MU/11V03 includes the PDP11/03 microcomputer, dual RX11 floppy discs (RX11-BX) with 512K-byte capacity, up to 56K bytes of MOS/RAM memory, expander box, power supply, extended instruction set/floating-point instruction set, and a LA36 DECwriter or VT52 display terminal connected via a serial line interface. Up to three additional terminals can be supported. These can be LA36 DECwriters, VT50 or VT52 Display Terminals, or a VT55 Graphics Terminal with or without hard copy.

The MU/11V03 is housed in a cabinet on rollers; the cabinet is 25 inches high, 19 inches wide, and 25 inches deep and weighs about 200 pounds. Initially, Digital plans to market the MU/11V03 in the education field for computer usage training; computation and problem-solving in science, mathematics, and engineering; simulation of physical and social conditions; and computer-aided instruction in mathematics and languages.

The MU/11V03 is sold or leased bundled. Lease/purchase plan is for a 5-year full payout lease.

PRICE DATA

Model Number	Description	Purchase Price $	Lease/ Month $
MU/11V03	System for one terminal includes	16,220	472
11/03XX	LSI-11 CPU with 4K x 16 MOS memory, cabinet, power supply		
RX11-BX	Dual flexible disk unit		
MSV11-B	4K x 16 MOS add-on memory (6 modules)		
BA11-ME	Expander box and power supply		
KEV11	Extended instruction set/floating-point instruction set		
LA36 or VT52	Terminal (console) serial line control—20 ma or EIA (CCITT). Can be connected remotely via DF0L interface		
Three additional terminals can be selected from the following:			
VT50-AA	12-line CRT	1,250	
VT52-AA (AB)	24-line CRT	1,995	
LA36-CA (CB)	30-CPS hard copy	2,175	
VT55-AA (AB)	Graphics terminal	2,495	
VT55-BA (BB)	Graphics terminal w/hard copy	3,295	
SOFTWARE			
RT11	Operating system	NC	
BASIC	Compiler and interpreter	NC	
MACRO	Assembler	NC	
FORTRAN IV	Compiler	700	



OVERVIEW

PDP-11, Digital's 16-bit minicomputer, was introduced in January 1970 with the announcement of the PDP-11/20. Since then, Digital has continued to expand the line at both the upper and lower ends until it covers most of the market up to a range of medium-scale general-purpose computers. Digital directs most systems to both the OEM and end-user markets.

A basic processor design frequently has two possible model numbers, a number ending in zero if it is an end-user system or a number ending in 5 if it is an OEM system. Thus, Models 11/05, 11/15, and 11/35 are the OEM equivalents of Models 11/10, 11/20, and 11/40, respectively. Although no OEM model numbers have been assigned, the 11/45 is available in both OEM and end-user versions. The PDP-11/50 is a PDP-11/45 that uses MOS semiconductor solid-state memory for main memory. The PDP-11/04 is an 11/05 that uses a 725-nanosecond MOS memory and MSI circuitry to achieve small size and low cost. In general, model numbers reflect processing power, with lower numbers for smaller, slower speed, less powerful systems and higher numbers for faster, larger, more powerful systems.

The PDP-11/40 and its companion model 11/35 were logically like the 11/20 and comparable in price, when introduced. The 11/40, however, has an expanded instruction set, one additional optional processor mode (two modes total), and a larger memory capacity than the 11/20, as well as optional hardware for floating-point arithmetic and memory management. Therefore, it has replaced the slower 11/20 as the backbone of the PDP-11 line because it offers higher performance at the same cost. Digital no longer actively markets the 11/20, or its OEM equivalent, the 11/15.

The PDP-11/45 and 11/50 are major upward expansions of the PDP-11 line and offer many features unavailable for the other models, including semiconductor bipolar or MOS memory and three processing modes. They are designed for applications requiring large memories, fast computation speeds, or multiprocessor configurations.

PDP-11/45 and 11/50 memory segmentation option is functionally similar to the 11/35 and 11/40 memory management option although it differs in some respects because of the larger number of registers and processing modes on the 11/45 and 11/50. Memory segmentation (memory management) provides virtual addressing for memories larger than 28K words; it also provides a means of memory protection for multiprogramming environments.

At the low end of the line, the 11/04, which is the newest member of the series, keeps the line competitive with very small low-cost OEM systems. These have been the first to benefit from the new MOS and microprocessor technologies and frequently have the CPU on a single board.

The PDP-11 line has three characteristics that distinguish it from other computers in its class: the UNIBUS, multiple general-purpose registers, and the manner of handling I/O operations. Like many of the newer systems on the market, later models are microprogrammed.

All PDP-11 models except the PDP-11/45 and 11/50 are organized around a single fast UNIBUS that connects all system components. The processor, memory, and peripheral devices operate as UNIBUS subsystems; the processor allocates UNIBUS time to system components, which communicate with each other in a master-slave relationship.

The distances between devices and the speeds of the connected devices are immaterial because of the master-slave communications technique. This arrangement means, for example, that memory modules with different speeds can be connected to a system.

A single UNIBUS inherently limits system speed to that of the UNIBUS because units in the system must time-share it. The PDP-11/45 and 11/50 overcome this limitation by using a second bus between solid-state memory and the CPU. Also solid-state memory has two ports of entry; one port can connect to one CPU and the other port to a second CPU. Thus, solid-state memory can be shared by two processors.

All PDP-11 processors have at least eight general-purpose registers, which can be used as accumulators, address or stack pointers, or index registers. Two registers have special functions as well: one is the program counter, and the other is a hardware stack pointer for interrupt handling. The PDP-11/35 and 11/40 have two stack pointers for interrupt handling, one for each of the two processing modes; thus, a program can use only the pointer associated with its processing mode. The general-purpose registers are versatile and are used to implement a powerful addressing scheme, which makes stack manipulation easy.

The PDP-11/45 and 11/50 have 16 general-purpose registers: 12 are dual sets of six registers used for accumulators, address or stack pointers, and index registers; three

are hardware stack pointers that handle interrupts for the three processor operating modes; and one register is the program counter. The 11/45 and 11/50, like the other PDP-11 processors, have only one program counter.

All PDP-11 processors address I/O device registers as memory locations; thus, the entire instruction set can be used to operate on data or control information held in those registers. Memory addresses 28,672 to 32,767 are reserved for I/O register addressing, so maximum main memory for a basic system cannot exceed 28,672 words. Memory to 124K words is available as an option on the 11/35, 11/40, 11/45, and 11/50 and by special order on the other systems.

Digital provides a comprehensive range of peripherals for its PDP-11 line: conventional paper tape and punched card I/O units including a mark sense card reader; DECtape as mass storage for small systems and industry-standard magnetic tape devices for larger storage requirements; fixed-head disc units and movable-head disc cartridges for larger systems; graphic subsystems; special-purpose subsystems to handle analog/digital and digital/analog and digital I/O for data acquisition and control applications; and a broad range of communication interfaces for data communications environments.

Software support for the PDP-11 is substantial. Software packages currently offered include a Paper Tape Software System and a Cassette Programming System (CAPS) for small configurations, Resource Time-Sharing System (RSTS), Disc Operating System (DOS), two Real-Time Multiprogramming Systems (RSX-11 M and D), and a smaller single-user real-time system (RT-11), a Communications-Oriented Multi-Task Executive (COMTEX-11), and others. Current languages supported are the PAL-11 and MACRO-11, assembly languages, FORTRAN IV, FOCAL, BASIC Plus, and COBOL. These packages support small stand-alone systems, time sharing, batch processing, real-time multiprogramming, communications applications (including 2780 and 2788 emulation for front-end and concentrator configurations), graphics, and laboratory applications.

Table 1 lists system specifications common to all models and Table 2 lists the chief differences among models.

Competitive Position

PDP-11 is a major minicomputer system from the leading minicomputer manufacturer—it is the system against which all other minicomputers are compared in the marketplace.

Digital was slow to enter the 16-bit minicomputer field, having a large investment in its popular 12-bit PDP-8 line and 18-bit PDP-9/15 line. By the time the PDP-11 was introduced, the design for most 16-bit minicomputers had stabilized and included a paging addressing scheme, priority interrupt system, programmed I/O, and direct memory access channel.

Table 1. Digital PDP-11: Characteristics Common to All PDP-11s

ADDRESSING	
Direct (no. of words)	None (always through internal registers)
Indirect	Yes
Indexed	Yes
INPUT/OUTPUT	
Programmed I/O	Yes
DMA Channels (no.)	1 (any no. of devices per channel)
Multiplexed I/O (no. of sub-channels)	None
MEMORY	
Parity	Option
Basic Addressable Unit	Byte or word
Bytes per Access	1 or 2
DECIMAL ARITHMETIC	No
MICROPROGRAMMED	All models except 11/15 and 11/20

PDP-11's design was radically different, incorporating features not provided in most other systems, such as the UNIBUS that connects all units in the system; multiple internal general-purpose registers used as accumulators, index registers, address and stack pointers and special-purpose registers (program counter and interrupt pointer); and I/O registers that operate like memory locations. Thus, Digital asserted itself as the trend-setter, leaving other manufacturers to follow its lead or to compete by using minicomputers with designs that could rapidly become obsolete.

To date, only a few minicomputer manufacturers have introduced systems similar to the PDP-11. The GRI-909 and the Lockheed SUE resemble PDP-11 somewhat, in that they have a universal bus comparable to the UNIBUS. The cost of developing totally new system software has probably prevented other manufacturers from departing from traditional designs. In addition, the single-bus architecture has some major drawbacks for real-time applications that require many I/O operations. Even for large configurations, a second bus is unavailable except for solid-state memory modules.

Major PDP-11 competitors are the Data General ECLIPSE; General Automation 16 Series; Honeywell System 700; Hewlett-Packard 21MX Series; Varian V70 Series; PRIME 100, 200, 300; MODCOMP I, II, and IV; Xerox 530; and Digital's own PDP-8. Hewlett-Packard's powerful HP 3000 competes directly with the PDP-11/45 and 11/50. Other systems compete in specific application areas where they provide strong system support.

The PDP-11 is a formidable competitor. Its members cover a broad range of processor power, with each larger system upward compatible with smaller systems in the line. The software support also covers a broad range, from small systems using the RT-11 operating system to large configurations with 124K words of memory and the

Table 2. Digital PDP-11: Differences Among PDP-11s

Model	PDP-11/04; 11/E05; 11/05; 11/10	PDP-11/15; 11/20; 11/R20	PDP-11/35, 11/35F; 11/40	PDP-11/45; 11/50
ARCHITECTURE				
CPU Models	KD11-B	KC11; KA11; KAR11	KD11-A	KB11
Microprogrammed	Yes	No	Yes	Yes
G-P Registers	8	8	9	16
Buses	UNIBUS	UNIBUS	UNIBUS	UNIBUS + semiconductor memory bus
Automatic Priority Interrupts	Multiline, multilevel	Single-line, multilevel	Multiline, multilevel	Multiline, multilevel + 7 software levels
Stack Size	Fixed	Fixed	Fixed std; variable opt	Variable
Floating Point	Software	Software	Hardware opt	Hardware opt
MEMORY				
Types	Core (11/05, 11/10); MOS (11/04)	Core	Core	Core/MOS/bipolar
Capacity (words)				
Min	4,096	4,096	8,192	16,384
Max	28,672	28,672	126,976	126,976
Increment Sizes (words)	8,192; 16,384;	8,192; 16,384	8,192; 16,384	1,024; 4,096; 8,192; 16,384
MEMORY				
Management Hardware	No	No	Yes, opt	Yes, opt
Memory Protect	No	No	Opt	Opt
Cycle Time (μsec)				
Core	0.90, 0.98	0.90	0.90, 0.98	0.90, 0.98
MOS	0.725 (11/04 only)	–	–	0.495
Bipolar	–	–	–	0.300
INSTRUCTIONS				
Overlapped	No	No	Yes	Yes
Extended Arithmetic	Opt	Opt	Opt	Std
Std Instruction	Basic	Basic	Basic + XOR, SOB, RTT, MARK, SXT	11/40 set + MUL, DIV, ASH, ASHC, SPL
No. (std; opt)	70; 4	70; 4	70; 10	83; 50

RSX-11D Operating System. User programs in a multiprogramming environment can use up to 32K words for program space and 32K words of data space. Also, the PDP-11 is a relatively new system from the largest minicomputer manufacturer; thus it is still in the growth period of its life cycle. Digital will continue to enhance the line with both software and hardware.

The one disadvantage that Digital has in relationship to the large computer manufacturers is that the company still does not lease its computers. This decision deters some potential users who do not wish to make the total commitment of buying a system. It also means Digital does not have a solid rental base for steady income. So far, this has not thwarted Digital's growth although it is difficult to believe that the market for minicomputers can continue to grow at its current rate. As the minicomputer manufacturers market to less sophisticated users and to smaller companies, leasing will become more of a competitive factor.

User Reactions

Interviews with several PDP-11 users to get sample responses to the systems produced information on a wide variety of applications since some users have several systems, each used for different purposes. A southern telephone company uses one PDP-11/45 with a 48K-word memory for I/O preprocessing and media conversion to magnetic tape. A second, disc-based (300M bytes total) 11/45 polls two computers, which in turn poll 500 terminals for sales and delivery data — also converted to magnetic tape that feeds into a CDC 3301. A large university laboratory has a disc-based PDP-11/45, a core-based 11/40, and a core-based 11/15, each running different instruments and experiments. The 11/45 is used for program development for the other two, and also to communicate with Brookhaven's CDC 6600. A large research institution also uses a PDP-11/40 with one disc to tie into Brookhaven's computer, as well as to run a graphics display. A steel company has two 11/20s and four 11/10s, all used

for automatic gauge control on rollers/reversers. A large oil company uses a PDP-11 with 16K words of memory to poll 48 terminals to obtain delivery and service information from all over the country.

Users seem to agree that the PDP-11 CPUs are reliable, and service is prompt. Promptness is variously defined, of course; one user, who is 600 miles from the nearest service center, feels that a 1- or 2-day response time is pretty good. Universally, the CPU is praised for reliability, but some users have found problems with various I/O components that must be adjusted. The steel company, for instance, had some trouble with a power supply that eventually had to be replaced. The steel company does its own maintenance, and complains that, under these circumstances, it does not receive news about field engineering changes, such as a new power supply. The company feels that the UDC (Universal Digital and Analog Subsystem Controller) interface could use some design work because the large circuit boards are unwieldy and difficult to change.

Users universally feel the system software is efficient and proves to have no unexpected bugs. One user at the university chemistry laboratory would like to see Digital develop a high-powered time-sharing system that would allow multiple interactive terminals for users to develop and execute programs in FORTRAN or a similar high-level language. A user at the university laboratory says that the 11/45 hardware could clearly support this type of a system but system software is needed. The user at the research institute is delighted that the system is considerably more powerful than expected, and has found that it can do more and more of its calculations at the satellite, instead of using the remote Brookhaven system as originally intended.

Configuration Guide

A PDP-11 system consists of a processor, UNIBUS, memory ranging in size from 4,096 to 28,762 words (126,976 on the 11/35, 11/40, and 11/45 and by special order on the other PDP-11 processors), programmer's or operator's console, and peripheral devices. Addresses of the top 4K from the 32K memory words of the basic system are reserved to address I/O device registers.

Minimum system configurations for each of the models are as follows:

- 11/04 — KD11-D CPU, 4K- or 8K-word MOS memory, operator's console, ASCII device control logic, power supply, bootstrap, ROM diagnostics, DMA, 4-level interrupt, 5-1/4-inch chassis with 14 or 9 slots.
- 11/05, and 11/E05 — KD11-B CPU, 4K- or 8K-word core memory, programmer's console, Teletype control, power fail/auto restart, power supply, line frequency clock, 4-level interrupt system; standard core (900-nanosecond cycle time); Model 11E05 uses 16K-word core board (980-nanosecond cycle time).
- 11/10 — KD11-B CPU, memory, console, power supply, real-time clock, terminal interface and 5-1/2-inch assembly for basic configuration: the same features with 16K-word memory, 10.5-inch assembly, DECwriter, RK11D disc, TA11 cassette and bootstrap loader for larger configurations.
- 11/35 and 11/35F — KD11-A CPU with 4-level interrupt and 32K-word memory, memory management unit, console, 21-inch chassis, power fail/auto restart, power, OEM diagnostics; prewired slots for clock, extended arithmetic, floating point, prog. stack; 11/35F is like 11/35 but with 32K words of 980-nanosecond-core modules.
- 11/40 — KD11-A CPU with 4-level interrupt and 8K- or 16K-word memory and console terminal; submodels differ depending on whether memory is 8K or 16K words, whether parity is included, and whether the console terminal is a Teletype, LA30 DECwriter, or VT05 display.
- 11/45 — KB11-A CPU with 4-level interrupt, 16K- or 32K-word core memory, console terminal; submodels differ depending on whether memory is 16K or 32K words, whether parity is included, and whether terminal is Teletype or LA30 DECwriter; DECwriter version includes clock and bootstrap.
- 11/50 — KB11-A CPU with 16K-word MOS memory and 16K-word core memory, both with parity, memory management, LA30 DECwriter, clock, and bootstrap.

All processors support all of the devices provided for the PDP-11 line, as listed in Table 3. The 11/04 includes a four-slot or nine-slot, 5-1/4-inch chassis. The 11/05 and 11/10 include either a 5-1/4 inch or a 10-1/2-inch chassis. Larger models use only the larger chassis. The 10-1/2-inch chassis has 20 slots, which can be expanded to 40 slots within the chassis. All PDP-11 systems can also attach one or two external 20-slot bus extensions. The 11/04 is designed as a MOS memory system, but core can be added to the system provided it is located in an external extension chassis.

Models 11/10 and below can expand memory to 28K words. The 11/35, 11/40, 11/45, and 11/50 have memory management options allowing memory up to 124K words to be addressed.

The 11/35 and 11/40 processors can support two processor modes with the memory management option and a floating-point arithmetic option, in addition to all the features of the 11/20. The memory management option, which is in most respects similar to the memory management option on the 11/45 and 11/50, allows addressing 124K words of core and provides for programmed memory protection.

PDP-11/45 and 11/50 use a processor that has all the features of the 11/40 plus three processing modes, more internal registers, an internal bus to semiconductor memory, and options for memory management and floating-point arithmetic. They are dual-bus systems. An internal

Table 3. Digital PDP-11: Peripherals

Model No.	Description
Discs	
RC11/RS64	Fixed-head discs — 64K wds/drive, 8 drives/controller
RF11/RS11	Fixed-head discs — 256K wds/drive; 8 drives/controller
RJ03/RJ04, RS03/RS04	Fixed-head discs — 256K/512K wds/drive; 8 drives/controller
RK11/RK05	Moving-head discs — 1.2M wds/pack; 8 drives/controller
RP11/RP03	Moving-head discs — 20M wds/pack; 8 drives/controller
RJP04	Moving-head discs — 3330-type, 44M wds/pack, 8 drives/subsystem
Magnetic Tape	
TC11/TU56	DECtape — 288K char/reel; 4 drives/controller
TM11/TU10	7 or 9-trk magnetic tape—45 ips; 8 drives/controller
TA11	Dual cassette transport and controller
TJU16	9-trk magnetic tape system — 800 bpi only or mixed 800 NRZI/1,600 PE, 8 drives/controller
Card	
CM11	Mark sense reader — 40 col, 200 cpm
CR11/CD11	Punched cards — 80 col, 300/1,000 or 1,200 cpm respectively
Paper Tape	
PC11	Reader/punch — 300 cps read, 50 cps punch
PR11	Reader — 300 cps
Printers	
LP11	Line printer series — 170 to 1,200 lpm, 80 to 132 cols, 64 or 96 char
LS11	Line printer — 60 lpm, 132 cols, 64 char
LV11	Electrostatic printer/plotter — 500 lpm, 120,000 dots/sec
CRT	
VT01/TR01	Tektronix 611/RM503, respectively
VR14	Point plot display — 7 x 9 inches
VT05	CRT displays — 1440 char (20 lines, 72 char/line)
Graphics	
GT40	PDP-11/10-based subsystem — 17-inch CRT, light pen
GT42	PDP-11/40-based subsystem — 17-inch CRT, light pen, disc
EG11	Engineering display subsystem — dot display, 71 x 43 A/N characters, controller
Teletypewriters	
Teletypes	LT33 & LT35 ASR and KSR units — 10 cps
LA30	DECwriter — 30 cps, local/remote
Communications	
DC11	Digital I/O subsystem — 50 to 1,800 baud units
DL11	Full-duplex single serial line interfaces — to 2,400 baud
DJ11	16-line multiplexor
DH11	Programmable asynchronous 16-line multiplexor
DP11	Synchronous line module set — full/half duplex models up to 40K baud
DU11	Synchronous interface — full/half duplex, 9600 baud
DQ11	Synchronous interface — full/half duplex, models up to 1.0M baud
DF11	TTL to 20 mA local TTY, or EIA/CCITT voltage
DN11	System unit for 4 Bell 801 ACUs
DC08	Telegraph line interface — up to 32 lines
Process I/O	
LPS	Laboratory peripheral system — for up to 48 channels of A/D and 8 channels of D/A
AD01	A/D conversion subsystem — up to 32 channels
AA11	D/A conversion subsystem — up to 4 channels

bus connects the central processor to semiconductor (MOS or bipolar) memory modules, and the UNIBUS connects the processor, core memory, and all other system units. All semiconductor memory modules have two ports of entry; thus, two processors can share semiconductor memory modules. A PDP-11/45 or 11/50 system can use a mixture of MOS, bipolar, and core memory up to the maximum total memory capacity of 126,976 words.

The 11/45 and 11/50 processors can support two solid-state memory controllers. Each controller can support only one type of memory: up to four 4K-word MOS modules or four 1K-word bipolar memory modules. Thus, a system can have a maximum of 32K words of MOS memory and 8K words of bipolar memory, or 16K words of MOS and 4K words of bipolar memory. The basic 11/45 configuration uses all core memory, while the 11/50 uses either all MOS or a mixture of MOS and core. Either model can be expanded to include both types as well as bipolar memory modules.

Memory for all PDP-11 models can be read/write or read only. Modules are available in increments of 1K (bipolar), 4K (MOS), 8K or 16K (core) words, with only core common to all models. All present core memory modules have a single port of entry while semiconductor modules for the 11/45 and 11/50 can have two ports. Although any PDP-11 system can support core memory modules with any cycle rate, the memory cycle rate considered standard for the different systems is 900 nanoseconds for 8K-word modules and 980 nanoseconds for 16K-word modules. Parity is optional on all models.

Software packages may require considerably more than the basic configurations. Table 4 lists configuration requirements for the major software packages.

In addition to general configurations, Digital offers hardware/software packages for special applications,

which provide savings over using systems configured from a components shopping list. Packages are offered for GT40 and GT42 graphics subsystems, laboratory systems, industrial systems, and communications systems.

Compatibility

PDP-11 computers are upward compatible, from the PDP-11/04 through the 11/10, 11/20, 11/40, to the 11/45 and 11/50, and their OEM equivalents. All can use the same peripheral devices and core memory modules, as well as the same instruction and data formats. All use the same basic instruction set; the 11/35, 11/40, 11/45, and the 11/50 use supersets of the basic instruction set.

PDP-11 is not compatible with any other computer system.

MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks outside the large computer companies, both in the United States and worldwide. More than 1,500 engineers man its service staff.

Aside from 46 sales and service locations in the United States, Digital has offices in five Canadian cities, six Australian cities, five German cities, six U.K. cities, three Brazilian cities, and one or two cities each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, the Netherlands, New Zealand, Norway, Philippines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicomputer manufacturers have traditionally aimed at somewhat "self-sufficient" users and have thus provided considerably less software support and applications programming assistance than the large systems makers, this picture is changing, as evidenced by Digital's recently added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour periods. An on-site engineer can also be hired if requirements are critical; on the other hand, a user can buy service on an individual call basis, or set up his own maintenance staff.

HEADQUARTERS

Digital Equipment Corporation
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Table 4. Digital PDP-11: Software

Package	Description
DOS	Disc operating system; batch package adds job stream processing; requires 8K-wd memory, TTY, disc, DECtape or high-speed paper tape device
RSTS	Time-sharing for up to 16 (RSTS-11) or 32 (RSTS-E) terminals; RSTS-11 requires 20K-wd memory, 256K-wd disc, 2 DECtapes, clock, terminal interfaces; RSTS-E requires 40K-wd memory with parity, larger disc
RT-11	Single user interactive real-time system for program development in scientific or research environment; requires 8K-wd memory, console terminal, and either dual DECtape or disc plus paper tape or cassette
MUMPS-11	Interpretive data management software system geared to interactive I/O; requires 8K-wd memory on any PDP-11, disc, tape, and console terminal
CAPS-11	Cassette programming system for 4K-wd memory, dual cassette drives, and console terminal
RSX-11	Real-time multiprogramming executive in 5 versions, 2 actively marketed; running from 8K-wd core-based or disc-based version with assembly language support, to full-blown disc-based foreground/background multiprogramming system supporting on-line FORTRAN and COBOL. Configurations vary widely; largest systems require memory management option
COMTEX-11	Modular reentrant package for servicing communications devices; SCIP monitor, and TAP table-oriented, terminal routines
BASIC	Extension of Dartmouth BASIC, language of RSTS and RT-11, also stand-alone version (desk calculator)
FOCAL	Interpreter for small systems in either stand-alone or DOS versions
FORTRAN IV	ANSI standard, batch versions for DOS or on-line version for RSX-11
COBOL	ANSI x • 3.23-1974, standard plus extensions; requires PDP-11/30 or larger system with 48K wds of memory, printer, card reader, keyboard/display, and RSX-11 (M or D)
Assemblers	Absolute and relocatable PAL-11, stand-alone and DOS, RSTS-11, COMTEX-11, RSX-11 versions
Utilities	Editor, debugger, linker, librarian, loader and so on.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	LABORATORY AND SCIENTIFIC SYSTEMS		
PDP-11E10-NE/NF*	Disc Operating System with PDP-11/10	24,000	285
DECLAB 11/10-A	LAB System with ASR-33 terminal	11,495	131
DECLAB 11/10-B	Lab System with DECwriter and 10-bit A/D	15,585	159
DECLAB 11/10-C	LAB System with DECwriter and 12-bit A/D	18,385	191
DECLAB 11/10-D	LAB System with DECwriter; uses Foreground/Background Operating System	26,750	265
DECLAB 11/10E	LAB System with 1.2M-wd disc cartridge drive and control	29,550	297
DECLAB 11/40-AA/AB*	Laboratory Computer System with PDP-11/40 CPU	37,500	494
RSX-11D System #1	Real-Time System Executive System with PDP-11/50	111,100	886
RSX-11D System #2	Real-Time Executive System with PDP-11/40	52,525	444
RSX-11D System #3	Same as System #2 except for RK05 disc cartridge drive instead of TM11 magtape unit	46,880	407
RT-11 System #4	Real-Time system with PDP-11/50	57,505	557
RT-11 System #5	Real-Time System (same as system #4 except for RK05-AA/BB* disc cartridge drive instead of TM11 magtape)	51,860	520
RT-11 System #6	Real-Time System with PDP-11/45	49,505	401
RT-11 System #7	Real-Time System (same as System #6 except RK05-AA/BB* disc cartridge drive instead of TM11 magtape)	43,860	364
RT-11 System #8	Real-Time System with PDP-11/40 Recommended software: RT-11 monitor and system programs, Dartmouth BASIC, and ANSI Std FORTRAN IV	38,945	345
RT-11 System #9	Real-Time System (same as System #9 except BM792-YB disc/DECtape bootstrap loader and RK05AA/BB disc cartridge drive instead of TM11 magtape) DOS/BATCH Operating System and ANSI Std FORTRAN IV	33,050	306
DOS/BATCH System #4	DOS/Batch System with PDP-11/50	57,505	557
DOS/BATCH System #5	DOS/Batch System (same as System #4 except RK05-AA/BB* disc cartridge drive)	51,860	520
DOS/BATCH System #6	DOS/Batch System (same as System #4 except with 11/45-CU/CV*CPU)	49,505	401
DOS/BATCH System #7	DOS/Batch System (same as System #6 except RK05-AA/BB* disc cartridge drive)	43,860	364
DOS/BATCH System #8	DOS/Batch (same as RT-11 System #8 but with recommended software: DOS/BATCH operating system and ANSI Std FORTRAN IV)	38,945	345
DOS/BATCH System #9	DOS/Batch System (same as RT-11 System #9 but with recommended software: DOS/BATCH operating system and ANSI Std FORTRAN IV)	330,050	306
CAPS-11 System #10	CASSETTE Programming System with PDP-11/10	12,335	147
CAPS-11 System #11	Cassette Programming System with PDP-11/40 Recommended software: Dartmouth BASIC/PTS	19,200	185
MUMPS-11 System #12	MUMPS-11 Software Package, with 11/45	80,195	580
MUMPS-11 System #13	MUMPS-11 Software Package with 11/40	45,145	386
PHA-11 System #14	Pulse Height Analysis System with PDP-11/40	52,920	456
PHA-11 System #15	Pulse Height Analysis System on PDP-11E10	32,500	330
GAMMA-11 BM11-HA/HB*	Nuclear Medicine System on PDP-11/40	56,500	442
11/45-RP/RR*	RSTS/E Timesharing Systems on PDP-11/45; with dual DECtape and cartridge disc storage; expandable	83,670	485
11/45-RS/RT*	Same as 11/45 RP/RR except industry std 9-track magnetic tape instead of DECtape unit	85,715	538
11/45 RU/RV*	Same as 11/45 RS/RT except with floating-point processor and 20M-wd disc pack unit	97,485	635
RSX-11D	Real-Time Operating System on PDP-11/45	64,315	433
11/45-NA/NB*			
11/45-NC/ND	Same as 11/45-NA/NB* except with additional 16K parity core memory and H960-D extension mounting cabinet with PDP-11/45 and simultaneous background batch processing	73,015	473
11/45-NE/NF		122,040	743
11/45-NH/NJ	Same as 11/45 NH/NJ except with RK05 DECpack disc drive and no mag tape unit	67,370	438
11/45-PS/PT	Batch Processing System on PDP-11/45	51,205	378
11/45 PU/PV	Same as 11/45 PS/PT except with RF11-A 262K fixed-head disc unit and TC11 DECtape unit instead of RK11-D DECpack disc unit and TM11-E mag tape unit	52,560	290
11/50-NA/NB	Batch Processing System on PDP-11/50	73,015	580
11/50-NC/ND	Same as 11/50-NA/NB* except additional 16K parity core memory	78,615	605
11/50-NE/NF*	High-Performance PDP-11/50-Based Real-Time System with simultaneous background batch processing	153,500	990
11/50 NH/NJ*	Same as 11/50 NC/ND* except 1.2M-word DECpack instead of mag tape unit	72,970	570
11/50-PS/PT*	Batch Processing System on PDP-11/50	59,205	525
11/50-PU/PV	Same as 11/50 PS/PT except RF11-A 262K fixed-head disc unit and TC11-G DECtape unit instead of RK11-D DECpack disc unit and TM11-E mag tape unit	60,560	437
11/50-PW/PY	Batch Processing System on PDP-11/50 with high-speed card reader and line printer, floating-point hardware, industry std mag tape and 20M-word disc pack storage	137,980	1,004
11/50 RP/RR	48K 11/50-Based Timesharing System on PDP-11/50 with dual DECtape and cartridge disc storage; expandable to 32 simultaneous users	92,370	632
11/50-RS/RT	Same as 11/50 RP/RR except TM11-E mag tape unit instead of TC11-G DECtape unit	94,415	685
11/50-RU/RV	Timesharing System on PDP-11/50 with 20 M wd disc pack storage, hardware floating-point processing, industry std mag tape expandable to 32 users	106,185	782
	CENTRAL PROCESSOR AND WORKING STORAGE		
PDP-11/04	Computer System with processor, operator's console and bootstrap loader	2,475	NA
PDP-11/05	Computer System (OEM only) with KD11-B Central Processor		
KA/KB*	4K Core (space for 8K core and 4 peripheral controllers)	4,395	53
LA/LB*	Same as KA except 8K core (space for 4 peripheral controllers)	4,995	69
NC/ND*	8K Core (mounted in 10.5-inch box)	5,995	69
SC/SD*	16K Core	7,495	NA
PDP-11/05-SC/SD*	16K Core; 28K Chassis	7,495	74
	Processor Options		
MM11-K	4K Wd of 16-Bit Read/Write Core Memory (900-nsec cycle time)	2,700	20
PDP-11E05 NE/NF*	Computer System (OEM only) with KD11-B Central Processor and 16K core	24,000	269
PDP-11/10 AC/AD*	Computer System with KD11-B Central Processor and 8K core	6,995	69
KE11-A	Extended Arithmetic Hardware Element (multiply/divide; multiple shifts; normalize)	1,940	10
KG11-A	Communications Arithmetic Element	810	6
PDP-11/10 NC, ND	Same as 11/10-AC, D except in 10½-inch assembly	7,495	69
PDP-11/10 NE, NF	Basic PDP-11/10 with 16K core	24,000	285
11/10-SC/SD*	PDP-11/10 Computer in 10.5-Inch Assembly with 16K-word core memory, real-time clock, and console terminal control (for serial devices)	7,495	74
KG11-A	Communications Arithmetic Element (for calculation of cycle and longitudinal redundancy checks; calculation and test of block check char; required for sync communications)	900	6
PDP-11/35 FL/FM*	Computer System (OEM only) with KD11-A Central Processor and 32K Core	20,495	147
11/35-SC/SD*	Same as 11/35-FL/FM* except 16K MF11-U memory and 40K chassis	11,495	111
11/35-JE/JF*	Same as 11/35-FL/FM* except 8K ME11-L memory and 56K chassis	9,995	100
11/35-JC/JD*	Same as 11/35-FL/FM* except 8K MM11-S memory and 32K chassis	9,495	101
11/35-JA/JB*	Same as 11/35-FL/FM* except 8K MF11-L memory and 32K chassis	9,495	100
PSP-11/40 CA/CB*	Computer System with KD11-A Central Processor and 8K Core	12,995	143
PDP-11/40 BA/BB*	Same as 11/40-CA except 16K wds of core memory	15,500	138
PDP-11/40 BC/BD*	Same as 11/40-BA/BB except with Serial LA30 DECwriter and control instead of Teletype	16,250	133
PDP-11/40 BE/BF*	Same as 11/40-BC/BD except with VT05 display terminal and control instead of the LA30	16,250	124
PDP-11/40 BH/BJ*	Same as 11/40-BA/BB except core memory has parity	16,900	133
PDP-11/40 BK/BL*	Same as PDP-11/40-BC/BD except core memory has parity	17,650	127
PDP-11/40 BM/BN*	Same as PDP-11/40-BE/BF except core memory has parity	17,650	119
	Options for KD11-A Processor		
KE11-E	Signed Integer Multiply and Divide; extended instruction set (EIS) option	1,400	11
KE11-F	Floating-Point Processor (4 instructions: multiply, divide, subtract, add; requires KE11-E)	1,500	11
KJ11-A	Stack Limit Option (permits a soft stack limit violation)	400	5
KT11-D	Memory Management Option (permits access to 124K wds; includes KJ11-A)	2,480	21
PDP-11/45 BA/BB*	Computer System KB11-A Processor with 16K-wd core memory, ASR33 TTY terminal, and control cabinet	26,660	196
PDP-11/45-BH/BJ*	Same as 11/45 BA/BB except core memory has parity	27,670	191
PDP-11/45-CU/CV*	KB11-A Processor with 16K-wd parity core memory, serial LA30 DECwriter, and control	27,760	194
PDP-11/45 CW/CY*	Same as 11/45-CU/CV except with 32K-wd parity core memory	37,570	252

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
PDP-11/45-FK/FL	KB11-A Processor with 16K core memory, no parity (OEM)	23,900	191
PDP-11/45-FH/FJ	KB11-A Processor with 16K core memory, and parity (OEM)	25,300	186
PDP-11/45-FU/FV	KB11-A Processor with 32K core memory, no parity (OEM)	32,600	254
PDP-11/45-FS/FT	KB11-A Processor with 32K core memory and parity	35,100	244
PDP-11/50 CU/CV*	Same as 11/45-CU/CV except has 16K-wd MOS memory with parity	35,670	350
PDP-11/50 CW/CY*	KB11-A Processor with 16K MOS and 16K core	46,270	408
PDP 11/50-FK/FL	KB11-A Processor with 16K MOS memory, no parity (OEM)	32,000	341
PDP 11/50-FH/FS	KB11-A Processor with 16K MOS memory and parity (OEM)	33,000	341
PDP 11/50-FU/FV	KB11-A Processor with 16K MOS, 16 core, no parity (OEM)	39,900	405
PDP 11/50-FS/FT	KB11-A Processor with 16K MOS, 16 core, and parity (OEM)	42,500	400
	Options for KB11-A Processor		
FP11-B	Floating-Point Processor (operates on 32- and 64-bit nos.; integer to floating conversion)	5,290	45
KT11-C	Memory Management Unit	4,210	32
	Options for Any PDP-11 Processor		
KG11-A	Communications Arithmetic Element	900	6
KE11-A	Extended Arithmetic Hardware Element	1,940	11
	Memory for All PDP-11 Processors		
ME11LA/LB*	Memory System (16-bit read/write; 900-nsec core; rack mountable; power supply; first 8K increment)	5,200	37
MF11-L	8K Words of 16-bit Read/Write Core Memory (900-nsec cycle time; expandable to 24K in 8K or 12K increments)	4,700	37
MM11-L	8K-Word Expander for ME11-LA or MF11-LB	4,400	37
MM11-LK	12K Word Expander for MF11-L or ME11-L	7,100	58
MM11-S	8K-Word Core Memory and Control (900-nsec cycle time)	4,700	38
MF11-U	16K-Word Core Memory and Control with Expansion Capability to 32K (980-nsec cycle time)	4,900	32
MM11-U	16K-Word Expander Core Memory (980-nsec cycle time; MF11-U reqd)	4,500	32
MF11-UP	16K-Word Parity Core memory and Control with Expansion Capability to 32K (980-nsec cycle time)	6,300	27
MM11-UP	16K-Word Parity Core Memory Expander (980-nsec cycle time; MF11-UP reqd)	5,600	27
FM11-U	Conversion Kit (to add 16K memory capability)	1,000	–
	Memory for 11/40 and 11/45		
MF11-LP	8K-Word Parity Core Memory	5,700	32
MM11-LP	8K-Word Expander Parity Core Memory	5,400	32
	Semiconductor Memory for 11/45 and 11/50		
MS11-CC	Bipolar Memory Control	1,950	13
BC	First MOS Memory Control	1,950	13
BD	Second MOS Memory Control	1,500	13
MS11-CM	1K-Word Bipolar Memory (300-nsec cycle time)	1,950	16
CP	1K-Word Bipolar Memory (byte parity; 300-nsec cycle time)	2,500	16
BR	4K-Word MOS Memory (495-nsec cycle time)	3,000	42
BT	4-K-Word MOS Memory (byte parity; 495-nsec time)	3,400	42
	Graphic Systems		
GT40AA/AB*	Computer-based PDP-11/10 Graphic Terminal System	14,500	186
GT40AC/AD*	Same as GT40-AA/AB but ASR33 replaces keyboard	15,720	223
GT40AE/AF*	Same as GT40-AA/AB but LA30 DECwriter replaces keyboard	16,795	217
GT42AA/AB*	Computer-Based Graphic Terminal System	17,500	151
GT42 AC/AD*	Same as GT42-AA/AB but ASR33 replaces keyboard	18,720	181
GT44 AE/AF*	Same as GT42-AA/AB but LA30 DECwriter replaces keyboard	19,795	176
GT42 AA/AB*	Graphic Display Standard System	34,500	424
BM873-YA	Restart/Loader	400	1
MR11-DB	64-Word Bulk Storage Bootstrap Loader	700	5
	MASS STORAGE		
	Fixed-Head Discs		
RC11-A/B*	64K-Word Fixed-Head Disc Drive and Controller (for up to RS64 drives)	8,300	37
RS64-A/B*	64K-Word DECdisc Fixed-Head Drive (16 μsec/word transfer rate; 17-msec avg access time)	5,500	16
RF11 AA/BB*	256K-Word Disc Drive and Controller (for up to 8 RS11 discs; includes cabinet)	16,650	69
RS11/RS11-A*	256K-Word Fixed-Head Disc Drive (16 μsec/word transfer rate; 17-msec avg access time)	10,700	40
RJS03 BA/BD*	256K-Word Disc Drive and Controller (for up to 8 RS03 or RS04 drives; 4 or 8 μsec transfer rate; 8.5-msec avg access time; includes cabinet with space for 2 additional drives)	14,000	75
RJS04 BA/BD*	512K-Word Disc Drive and Controller (expands up to 8 RS03 or RS04 drives; includes cabinet with space for up to 2 additional drives)	18,000	85
RS03 AA/AD*	256K-Word Disc Drive (4 or 8 μsec/word transfer rate, 8.5-msec avg access time)	9,000	48
RS04	512K-Word Disc Drive (4 μsec/word transfer rate, 8.5-msec avg access time)	13,000	58
	Removable Discs		
RK11-DE/DJ*	1.2M-Word Disc Cartridge Drive (expandable to 8 RK05 DECpack disc drives; cabinet includes space for 3 additional RK05s)	11,000	106
RK05-AA/BB*	1.2M-Word DECpack Moving-Head Disc Cartridge drive (11.08 μsec/word transfer rate; 70-msec avg seek time)	5,100	64
RK05K-11	Cartridge for RK05	99	–
RP11 CE/CJ*	20-Word Disc Pack Drive and Controller (expandable to 8 RP03s)	31,880	233
RP03 AS/BB*	20M-Word Moving-Head Disc Drive (7.5 μsec/word transfer rate; 29-msec avg access time)	20,000	159
RP02-P	Disc pack for RP03 (20M wds)	295	–
	INPUT/OUTPUT		
KW11-L	Real-Time Clock (line frequency; causes interrupt every 16.6 msec [60 Hz] or 20 msec [50 Hz])	300	3
KW11-P	Programmable Real-Time Clock	700	6
LT33 DC/DD*	Teletype ASR 33 (with paper tape reader/punch; 10 cps)	1,850	37
CC/CD	Teletype KSR 33	1,400	32
LT35 DC/DD*	Teletype ASR 35 (with paper tape reader/punch; 10 cps)	4,860	32
CC/DD*	Teletype KSR 35	3,240	29
LC11-A	Controller for Data Terminal LA30-P	500	6
LA30 PA/PD*	DECwriter Data Terminal	2,795	32
CA/CD*	Same as LA30-PA except serial 20 ma current loop; switch selectable 110, 150, or 300 baud	3,195	32
EA/ED*	Serial DECwriter Word Copy Terminal	3,195	30
PC11,-A*	High-Speed Paper Tape Reader (300 cps) and Punch (50 cps) with Control	3,900	38
PR11	High-Speed Paper Tape Reader (300 cps) with Control	2,400	22
H-722	Transformer (required for 230 V operation of PC11, PR11)	100	–
CM11/CM11-A*	Mark-Sense Card Reader (40 col; 200 cpm)	5,290	50
CR11/CR11-A*	Card Reader (80 col; 300 cpm; tabletop model)	4,860	53
CD11-B/CD11-A*	Same as CR11 except 1,000 cpm; with DMA interface	10,800	74
CD11-EA/EB*	Card Reader (80 col; 1,200 cpm)	15,120	95
CM11-FA/FB*	Mark Sense and Punched Card Reader (285 cpm; includes control unit)	5,290	53
LP11	Line Printer (300 lpm; includes control logic)		
FA/FB*	(80-col, 64 char; 350 lpm)	12,000	60
HA/HB*	(80-col, 96 char; 250 lpm)	13,500	65
JA/JB*	(132-col, 64 char; 240 lpm)	17,500	75
KA/KB*	(132-col, 96 char; 170 lpm)	19,000	80
RA/RB*	Same as LP11-JA except 1,200 lpm; heavy duty	30,000	154
SA/SB*	Same as LP11-KA except 900 lpm; heavy duty	33,000	154
VA/VD*	132-Col, 64-Char Printer and Control Unit (300 lpm)	9,900	72
WA/WD*	132-Col, 96-Char Printer and Control Unit (230 lpm)	11,900	72
LS11-A,B*	132 Col, 64-Char (60 lpm)	5,615	48
LV11-BA/BB	Electrostatic Printer/Plotter and Controller; 132-col, 96 char; 500 lpm, 120,000 dots/sec	11,770	50
TC11-GA/GB*	DECtape Transport and Controller (for up to 4 TU56 transports; includes cabinet; 288K char/reel)	9,500	45
TU56	Dual DECtape Transport (288K char/reel)	5,100	32
TU10	Industry-Compatible Tape (½-in. tape; 800 bpi; 45 ips; 7-channel model has provision for program-selectable 556 and 200 bpi; up to 7 slave units can be added to each master and control; cabinet included)		
TM11-EA/ED*	9-Track Master (1st unit)	10,745	101
TU10-EE/EJ*	9-Track Slave	7,505	74
TM11-FA/FD*	7-Track Master (1st unit)	12,500	101
TU10-FE/FJ*	7-Track Slave	7,505	74
TA11-AA/BB*	Dual Cassette Transport and Controller	2,990	38
TU60-K	Cassette (150 ft.; 90,000 char)	7	
AA11-A	Control for VT01-A Scope (requires AA11-D and 2 BA614s)	645	2
B	Control for Scope (requires AA11-D and 2 BA614s)	645	2
C	Control for VR14 Scope (requires AA11-D and 2 BA614s)	645	2
VT01-A	Tektronix 611 Storage Tube Display	3,240	80
VR01-A	Tektronix RM503 Oscilloscope Display	1,080	15
VR14/VR14-A*	Point Plot Display (7 x 9 in.)	3,240	19
VT05B-AA/AD*	CRT Display (A/N; with keyboard; half/full-duplex; 64/96-char set; 20 lines, 72 char/line; TTY compatible; 110, 150 or 300 baud; requires DC11; no parity)	2,795	23
BA/BD*			
VT05B-CA/CB*	CRT Display (A/N; parity; 64/96-char keyboard; DF01-A or Bell 103 equivalent reqd; BC05-D cable reqd)	2,795	23
DA/DB*			
VT11-AA/AB*	Display Processor with 17-In. CRT and Light Pen	9,500	250
	DATA COMMUNICATIONS		
DC11-AA	Dual Asynchronous Serial Line System Unit and Clock (for mounting 2 DC11-DA modules; 110, 134.5, 150, or 300 bps; typical 103 modem speeds program selectable)	350	3
DC11-DA	Full Duplex Serial Module Set for DC11A (5-, 6-, 7-, or 8-bit codes; EIA/CCITT termination for direct use with 103 or 202 modem)	700	7
H312A	Asynchronous Null Modem (allows direct connection of peripherals with EIA 232 interface with a DC11)	85	2
DL-11A	Full Duplex Single Serial Line Interface (replaces KL11; customer specifies speed group 1 [110 baud] or 3 [50, 75, 150, 300, 600, 1,200, 1,800, and 2,400 baud]; for DEC-supplied TTY or VT05)	500	6

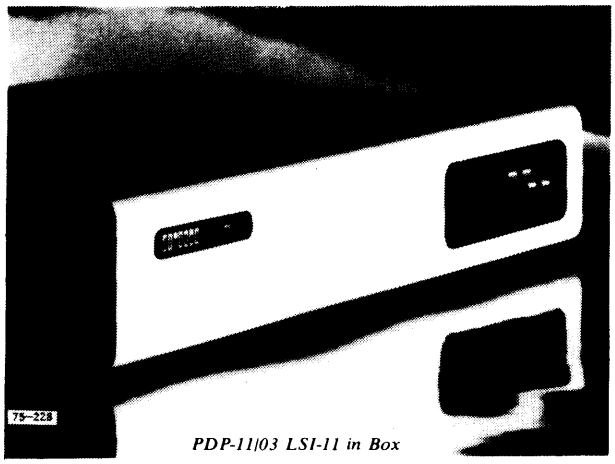
TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
DJ11-AA	Asynchronous 16-Line Multiplexor for EIA/CCITT terminals or lines	3,400	32
DJ11-AB	Asynchronous 16-Line Multiplexor for use with external signal conditioning equipment	3,100	27
DJ11-AC	Asynchronous 16-Line Multiplexor for 20mA level conversion	3,200	32
DH11-AA/AC*	Programmable Asynchronous 16-Line Multiplexor and Mounting Panel with space for up to 4 DM11 line adapters (16 lines)	4,400	32
DH11-AB	Programmable Asynchronous 16-Line Multiplexor with data cable for connection to DC08 telegraph line interface	4,200	29
DM11-BB	Modem Control Multiplexor	1,295	19
DM11-DA	Line Adapter for 4 20mA terminals	170	5
DM11-DB	Line Adapter (4 EIA lines; includes four 25-ft modem cables)	485	5
DM11-DC	Line Conditioning	860	11
DP11-DA	Synchronous Line Module Set and System Unit	1,700	19
CA	Data/Sync Register Extender	400	3
KA	Internal Clock	300	3
DP11-DC	Same as DP11-DA, only suitable with direct use with 303 modems; includes 25-ft cable	2,100	19
DU11-DA	Full/Half-Duplex Synchronous Interface Data set control included	900	5
DQ11-DA	Full/Half-Duplex NPR Synchronous Interface with programmable transmission speeds up to 10,000 baud	2,800	24
DQ11-EA	Full/Half-Duplex Synchronous NPR Interface to Bell System 303 or equivalent modems	4,200	25
DQ11-KA	Crystal Clock Option	150	1
DC08-CS	Telegraph Line Interfaces (not for 11/45) Interface Panel (up to 16 DC08-CM dual-line adapters)	2,160	4
CM	1 Dual Telegraph Terminal and Receive Line Adapter	230	2
EB	Telegraph Line Current Adjustment Panel	2,160	2
D	Distribution Panel	1,080	2
793	Power Supply	540	7
893	Fuse Panel	1,080	–
H316-A,B*	Dual Telegraph Line Interface for 2 common carriers on private telegraph circuits	1,000	3
DR11-B	General-Purpose Direct Memory Access Interface	1,400	13

Notes:
* Starred submodel is 230V, 50/60 Hz version; unstarred submodel is 115V, 50/60 Hz version; some components are also available for 47 to 420 Hz.
(1) DEC does not rent equipment.
(2) Contact Digital in Maynard MA.
(3) Maximum total memory is 124K; system allowed max of 2 solid-state memory controllers. OEM models available for most equipment.
– Not Applicable NC No Charge NA – Not Available

DIGITAL EQUIPMENT CORP.

PDP-11 System Report Update



PDP-11/03 LSI-11 in Box

PDP-11V03

The PDP-11V03 is a disc version of the PDP-11/03 with operating system and high-level languages. It includes dual floppy disc drives, either an LA36 keyboard printer terminal or a VT52 DECscope alphanumeric display terminal, and RT-11 real-time operating system. FORTRAN IV or BASIC can be added to the system for high-level language capabilities.

RT-11 is a disc-based operating system that can be used to develop and execute user programs written in FORTRAN IV, BASIC, or Assembler machine language. RT-11 includes modules for debugging, editing, file maintenance, library access, and utility operations.

The RXV11 floppy disc drive for the system has a total storage capacity of over 500K bytes. Average access time is 483 microseconds, and data transfer rate is 10K bits per second.

In single-unit quantities, the PDP-11V03 system is priced at $9,950. For 100-unit quantities the following prices apply.

Equipment	Price $ (100-unit quantity)
PDP-11/03 with 8K-word RAM	1,997
RXV11 dual floppy disc	2,496
Floppy disc bootstrap	192
LA36 printer	1,392
VT52 CRT	1,277
RT11 operating system	420

Bipolar Parity Memory

Digital now offers a new solid-state memory unit, called MS11-AP, that allows up to 32,768 words of bipolar parity memory to be added to PDP-11/45 or 11/50 minicomputers. Previously, the PDP-11/45 and 11/50 could accommodate a maximum of 8K words of bipolar memory.

The new memory, designed on a 4K-word memory matrix board, can be used where high speeds are essential. Such applications include use in simulation problems and control response situations. Bipolar memory is 40 percent faster than MOS memory. Up to 3 million instructions can be executed per second with the bipolar memory.

In 16K-word units, the memory purchase price is $19,700. First deliveries began in Fall 1975, and delivery can be expected 90 days after Digital receives the order.

DEC DATASYSTEM (DDS) 350 SERIES

Three new low-cost, disc-based PDP-11 timesharing systems operate as a bridge between the earlier PDP-8-based DDS-300 Series and the PDP-11-based DDS-500 Series. The upgrade path from the DDS-300 to the 500 is via DIBOL, previously offered only for the PDP-8, but now supported on the PDP-11-based DDS-350 Series.

The DDS-350 Series consists of three models: DDS-352, 354 and 356. All three support up to four hardcopy or A/N display terminals, which access the same data base. The systems include a PDP-11/10 CPU with 32K characters of core, expandable to 56K characters. Mass storage for the series includes a minimum of two floppy disc drives of 512K characters for the 352, two cartridge disc drives providing 4.8 million characters of storage for the 354 and two disc packs providing more than 40 million characters for the 356. Maximum on-line storage for the DDS-350 series system is 160M bytes. The DDS-352 and 354 are both upwardly compatible with the DDS-356.

Software for the series is Commercial Operating System (COM) 350, featuring independent jobs, intertask communications, line printer spooling, more than 200 text

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error messages, sort utility, selective data file and total disc backup utilities. Digital Business Oriented Language (DIBOL) II is supported by COS 350. An optional communications protocol package emulates the IBM 2780 for telephone transmission of data in a distributed network.

A choice is available of several video or hardcopy terminals, line printers, and magnetic tape in speeds from 800 to 1,600 bpi and an 80-column card reader.

Small companies can use a DDS model for standalone processing. In larger firms, the systems can be used as control computers in a distributed processing network. A Datasystem 352 with central processing unit, two floppy discs, CRT and 30-character-per-second printer can be purchased for approximately $20,000; the 354 with two cartridge disc drives, central processor, two terminals and a 165-character-per-second printer costs about $37,000; and the top-of-the-line Datasystem 356, with two large disc packs, CPU, any combination of four video or hard-copy terminals, and a 300 line-per-minute printer costs between $65,000 and $70,000.

Digital is marketing the new systems through its OEM network. First deliveries began August 1975.

PDP-11T10

A new standard hardware configuration for the PDP-11/10 called the PDP-11T10 has been announced. The configuration includes a PDP-11/10 processor with 16K words of core memory, dual 1.2-million word RKO5 disc pack drives, LA36 30-character-per-second DECwriter, bootstrap loader, cabinet, and mounting hardware. Purchase price for the new package is $22,000, about 15 percent lower than the equivalent configuration would be if the constituent items were purchased separately. An OEM version, called the PDP-11T05, is also available. In 50-unit quantities the OEM version costs $14,520. The new configuration is available immediately from stock.

NEW SOFTWARE PACKAGES

Four new software packages for use with the RT-11 disc operating system add extensive support for PDP-11 laboratory peripherals. The packages provide support for analog to digital, digital I/O, graphics, and plotting systems, including both peripheral devices and interfaces. Two of the new packages have been integrated into the FORTRAN/RT-11 system, while two more are available under separate license.

The following systems are built into the FORTRAN/RT-11 system.

- A systems library package provides the user with utility functions, character-string manipulation and most RT-11 monitor features at the FORTRAN language level. Both foreground/background and single-job monitor functions are performed under RT-11.
- A FORTRAN/RT-11 extensions package gives the FORTRAN programmer complete control of three real-time subsystems and a graphics subsystem.

The following packages are separately licensed.

- A library of subroutines aids in developing programs in FORTRAN IV and plot graphic data on Digital's LV-11 electrostatic printer-plotter. Text can be printed horizontally and vertically. Graphic output control and shading facilities are provided.
- A scientific subroutine package includes 125 FORTRAN IV subroutines in source code. These give the user many mathematical and statistical routines required for scientific programming. Some typical applications for the package are statistical data reduction, scientific calculations and monitoring laboratory instruments.

License costs for the printer/plotter package and the scientific subroutine package are $1,000 and $300, respectively.

PDP-11/03

Digital now has an end-user version of the LSI-11. Called the PDP-11/03, the system boxes the LSI-11 processor and includes a power supply. Both MOS RAM and core memory configurations are available.

The PDP-11/03, with 4K words of MOS RAM memory, a serial interface, power supply, rack mountable enclosure and an operator's front panel, can be purchased for $2,495. The core memory version costs $2,925. Both are available for either 115 or 230 vac power source.

The LSI-11 was introduced in February 1975. The 1,200-nsec processor is designed on one 8.5- by 10-inch board for the MOS version and on two boards for the core version. In quantities of 100, an LSI-11 processor with I/O bus, 4K words of MOS RAM, real-time clock, single level interrupt, and power fail/auto restart, for standalone operation, costs $634. The core version costs $983 in 100-unit quantities.

Options available for the PDP-11/03 include an extended arithmetic chip, serial line interface module, parallel line interface module and four expansion memory modules: 4K-word RAM, 1K-word RAM, 4K-word PROM/ROM, and 4K word core. The unit measures 3½ x 19 x 13½ inches and weighs 35 pounds. First delivery was in September 1975.

NEW FLOPPY DISC

Users of Digital's PDP-11 mini can now add a low-cost floppy disc system called the RX11. The system has a 256K-byte capacity, a 10K-byte-per-second transfer rate and an average access time of 483 milliseconds. RX11 is available in either single- or dual-disc drive configurations. Extensive operating system and diagnostic software support the system.

The diskettes used on the RX11 are industry compatible, formatted in 77 tracks with 26 sectors per track. The system fits into a standard 19-inch rack and can be used as a random access file device or for input-output. Since the head only contacts the disc during reading and writing, disc life is prolonged. The systems are reported to be highly reliable, with a design goal mean time between failure of 5,000 hours.

Purchase price for the RX11 is $2,900 for a single disc drive and $3,900 for a dual-disc configuration. The diskettes cost $40 in five-disc lots and $75 for lots of 10. Delivery of the system can be expected 30 days after Digital receives the order.

POWER DEMAND CONTROL SYSTEM

An energy-conserving real-time minicomputer package has been introduced by Digital Equipment's Industrial Products Group. Called the Power Demand Control System, the new package is based on a PDP-11/10 mini in a standard Industrial 1100 configuration.

The Power Demand Control System is connected to electrical metering equipment to monitor and project actual power consumption. The user establishes energy use priorities, eliminating non-critical electrical loads such as outdoor lighting or water heaters, and controlling lower-priority equipment so that units are not working simultaneously when energy demand is highest. This equalizes electrical load, reduces energy waste, and lowers electricity costs.

The Power Demand Control System software permits the user to assign equipment and priorities to suit individual needs. The software runs under the RSX-11M real-time software executive and allows operating parameters to be modified without reassembling or restarting the program. Standard hardware includes a PDP-11/10 minicomputer with 16K words of core, an industrial process I/O interface subsystem, a typewriter terminal, and cassette storage.

The system can be used effectively in the following typical applications: process manufacturing, factory operations, building complexes, hotels, and shopping centers — all heavy users of electricity.

Purchase price for the new system is under $30,000, and delivery can be expected approximately 60 days after receipt of the order.

INDUSTRIAL 1117-M

Also recently introduced by Digital was the Industrial 1117-M, an industrial real-time mini designed for factory data acquisition. The system, also based on the PDP-11/10, includes 28K words of core memory, dual disc drives, typewriter terminal, and an industrial input/output interfacing subsystem.

The Industrial 1117-M can be used in applications such as refining, materials handling and food processing. With industrial I/O, the system can perform operations that range from simple monitoring to complex closed-loop control. The interface features high noise immunity and has both analog and digital input and output capabilities. More than 3,000 data points can be controlled with the interface.

The new industrial I/O subsystem features an Industrial Control System (ICS) in place of the older UDC (Universal Digital Control) system. The ICS has built-in remote capability; it can be located up to 6,000 feet from the PDP-11.

Software for the system is RSX-11M. The purchase price is $32,000 and deliveries can be expected 45 days after the order is received by Digital.

NEW LOW-END VERSION of RSX-11

The RSX-11S, announced on April 7, 1975, is a new core-based subset of RSX-11M, which is used for program development for RSX-11S systems. A new RSX-11M, Version 2, will be delivered simultaneously with the 11S so programs that run under RSX-11S can be developed using FORTRAN IV, FORTRAN IV PLUS, or MACRO-11. Digital expects at least typical applications for the RSX-11S: process control where the environment is too harsh for a disc or where only a core-based system is needed; laboratory work where a data logger is needed to gather information for off-line processing; and applications where a dedicated satellite processor is required for an RSX-11M-based system.

The minimum configuration required by RSX-11S includes a PDP-11 processor with 8K words of memory, real-time clock, hardware loader, and load device which can be cassette tape, paper tape reader, DECtape unit, or magnetic tape drive. The load device is used to load programs developed on the RSX-11M and transported to the RSX-11S.

The RSX-11S is licensed for $1,200 with full software support and for $600 without software support. Deliveries are scheduled for fall 1975.

DIGITAL EQUIPMENT
PDP-11/70 System Report

OVERVIEW

The PDP-11/70 is Digital Equipment's PDP-11 compatible system designed to compete in the new "midicomputer" marketplace. Many aspects of the 11/70 system architecture resemble that of the 11/45, but the 11/70 has expanded maximum memory capacity and reorganized I/O structure; it incorporates a high-speed cache memory. Digital has added important new software to implement a system with three times the throughput speed of the 11/45; the 11/70 can operate in a multi-user, multi-language, multi-function environment. It solves the throughput problems associated with traffic on the UNIBUS experienced with larger 11/45 configurations. The PDP-11/70 competes with the Data General Eclipse, Interdata 8/32 Megamini, Modcomp IV and Prime 300. All these systems provide real-time interactive capabilities that rival many small scale batch systems in size, speed and scope, at prices drastically lower than those charged by the larger mainframe computer makers.

The PDP-11/70 still uses a 16-bit word, but internal busses are 32 bits wide. A memory management unit and a high-speed cache memory also help achieve high performance. The 32-bit busses are used to transfer data between main memory and cache memory and between main memory and certain high-speed mass memory controllers for moving-head discs, fixed-head discs and magnetic tape drives. This relieves the UNIBUS of traffic for transfers between mass storage device controllers and main memory, although the same discs used on other PDP-11 systems can still be attached to the UNIBUS. Cache memory, a 2,048-byte high-speed bipolar memory that stores a replica of selected portions of main memory, significantly reduces most memory access times. Cache also controls high-speed transfers between memory and the UNIBUS, memory and CPU, and memory and the four high speed controllers, so that all can operate virtually simultaneously. The management unit, a standard 11/70 feature, increases memory addressing to 4M bytes by adding six addressing bits to produce a 22-bit address. Despite the addressing capability, Digital currently limits memory capacity to 2M bytes. Memory mapping on the 11/70 does not increase instruction execution times.

Cache memory increases system throughput because programs tend to access instructions in sequential order or in small loops and to access data sequentially. Cache stores not only the current instruction or data word but also the next 16-bit word in sequence. This provides a look-ahead feature. Data and instructions remain in cache until they are replaced by a more recently accessed word. This provides a look-back feature. Digital's test indicate the "hit" rate for finding an addressed word in cache is between 90 and 95 percent. This high rate is due to the algorithm for storing and saving data, and to the size of the cache. The cache produces an effective memory cycle time of less than 400 nanoseconds per 16-bit word, while the memory cycle time is 1.0 microsecond.

The 32-bit wide busses are used between cache and main memory and between main memory and the special high-speed data channel controllers used on the 11/70. Data transfers between the CPU and cache are over a 16-bit wide bus, and transfers between the high-speed controllers and mass storage devices or other peripherals are also 16 bits wide. The memory management unit and the UNIBUS mapping unit, which are transparent, code and decode addresses so that the correct 16 bits, 18 bits, 22 bits, 32 bits, or 36 bits (4 bytes plus 4 bits of parity) are sent or received by the appropriate portion of the processor.

The PDP-11/70 is completely compatible with the rest of the PDP-11 line. The central processor generates 16-bit addresses, but the UNIBUS carries 18-bit addresses, the same as other PDP-11s. All peripherals available for other

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PDP-11 systems can be attached to the 11/70 UNIBUS, and all programs written for comparable configurations can be run on the 11/70. New high-speed controllers that attach to the 32-bit wide bus are used only on the 11/70.

Table 1 compares the characteristics of the PDP-11 mainframes.

Both the RSTS/E and the RSX-11D operating systems from the 11/45 will run on the 11/70.

The PDP-11/70 RSTS/E (Resources Timesharing System/Extended) supports 63 users employing the extended BASIC Interpreter in the foreground with an ANSI 74 COBOL-11 program in the background. (A special feature called "$COBOL" allows terminals to access the COBOL compiler via BASIC PLUS. Each terminal that accesses COBOL requires 20K words of memory.)

The RSX-11D operating system is for dedicated real-time systems; it supports FORTRAN IV and FORTRAN IV PLUS, an optimizing compiler. In addition, a new multi-user, multi-language, multi-function operating system called the Interactive Application System (IAS) is scheduled for delivery in November 1975. IAS is currently operating at two or three sites. It will handle multi-language timesharing and batch processing concurrently with limited real-time processing. IAS supports FORTRAN IV, FORTRAN IV PLUS, BASIC, COBOL, and MACRO (assembler).

Digital expects to market the PDP-11/70 to all of its usual markets for industrial business, communications, OEM, laboratory, education, computation, and typesetting applications. Digital spokesmen indicated they expect the PDP-11/70 to outsell the PDP-11/45. To date, more than 2,000 PDP-11/45 systems have been sold. Digital

Table 1. Specifications of PDP-11 Computers Compared

Model	PDP-11/04; 11/E05; 11/05; 11/10	PDP-11/15; 11/20; 11/R20	PDP-11/35; 11/35F; 11/40	PDP-11/45; 11/50	PDP-11/70
ARCHITECTURE					
Microprogrammed	Yes	No	Yes	Yes	Yes
G-P Registers	8	8	9	16	
Buses	UNIBUS	UNIBUS	UNIBUS	UNIBUS + semiconductor Memory bus	UNIBUS + high-speed data bus
Automatic Priority Interrupts	Multi-line, multi-level	Single-line, multi-level	Multi-line, multi-level	Multi-line, multi-level + 7 software levels	Multi-line, multi-level + 256 software levels
Stack Size	Fixed	Fixed	Fixed std; variable opt	Variable	Variable
Floating Point	Software	Software	Hardware opt	Hardware opt	Hardware opt
MEMORY					
Types	Core (11/05, (11/10); MOS (11/04)	Core	Core	Core/MOS/bipolar	Core
Capacity (words)					
Min(1)	4,096	4,096	8,192	16,384	28,672
Max(1)	28,672	28,672	126,976	126,976	1M
Increment Sizes (words)	8,192; 16,384	8,192; 16,384	8,192; 16,384	1,024; 4,096; 8,192; 16,384	32,568
MEMORY					
Management Hardware	No	No	Yes, opt	Yes, opt	Yes, std
Memory Protect	No	No	Opt	Opt	Std
Cycle Time (μsec)					
Core	0.90, 0.98	0.90	0.90, 0.98	0.90, 0.98	1.0
MOS	0.725 (11/04 only)	—	—	0.495	—
Bipolar	—	—	—	0.300	(cache) 0.240
INSTRUCTIONS					
Overlapped	No	No	Yes	Yes	Yes
Extended Arithmetic	Opt	Opt	Opt	Std	Std
Std Instruction	Basic	Basic	Basic + XOR, SOB, RTT, MARK, SXT	11/40 set + MUL, DIV, ASH, ASHC, SPL	11/45(+ floating point opt) in several modes
No. (std; opt)	70; 4	70;4	70; 10	83; 50	400; 446

Note:
(1) Excluding 4,096 physical words reserved for UNIBUS mapping.

Equipment is the leading minicomputer manufacturer, with sales and service offices in 46 cities in the United States, and 24 countries outside the United States. The 11/70 undoubtedly will be an important system to watch in the developing "midicomputer" market.

COMPETITIVE POSITION

The PDP-11/70 can be considered from several points of view. It provides upward mobility for current users of PDP-11 systems. It can computerize applications that have not been efficiently computerized before. It can — because of its size and low cost — directly impact batch business systems by offering a timesharing and/or distributed processing alternatives. It can — because it concurrently operates in several modes — be used by manufacturers to combine functions to process control, data entry and business processing that were previously served by several systems.

The PDP-11/70 will fare differently on all these fronts. Unquestionably, sooner or later it will be used to upgrade PDP-11/45 installations. Initial prospects for minicomputertype applications on a large scale include a variety of aeronautics, traffic control and military applications, as well as communications preprocessing and message switching.

Digital, in its initial announcement of the PDP-11/70, introduced the PDP-11/70-based DEC Datasystem 570 with the Commercial Time Sharing System Extended (CTS 500/E) software. This implies that Digital expects the PDP-11/70 to be particularly important as a basis for a mainly business-oriented system, a timesharing type system that would offer an alternative to small- and medium-scale batch processing systems of much higher price. Data General has also developed a commercial system, the C/300, based on their ECLIPSE 200 system. Thus, the PDP-11/70 may find many customers not as an 11/70 proper competing on the mini/midi market, but as a commercial system, with the system's low price offsetting the lack of applications software. The competitive stance of the PDP-11/70 as a commercial system is best examined in the context of AUERBACH business computer reports on the DEC Datasystem line, but it is noted here because of the system's ability to combine timesharing, real-time and batch processing under IAS.

Although the non-commercial market for midicomputers (as distinct from minicomputers) is still undefined and tentative to some extent, the fact that four companies have made new announcements in this area promises an interesting period of new developments. All undoubtedly expect customers to "move up" to bigger systems in process control and communications, and Digital expects multi-language timesharing under IAS to be important in the education market. It will be interesting to see if "midis" turn up new applications that could not have been done by several minis. Data General's ECLIPSE system is nearest to the PDP-11/70 in overall architectural specifications since it is strictly a 16-bit system, with a cache memory to speed processing and memory management to enlarge capacity. ECLIPSE currently can expand memory only to 256K bytes, it does not have internal 32-bit busses and it supports a smaller number of peripheral devices; both hardware and software facilities for communications are particularly well developed, and the price for a 128K-word system is lower for the ECLIPSE than the PDP-11/70. Interdata's 8/32 is a 32-bit system except for I/O facilities, it is the first 32-bit system by a major mini maker, and it is strongly oriented toward communications and real-time I/O, with speeds and I/O capabilities comparable to the PDP-11/70. SYSTEMS Engineering Laboratories, a small manufacturer, has introduced the SEL 32, a 32-bit word system. Both MODCOMP IV and Prime 300 also compete to some extent with PDP-11/70 configuration by virtue of their speed and size. Table 2 compares some of the specifications of these "midi" systems with IBM's 370/158.

With regard to Digital's own product lines, the PDP-11/70 was long overdue. Reports for the past 2 years indicated the traffic over the UNIBUS kept throughput down on configurations with substantial I/O requirements. Competitors consistently claimed to outbenchmark the 11/45 in real-time environments. Digital offered dual-ported solid state memory with a second internal bus to the CPU on the 11/45. The second port could support a second UNIBUS for multiprocessor configurations, but generally it was connected to the system UNIBUS. Solid state memory was restricted to 32K words, thus throughput was increased only for programs executed from solid-state memory.

The PDP-11/70 overlaps the low end of Digital's PDP-10 line, notably the older KA10 processor, which has not been actively marketed for 2 years. Digital recently upgraded the PDP-10 with the KL10 processor, which is several times as powerful as the older KA10. When asked if Digital plans to provide a bridge between the PDP-11 line and the PDP-10 line, a spokesman indicated such a bridge is at least 2 years away. One stumbling block is the PDP-10's 36-bit word, which is difficult to match with the PDP-11's 16-bit word.

With the new Digital Network Architecture (DNA), Digital is providing facilities so users can easily tie all the PDP computer systems together in a network. This is a good move, for Digital's systems span a broad performance range. The PDP-11/70 is a powerful system that can provide extensive data processing as well as communications capability.

Configuration Guide

A minimum PDP-11/70 System consists of a processor, UNIBUS, high-speed data bus with four I/O ports, 2,048-byte cache memory, 128K bytes of core memory, clock bootstrap loader, powerfail detect, disc and console. Standard processor features include 16 registers (12 accumulators, three stack pointers and a program counter), 4-line/8-level interrupt subsystem, memory management

Table 2. Comparison of Midicomputers with General Purpose Computer Systems

	Interdata 8/32 Megamini	Digital PDP-11/70	Data General ECLIPSE 200	SEL 32	IBM 370/158
Word Length (bits)	32	16	16	32	32
Instruction Execution Times (μsec (register to memory)					
Integer Add	1.2	1.8	2.5	1.2	.9
Integer Multiply	3.5	3.9	8.8	4.5	2.0
Integer Divide	5.8	8.3	11.2	5.1	9.9
Floating-Point Add	2.3	8.2	5.5	3.0	2.4
Floating-Point Multiply	3.0	11.2	7.2	4.5	2.3
Floating-Point Divide	5.3	12.2	7.9	8.9	8.9
Hardware I/O	Yes	No	No	No	Yes
Max DMA Rate (bytes/sec)	6M	4M	2M	6M	6.7M
Max Address Capability (bytes)	1M	64K	64K	512K	16M
General-Purpose Registers	8 stacks of 16 each	2 stacks of 8 each	1 stack of 4	1 stack of 4	1 stack of 16
Prices, & (Dollars)					
CPU + 128KB Memory	51,900	54,600(1)	35,500	43,900	NA
+ 256KB Memory	70,900	68,800	57,100	71,700	NA
+ 512KB Memory	107,400	101,800	NA	128,000	1,779,200
+ 1048KB Memory	179,400	163,800	NA	238,400	1,905,700

Note: (1) Digital bundles parity, console, line clock and installation in the system price.

and protection, and parity. Processor options include expansion of memory in 64K-byte increments up to 2M bytes, and a floating point processor with 46 associated instructions added.

The PDP-11/70 is a dual bus system. One bus is actually 36 bits wide; it carries four data bytes plus four parity bits between memory and the high-speed device controllers. The other bus is the 18-bit wide UNIBUS; it carries two bytes plus two parity bits. Like other PDP-11 systems, most peripheral controllers can connect to the UNIBUS in any order and in any combination. Although the UNIBUS map makes memory modules "look like" they connect to the UNIBUS in the same way as a peripheral device, they actually interface to the CPU via a high-speed cache memory. The 36-bit wide high-speed bus has four integral ports for the attachment of controllers for mass storage subsystems. These ports can attach RWP04 moving head disc subsystems. RWS03 and RWS04 fixed-head disc subsystems, and TWU16 magnetic tape subsystems. Transfers to and from these subsystems include byte parity.

The PDP-11/70 is sold in nine different models that vary in the type of mass storage device(s) included and in single or dual processor versions. Model numbers are as follows:

- PDP-11/70-EA single processor, cartridge disc.
- PDP-11/70-FA single processor, disc pack, and magnetic tape.
- PDP-11/70-FE single processor, dual-access disc pack and dual control, and magnetic tape.
- PDP-11/70-FK single processor, dual-access disc pack and dual control — one for 11/70 and one for any PDP-11, and magnetic tape.
- PDP-11/70-GA single processor, cartridge disc, fixed-head disc, and magnetic tape.
- PDP-11/70-HA single processor, disc pack, fixed-head disc, and magnetic tape.
- PDP-11/70-HE single processor, dual-access disc and dual PDP-11/70 controls, fixed-head disc, and magnetic tape.
- PDP-11/70-HK single processor, dual-access disc and dual controls — one for general PDP-11, fixed-head disc, and magnetic tape.
- PDP-11/77-FE dual processor 11/70s with dual-access discs and two control units and two magnetic tape drives.

All models include controllers for the mass storage units. A corresponding series of 230VAC, 50-cycle systems are also available.

The 11/70 UNIBUS is completely compatible with the UNIBUS for all other PDP-11 systems; it can attach any of the PDP-11 peripherals. These are summarized in Table 3.

Software packages, of course, demand different configurations. Memory requirements are usually satisfied by the minimum configuration, but peripheral requirements vary. Table 4 summarizes the major packages and their configuration requirements.

Compatibility

PDP-11 computers are upward compatible, from the PDP-11/04 through the 11/10, 11/20, 11/40, to the 11/45, 11/50 and 11/70, and their OEM equivalents. All can use the same peripheral devices, as well as the same instruc-

Table 3. Digital PDP-11: Peripherals

Model No.	Description
Discs	
RS03/RS04	Fixed-head discs — 256K/512K wds/drive; 8 drives/controller attach to high-speed data channel
RK05	Moving-head cartridge discs — 1.2M wds/pack; 8 drives/controller attach to Unibus
RP04	Moving-head discs — 3330-type, 44M wds/pack, 8 drives/subsystem attach to high-speed data channel
Magnetic Tape	
TC11/TU56	DECtape — 288K char/reel; 4 drives/controller
TM11/TU10	7 or 9-trk magnetic tape — 45 ips; 8 drives/controller
TA11	Dual cassette transport and controller
TJU16	9-trk magnetic tape system — 800 bpi only or mixed 800 NRZI/1,600 PE, 8 drives/controller
TU16	9-trk 1,600 bpi magnetic tape; 8 drives/controller; attaches to high-speed data channel
Card	
CM11	Mark sense reader — 40 col, 200 cpm
CR11/CD11	Punched cards — 80 col, 300/1,000 or 1,200 cpm respectively
Paper Tape	
PC11	Reader/punch — 300 cps read, 50 cps punch
PR11	Reader — 300 cps
Printers	
LP11	Line Printer series — 170 to 1,200 lpm, 80 to 132 cols, 64 or 96 char
LS11	Line printer — 60 lpm, 132 cols, 64 char
LV11	Electrostatic printer/plotter — 500 lpm, 120,000 dots/sec
CRT	
VT01/TR01	Tektronix 611/RM503, respectively
VR14	Point plot display — 7 x 9 in.
VT05	CRT displays — 1,440 char (20 lines, 72 char/line)
Graphics	
GT40	PDP-11/10-based subsystem — 17-in. CRT, light pen
GT42	PDP-11/40-based subsystem — 17-in. CRT, light pen, disc
EG11	Engineering display subsystem — dot display, 71 x 43 A/N chars, controller
Teletypewriters	
Teletypes	LT33 & LT35 ASR and KSR units — 10 cps
LA30	DECwriter — 30 cps, local/remote
Communications	
DC11	Digital I/O subsystem — 50 to 1,800 baud units
DL11	Full-duplex single serial line interfaces — to 2,400 baud
DJ11	16-line mplr
DH11	Programmable async 16-line multiplexor
DP11	Sync line module set — full/half duplex models up to 40K baud
DU11	Sync interface — full/half duplex, 9,600 baud
DQ11	Sync interface — full/half duplex, models up to 1.0M baud
DF11	TTL to 20 mA local TTY, or EIA/CCITT voltage
DN11	System unit for 4 Bell 801 ACUs
DC08	Telegraph line interface — up to 32 lines
Process I/O	
LPS	Laboratory peripheral system — for up to 48 channels of A/D and 8 channels of D/A
AD01	A/D conversion subsystem — up to 32 channels
AA11	D/A conversion subsystem — up to 4 channels

Table 4. Digital PDP-11: Software

Package	Description
RSTS-E	Timesharing for up to 63 terminals, using extended BASIC, runs on any minimum system with terminal; roughly requires 4K words of memory for each terminal implemented; requires 20K words of memory for each terminal that has the $COBOL facility.
RSX-11D	Real-time multiprogramming executive disc-based, uses on-line FORTRAN and COBOL, runs on minimum PDP-11/70 system
IAS	Combines real-time, batch and timesharing in foreground / middleground / background system, with extended BASIC and on-line FORTRAN and COBOL; up to 16 timesharing users, runs on minimum system
BASIC	Extension of Dartmouth BASIC, language of RSTS-E and IAS
FORTRAN IV	ANSI standard, extended, on-line version for RSX-11E and IAS
COBOL	ANSI X 3.23-1974, standard plus extensions
Assemblers	MACRO
Utilities	Editor, debugger, linker, librarian, loader and so on

tion and data formats. All use the same basic instruction set; the 11/35, 11/40, 11/45, 11/50, and the 11/70 use supersets of the basic instruction set.

PDP-11 is not compatible with any other computer system.

MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks outside the large computer companies, both in the United States and worldwide. More than 1,500 engineers man its service staff.

Aside from 46 sales and service locations in the United States, Digital has offices in five Canadian cities, six Australian cities, five German cities, six U.K. cities, three Brazilian cities, and one or two cities each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, the Netherlands, New Zealand, Norway, Philippines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicom-

puter manufacturers have traditionally aimed at somewhat "self-sufficient" users and have thus provided considerably less software support and applications programming assistance than the large systems makers, this picture is changing, as evidenced by Digital's recently added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour periods. An on-site engineer can also be hired if requirements are critical on the other hand, a user can buy service on an individual call basis, or set up his own maintenance staff.

TYPICAL PRICES

Model Number	Description	Purchase Price $
	Processors and Working Storage	
	All PDP-11/70 systems include: 11/70 central processor with memory management; 2K-byte parity bipolar cache memory (1 byte=8 data bits and 1 parity bit); 128K-byte parity core memory (MJ11-A plus MJ11-AE); bootstrap/diagnostic loader (M9301-YC); and line frequency clock (KW11-L); DECwriter II console terminal (LA36-C); terminal control (DL11-A); 2 cabinets for central processor and core memory; prewired space within the CPU chassis for mounted options	
11/70-EA/ ED*	PDP-11/70 with RK11-DE cartridge disc and control; RK05-AA cartridge disc; and BA11-KE expansion mounting chassis	72,650
11/70-FA/ FD*	PDP-11/70 with RWP04-AA disc pack and control and TWU16-EA (ED) magnetic tape and control	105,100
11/70-FE/ FJ*	PDP-11/70 system with RWP04-BA dual access disc pack and two 11/70 control units; TWU16-EA magnetic tape and control	117,100
11/70-FK/ FN*	PDP-11/70 system with RWP04-CA dual access disc pack with 11/70 control and general 11 control; TWU16-EA magnetic tape control	117,100
11/70-GA/ GD*	PDP-11/70 system with RK11-DE cartridge disc and control; RK05-AA cartridge disc; RWS04-BA fixed-head disc and control; TWU16-EA magnetic tape and control and BA11-KE expansion mounting chassis	109,350
11/70-HA/ HD*	PDP-11/70 with RWP04-AA disc pack and control; RWS04-BA fixed-head disc and control and TWU16-EA magnetic tape and control	126,300
11/70-HE/ HJ*	PDP-11/70 with RWP04-BA dual access disc pack and two 11/70 control units; RWS04-BA fixed-head disc and control; TWU16-EA magnetic tape and control	138,300
11/70-HK/ HN*	Same as 11/70 HE/HJ with general 11 control	138,300
11/77-FE/ FJ*	Dual processor PDP-11/70 with 2 TWU16-EA magnetic tape and control; RWP04-BA dual access disc pack; and 2 control units	187,200
FP11-B	Floating Point Processor	5,600
	Memory	
MJ11-AC/ AD*	256K byte parity core memory	33,000
MJ11-AG/ AH*	256L byte parity core memory expansion frame	31,000
MJ11-AA/ AB*	64K byte parity core memory unit	13,500
MJ11-AE	64K byte parity expander core memory	7,100
	Mass Storage	
	Discs	
RWP04-AA/ AB*	88 million byte disc pack drive and control unit	35,000
RWP04-BA/ BB*	88 million byte disc pack drive (with dual access) and 2 PDP-11/70 control units)	47,000
RWP04-CA/ CB*	88 million byte disc pack drive (with dual access and 2 control units	47,000
RP04-AA/ AB*	88 million byte disc pack drive (1.25 μsec/byte transfer time; 8.3 msec average access time)	25,900
RP04-BA/ BB*	Same as RPO4-AA/AB with dual access	30,800
RWS03-BA/ BD*	512K byte fixed-head disc drive and control unit	14,900
RWS04-BA/ BD*	1 million byte fixed-head disc drive and control unit	21,200
RS03-AA/AD	512K byte fixed-head disc drive	9,500
RS04-AA/AD	1M byte fixed-head disc drive 1 μsec/byte xfer time, 8.5 msec average access time	13,800
	Input/Output(1)	
	Magnetic tape	
TWU16-EA/ ED*	Program selectable 1,600/800 bpi magnetic tape transport and control	15,500
TWU16-EK/ EN*	800 bpi magnetic tape transport and control unit	14,450
TU16-EE/ EJ*	Magnetic tape transport	8,950
	Software	
QP210-AD/ AE/AF/AP	IAS (Interactive Application System)	7,800**
QP240-AD/ AE/AF/AP	BASIC	500**
QP230-AD/ AE/AF/AP	FORTRAN IV	700**
QP010-AD/ AE/AF/AP	COBOL-11	7,000**

Notes:

*Indicates 230 VAC, 50 cycle power; first number is 115 VAC, 60 cycle power
**License fee
(1) Other peripherals same as for other PDP-11 systems

DIGITAL EQUIPMENT CORP.
PDP-11/70 System Report Update

Floating Point Processor Halves Execution Time

Digital is now delivering the FP11-C floating point processor for the PDP-11/70. Preliminary tests indicate it increases throughput for floating point operations by factors ranging from two to three. The FP11-C is not only twice as fast as its predecessor, the FP11-B, but it performs more operations in parallel with the PDP-11/70 CPU than the FP11-B. The FORTRAN compiler for the PDP-11/70 supports the parallel operation of the floating point processor and CPU.

Typical instruction execution times for the FP11-C are as follows.

Floating Point Instruction	Execution Time, μsec	
Single-Precision	Register-to-Register	Memory-to-Register
Load	1.1	2.0
Add	1.7	2.0
Multiply	3.3	3.9
Divide	4.3	4.9
Double-Precision		
Add	1.7	2.6
Multiply	5.4	6.6
Divide	6.8	8.0

Floating point numbers consist of a sign bit, 8-bit exponent, and a 23-bit (single-precision) or 55-bit (double-precision) fraction. Floating point numbers are binary normalized, thus, no accuracy is lost for leading zeros as in hexadecimal formats, for example. Single-precision numbers yield 6.8 decimal digits accuracy, and double-precision numbers yield 16.4 decimal digits accuracy.

The FP11-C has 46 hardwired instructions and its own set of six 64-bit accumulators. Besides the basic floating point arithmetic instructions for add, subtract, multiply, and divide, the unit provides the following other instructions:

- Floating point Clear, Negate, and Make Absolute, for direct operations on numbers stored in memory.
- Test and compare for plus, minus, zero, greater than, less than, and equal to.
- Convert integers to floating point numbers.

Cost of the FP11-C is $5,900. First shipments were made in December 1975.

OVERVIEW

The XVM systems are modified configurations of Digital's PDP-15/76. The big news with the XVM systems is the XM15 memory processor that sits between memory and other system components: CPU, interrupt link from I/O processor, and external processor. Not only does it combine a number of features provided by options on the PDP-15 into one unit (automatic priority interrupt, Unichannel multiplexor, memory protect, memory relocate, memory bus interface, and multiport adapter) but it adds a number of new features: instruction lookahead, wide addressing, dual memory buses, memory interleaving (up to 4-way), dual memory relocation registers, user I/O mode, and new high density memory modules. The instruction lookahead feature increases the instruction execution speed of the XVM over the PDP-15/76 by about 40 percent. The maximum I/O rate via the peripheral processor is also increased because of the increased bandwidth due to memory interleaving: 2-way or 4-way. This increased performance allows most PDP-11 processors to function as the peripheral processor; only the PDP-11/10 is used as the peripheral processor for the PDP-15/76.

Software support for the XVM systems will be provided under RSX-PLUS III and DOS. The XVM systems can run in PDP-19/15 mode and run all PDP-19/15 programs.

XVM Models

The XVM systems are available in two models: XVM-100 and XVM-200.

The XVM-100 (Figure 1) is a small one-cabinet configuration that includes the CPU, memory processor, 32K words of memory, paper tape reader and punch, high speed multiply/divide, real-time clock, and LA36 DECwriter II. Memory can be expanded to 98K words in the basic cabinet. It can support the full line of XVM peripherals and software and can be configured into much larger systems including multiprocessor master/slave or ring configurations.

The XVM-200 is a dual processor configuration that includes all the features of the XVM-100 plus a PDP-11 with 8K words of memory as a peripheral processor and a 1.28 million-word disc cartridge drive and control. See Figure 2.

The dual memory bus structure of the XVM models lends itself to multiprocessor configurations. Systems can connect to each other in a master-slave relationship or in a ring relationship. The master is defined as the CPU that can address all the memory of all CPUs in the system as well as its own memory. The slave can address only 8K words of the master's memory in addition to its own memory. In a ring configuration, no CPU is the master; all

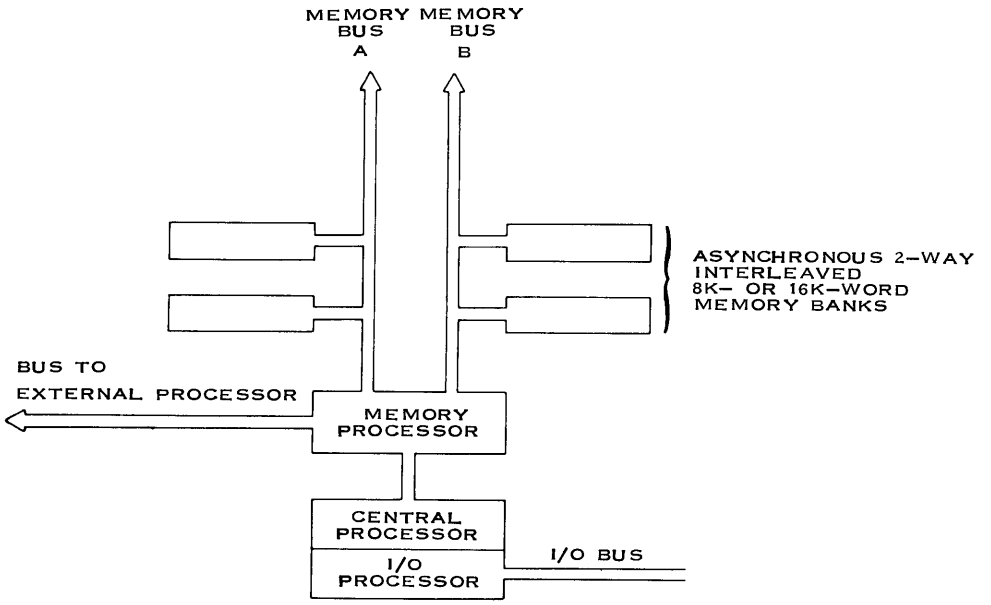


Figure 1. DEC XVM 100: Organization

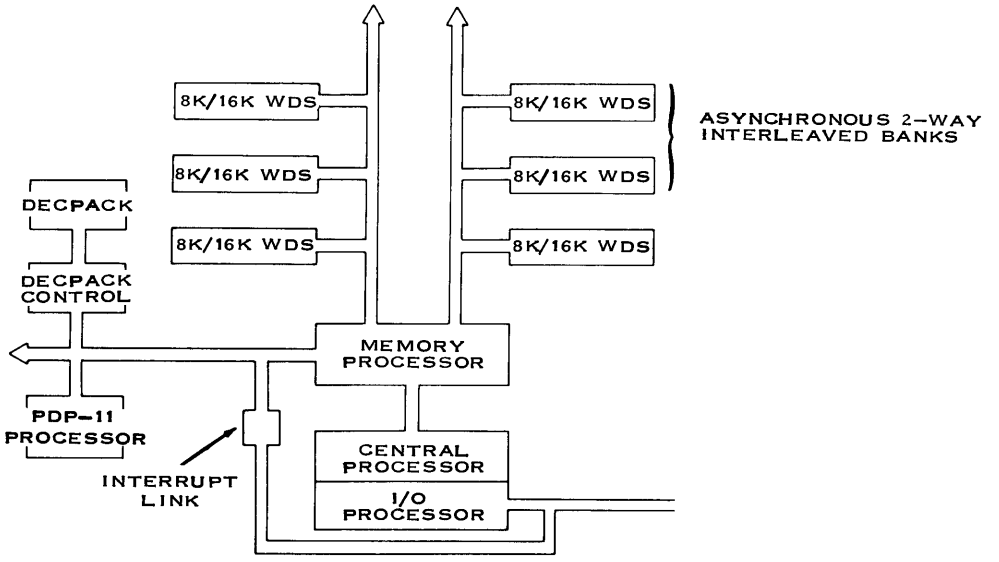


Figure 2. DEC XVM 200: Organization

CPUs in the system can address 8K words of each neighbor's memory in addition to its own memory.

When the PDP-11 is in the configuration, it is always the master because it can address all of the XVM memory. These configurations are now possible with the new PDP-11/70 functioning as a master and XVM systems operating as slaves.

DOS and RSX do not support multiprocessor configurations except for the PDP-11 in a Unichannel configuration. Many PDP-15 users have dual-processor configurations and have altered RSX to support them. Digital will put users in touch with other users who have modified RSX, but Digital does not directly support its operating systems for multiprocessor configurations.

New Features

The instruction lookahead feature provides a 4-word, 80-nanosecond buffer between memory and the instruction register. When an instruction is fetched, the CPU first

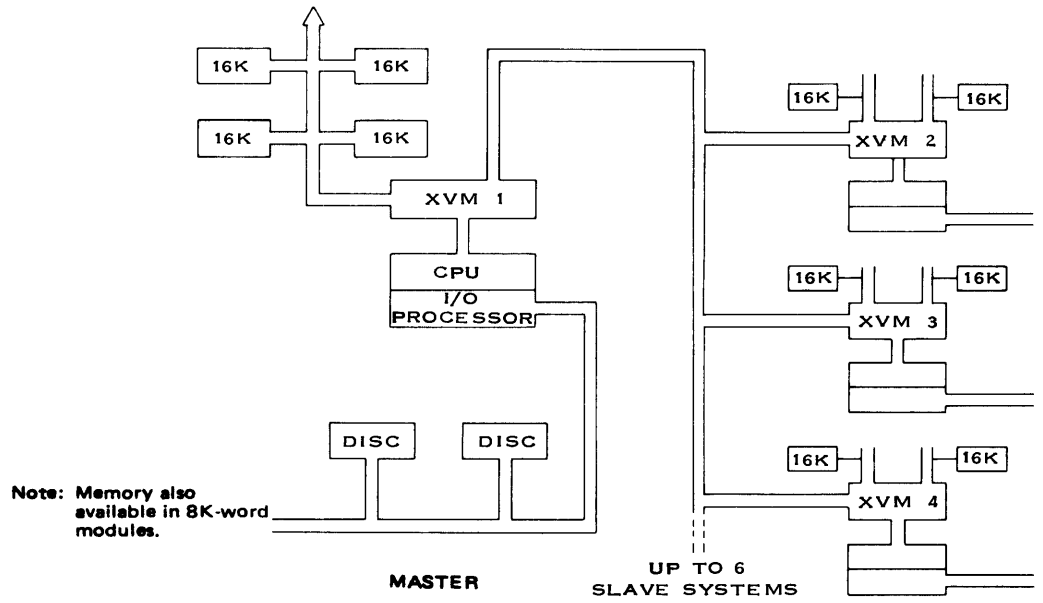
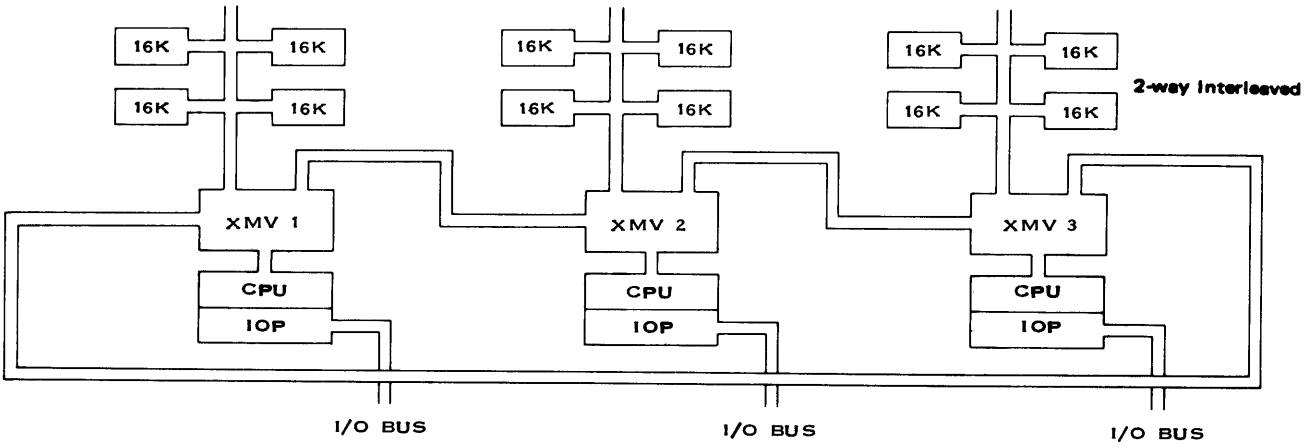


Figure 3. DEC XVM Systems in Master/Slave Relationship

checks the buffer to determine if the word is there. If so, the instruction is loaded into the instruction register. While it is executed, a new instruction is fetched from memory to fill up the buffer. Branch instructions reset the buffer and new instructions are fetched in a pipe-line fashion.

Wide Addressing provides 16-, 17-, or 18-bit indirect addresses for data areas. In PDP-9/15 mode, indirect addresses are 15 bits long. Thus the CPU can address only 32K words in this mode. Instructions are provided to set the addressing mode. The wide addressing allows user programs to address 64K, 128K, or 256K words of data; programs are restricted to 32K words. The software systems do not support 256K words of data. RSX allows any task to be 32K words and the user's data area to be 64K or 128K words. DOS supports 32K words for the executive and user code area and 128K words for the user data area.

Dual memory buses provide 2-way interleaving on each bus for an overall effect of 4-way interleaving. The dual bus arrangement allows memory to connect to one bus and a second XVM system to connect to the other bus. See Figure 3. In the ring configuration, the last processor in the daisy chain connects to the first processor via the mul-



Note: 8K-word modules also available.

Figure 4. DEC XVM Systems in Ring (daisy chain) Relationship

tiplexor connection in the memory processor normally used by the Unichannel for the PDP-11. See Figure 4.

Memory interleaving is normally implemented by interleaving two 8K- or 16K-word modules on each of the two memory buses. Although not yet announced as standard models, XVM systems can have a single memory bus on which two or four 8K- or 16K-word modules can be interleaved.

Dual memory relocation registers allow the split segmenting of a user task under RSX into a local and a global section. The local section is private to the task while the global section can be shared with other tasks. The user program can be given read/write or read-only access to the global section.

One common usage of split segmenting is for multiprocessor configurations where the global space resides in the shared memory area. Global area is divided into two logical areas to simplify code sharing: one area contains the code and another area is equivalent to the beginning of the user's local area to provide local variables.

User I/O mode has been added to EXEC and user modes for processing critical user I/O tasks that cannot tolerate the overhead inherent in the executive I/O handling routines. A task operating in user mode can address memory outside its own area or initiate I/O only through the executive. In user I/O mode, the user task runs under memory protection but can execute direct I/O. Which task(s) can execute in user I/O modes is decided at task installation time.

New MF15 memory modules are based on the MF11-UP core modules used for the PDP-11; 16K words are stored on one board. These modules are 18 bits wide (two bytes plus byte parity for the PDP-11); all 18 bits are used for data on the XVM; thus parity is unavailable on XVM systems. Cycle time for these modules is 980 nanoseconds per word. Two 16K-word modules are interleaved on each memory bus; thus the effective cycle time is considerably reduced for most applications.

Higher speed 8K-word modules are available if greater flexibility is needed in configuring memory banks.

Other features include a relocation disable feature for compatibility with operating systems that do not need dynamic address translation but do need extended addressing. It allows the disabling of the feature under program control.

A high-resolution accounting timer is available for apportioning resource costs among users running under XVM/RSX. Time can be allocated in 10-microsecond intervals.

The memory multiplexor resolves conflicts among the three asynchronous elements that can request access to memory; central processor or I/O processor, instruction lookahead feature, and the multiprocessor adapter for either the PDP-11 or another XVM. The multiplexor is an integral part of each memory port.

Upgrading to XVM from PDP-15

PDP-15 users can upgrade their systems to the XVM by adding the memory processor and removing the system options now incorporated as standard for the XVM systems. The PDP-15 memory protect and relocation hardware, automatic priority interrupt, memory multiplexor, and MM15 or MK15 memory must be removed. They are replaced by the XM15-U memory processor and MF15-U memory. PDP-15 ME15 memory can be field converted for XVM operation; other PDP-15 memory must be replaced.

PDP-15 users can also upgrade to XVM as part of upgrading to an XVM Unichannel configuration with a PDP-11 peripheral processor.

XVM is upward software compatible with the PDP-9 and PDP-15 operating systems: ADSS, B/F, DOS, BOSS, MUMPS, and RSX PLUS III.

XVM Software

Digital is modifying their three major operating systems as well as the RASP (real-time language for simultaneous processing) language to take advantage of the new features available to XVM systems.

The three operating systems are XVM/DOS, XVM/RSX, and XVM/MUMPS.

XVM/DOS will execute about 30 percent faster than PDP-15/76 DOS. FORTRAN and MACRO assembler programs can address up to 128K words of memory: 32K words for program code and 96K words for data defined in common blocks. PDP-15 FORTRAN programs will require recompilation and linking to take advantage of the larger arrays available on XVM.

XVM/RSX will execute faster, and thus it can handle more simultaneous users than RSX PLUS III on the PDP-15. It will support partitions of 128K words: the lower 32K words hold the program and data; the upper 96K words must store data defined in common blocks. The dual relocation registers are used to allow user tasks to address system common data blocks.

XVM/RSX supports EXEC, USER, and USE I/O operating modes.

XVM/MUMPS can support 20 to 48 users in a time-sharing data base management environment. MUMPS includes its own language.

COMPETITIVE POSITION

The XVM systems improve the price/performance of the PDP-15 line. The new high density memories are

cheaper than the older PDP-15 memories. Thus it is more feasible to add memory to enhance performance, especially for RSX and MUMPS systems. In addition, the processor instruction execution speed has been improved over a PDP-15 system by 30 to 40 percent with the instruction lookahead feature. This increased speed makes it feasible to connect larger PDP-11 systems, even the new PDP-11/70, to the XVM systems via the Unichannel.

The major markets for the PDP-15 line have been in the midicomputer range where considerable applications software has been developed by companies outside Digital. Although Digital does not support the software, the company sells configurations that run the software. Initially, Digital is offering configurations for the REDAC and ARK II packages offered by outside vendors for the PDP-15.

The MUMPS software which was developed for Massachusetts General Hospital under a government contract and supported by Digital was first implemented on a PDP-15. It has become popular for hospital applications. In fact, efforts are being made to standardize the MUMPS language. A number of other companies are selling MUMPS systems in competition with Digital, notably Atronix, Inc. Both a MUMPS Users Group and a MUMPS Standards Group have been formed.

The PDP-15 line is increasingly impacted by the surging PDP-11 so in the spirit of "if you can't lick 'em, join 'em," the PDP-15 Unichannel included the PDP-11/10. The "camel" is now even more "in the tent" with XVM. Any PDP-11 system can be incorporated in the Unichannel, and the PDP-11 is the master in the multiprocessor configuration.

The XVM systems will indirectly extend the life of the PDP-15 line. Digital's new network architecture protocols and DECnet software that will be added to RSX will also help. Digital still includes the line in its future plans. Because of its long life, the major development costs have been written off long ago, so the line is extremely profitable.

COMPATIBILITY

The XVM systems are upward software compatible with the PDP-9 and PDP-15. The XVM I/O processor is compatible with the PDP-15 peripherals and the peripheral processor is compatible with the PDP-11 peripherals.

CONFIGURATION GUIDE

The XVM systems can be configured to support all software available for the PDP-15. In addition the XVM can be incorporated in multiprocessor configurations with any PDP-11 processor and/or other XVM systems. All PDP-15 peripherals can interface to the I/O processor and PDP-11 peripherals can interface to the Unichannel.

TYPICAL PRICES

	Purchase Price, $	Maint $	Install $
BUILDING BLOCK CONFIGURATIONS			
XV100-AA/-AB Computer System (all processors [115V, 60Hz/230V, 50Hz]) Includes, in single-cabinet configuration: • KP15 central processor • KE15 extended arithmetic element • KW15 real-time clock • PC15 paper tape reader and punch • LA36 keyboard printer • XM15-UJ/-UK memory processor with 32K words of MF15 core memory • KF15 powerfail and automatic restart	37,500	410	
XV100-BA/-BB Computer System Same as XV100-A except with 64K words of MF15 core memory	46,500	464	
XV100-CA/-CB Computer System Same as XV100-A except with 96K words of MF15 core memory	55,500	518	
XV200-AA/-AB Computer System Includes, in two-cabinet configuration: • XV100-A computer system • PDP-11/10 peripheral processor with 8K words of MM11 core memory • RK15 Unichannel disc system with 1.28M words	57,500	617	
XV200-BA/-BB Computer System Same as XV200-A except with 64K words MF15 core memory	66,500	671	
XV200-CA/-CB Computer System Same as XV200-A except with 96K words MF15 core memory	75,500	725	
XVM MEMORY PROCESSOR OPTIONS			
XM15-BA/-BB Memory Processor (32K word ME15 memory is prerequisite) Includes: • Instruction lookahead hardware • Automatic priority interrupt • Memory protect and relocate • Wide address mode hardware • Split segment register • Task accounting clock • 19-inch cabinet • All cables and power supplies	9,000	98	713
XM15-UJ/-UK Memory Processor Same as XM15-B except with 32K words of MF15 core memory	17,500(1)	152	713
XM15-UL/-UM Memory Processor Same as XM15-B except with 64K words of MF15 core memory	26,500(1)	222	713
XM15-UN/-UP Memory Processor Same as XM15-B except with 96K words of MF15 core memory	35,500(1)	276	713
XVM SUPER-UNICHANNEL DISC SYSTEM			
RK15-LE/-LF Memory Processor and Unichannel Disc Includes: • XM15-UJ/-UK with 32K word MF15 memory	35,000	359	916

PRICE DATA (cont.)

	Purchase Price, $	Maintenance $
• PDP-11/10 with 8K word of MM11 memory		
• KW15 real-time clock		
• RK11-E disc control and RK05 disc drive with 1.28M words storage		
• Interprocessor interrupt link		
• Shared memory adapter		
TYPICAL XVM CONFIGURATIONS		
XVM/DOS or XVM/RSX (Minimum System)	72,600(2)	
Components:		
XVM-200 Computer System	57,500	
DECtape and Control	10,100	
Software:		
XVM/DOS-BOSS Operating System2	2,000	
Est. Software Installation and 1-year Services	3,000	
XVM/MUMPS (Minimum System)	93,430	
Components:		
XVM-100 Computer System	37,500	
9-track Magtape and Control	14,950	
RP152 Disc Pack Drive and Control with 10-million words	27,000	
DC01 Multistation terminal control with 8 lines	6,480	
Software:		
XVM/MUMPS Operating System	4,500	
Est. Software Installation and 1-year Services	3,000	
XVM Batch/Computational System	102,050	
Components:		
XVM-200-B Computer System with 64K core	66,500	
9-track Magtape and Control	14,950	
LP11 Line Printer	10,500	
CR11 Card Reader	5,100	
Software:		
XVM/DOS-BOSS Operating System	2,000	
Est. Software Installation and 1-year Services	3,000	
XVM/RSX Resource Sharing System with 5 Remote Terminals	109,700	
Components:		
XVM-100-B Computer System with 64K Core	46,500	
9-track Magtape and Control	14,950	
RP152 Disc Pack Drive and Control with 10-million words	27,000	
LT19 Communications Interface with Five Lines	7,000	
Five VT50 Video Terminals ($1,250 each)	6,250	
Software:		
XVM/DOS-BOSS Operating System	2,000	
XVM/RSX Operating System	3,000	
Est. Software Installation and 1-year Services	3,000	
XVM Graphics System for Printed Circuit Layout (REDAC(3))	96,600(2)	
Components:		
XVM-200-A Computer System with 32K Core	57,500	
DECtape and Control	10,100	
GT15 Graphics Processor with 17-inch Display	24,000	
Software(3):		
XVM/DOS Operating System(2)	2,000	
Est. Software Installation and 1-year Services	3,000	
XVM Graphics System for Architectural Design (ARK II(4))	116,075	
Components:		
XVM-200-A Computer System with 32K Core	57,500	
DECtape and Control	10,100	
GT15 Graphics Processor with 17-inch Display	24,000	
VW01 Writing Tablet and Control	3,780	
VT05 Video Display Terminal	2,795	
LT15 Terminal Interface	500	
LV11 Electrostatic Printer/Plotter	12,400	
Software(4):		
XVM/DOS Operating System	2,000	
Est. Software Installation and 1-year Services	3,000	
XVM Two-Station Graphics System for Computer-aided Design	132,600	
Components:		
XVM-200-B Computer System with 64K Core	66,500	
DECtape and Control	10,100	
GT15 Graphics Processor with 17-inch Display	24,000	
Second GT15 Graphics Processor	24,000	
Software:		
XVM/DOS-BOSS Operating System	2,000	
XVM/RSX Operating System	3,000	
Software Installation and 1-year Services	3,000	

* All XVM systems and options are discountable.

Notes:
(1) XM15 components replace KA15, KM15, and KT15 hardware, and any MM15 or MK15 memory. Customers presently using this hardware and memory can apply it toward the purchase of an XVM upgrade.
(2) Add $3,000 for XVM/RSX operating system and services.
(3) REDAC applications software is sold and supported by REDAC SOFTWARE Ltd., Newtown, Tewkesbury; Gloucestershire GL20 HE; England. Phone: Tewkesbury (0684) 294161. Telex: 43108. In the U.S., contact REDAC, Inc., 225 Great Road, Littleton MA 01776. Phone: (617) 486-8751.
(4) ARK II applications software is sold and supported by Decision Graphics, Inc., One Court Street, Boston MA 02108. Phone: (617)-742-6395.

HEADQUARTERS

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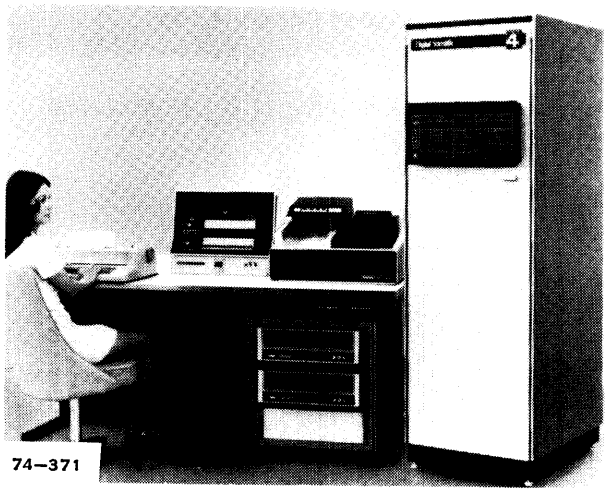

OVERVIEW

The Digital Scientific META® 4 system is a microprogrammed 16-bit minicomputer aimed at the same markets as IBM's 1130 and 1800 systems. The 4030 and the 4040 models provide complete emulation of IBM's 1130 and 1800 systems, respectively. Faster memory cycle time, faster command execution, higher-performance peripheral subsystems, and microprogrammability combined with lower prices for comparable configurations give the META 4 systems considerably better price/performance ratios than IBM equivalents. All IBM features and comparable peripheral subsystems are available to provide complete compatibility for 1130 and 1800 programs, to the extent that IBM diagnostics can run on a Digital Scientific Computer (DSC) system. Digital Scientific supplies software support for microprogramming and a set of system utilities to operate unique DSC peripherals. Operating systems and all other systems and applications software can be obtained from IBM.

Digital Scientific was started in 1967 as a customized systems house. The META 4 was introduced in 1970 as its only "standardized" product. Although the META 4 processor has been used for other types of applications, emulation of the 1130 and 1800 has continued to be the main marketing focus for the product line.

Digital Scientific has sales and service offices in New York City, Washington (DC), Detroit, Chicago, Dallas, and Los Angeles, with additional service offices in San Francisco, Phoenix, Tucson, Houston, Minneapolis, New Orleans, Pittsburgh, Philadelphia, Baltimore, Flint (MI), Danbury (CT), Clarkesburg (NJ), and Montreal (Canada). Headquarters are in San Diego. Leasing in the United States and Canada is handled by Digital Leasing Company. A distributor agreement with Mitsui and Company provides sales and service in Japan; an entry into western Europe is expected in early 1975.

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PERFORMANCE AND COMPETITIVE POSITION

Digital Scientific's main competitor in the 1130/1800 replacement market is the General Automation 18/30. The 18/30 is aimed more at 1130 replacement, because there are more 1130 than 1800 installations. IBM 1800 installations are more customized, hence more difficult to replace. General Automation, moreover, provides compatibility only at the CPU instruction level, and uses its own software to achieve comparable operating environments to some extent, but portions of user programs in some installations might have to be adapted. Also, GA does not attempt to provide any type of plug compatibility for peripheral subsystems. Digital Scientific provides compatibility for devices that attach to an IBM SAC channel and a wider range of peripherals.

For certain applications the META 4 has a significant price/performance edge even if GA's peripheral offerings meet software needs. Digital Scientific states that users have cut execution times by factors of 9, 10, and even 20 over the 1130 by using microcode, particularly for programs that use floating-point calculations. The memory cycle times for both DA and GA systems are half that for the IBM systems; consequently both cut execution times by a factor of at least two.

Other factors that increase the system performance for META 4 include overlapped cycle stealing for DMA transfers and the greater capacity of the disc subsystem, which can be expanded from 10M to 20M bytes. Table 1 compares the hardware of the DSC, GA, and IBM computers.

Digital Scientific is a smaller company than General Automation; both are about the same age. The GA system probably has a competitive advantage for small 1130 users who cannot significantly benefit from microcoding on the META 4 simply because the company is larger. In the 1800 replacement market, however, Digital Scientific is in a much stronger position vis-a-vis General Automation because their system is very similar to the IBM 1800, their microcoding capability can substantially improve performance, and they offer a full line of process I/O.

USER REACTIONS

Digital Scientific META 4 users proclaim it to be a reliable, fast, and price/performance effective system. Most users experienced no problems whatever in converting to the META 4 from their IBM 1130 and 1800 systems. One user said he was "delighted" with the ease of software conversion.

A spokesman for a civil engineering consulting firm handling highway and airport geometry as well as architectural and structural designs for schools, airports, and factories is very happy with the Model 4030. His META 4 improves on the speed and accuracy of this user's former

Table 1. Digital Scientific META 4: Mainframe Characteristics Compared to GA 18/30 and IBM 1130 and 1800

MODEL	DSC 4030	DSC 4040	GA 18/30	IBM 1130	IBM 1800
CENTRAL PROCESSOR					
Microprogrammed	Yes	Yes	No	No	No
No. of Instructions	55**	55**	32	29	31
No. of GP Registers	2*	2*	2	2	2
No. of Index Registers	3*	3*	3	3	3
Real-Time Clock	Yes	Yes	Yes	No	No
I/O					
Programmed I/O	Yes	Yes	Yes	Yes	Yes
DMA (no. of channels)	9	9	5	5	3 std, 6 opt
MEMORY					
Cycle Time (μsec)	0.90	0.90	0.96	2.2, 3.6	2.0, 4.0
Parity	Std	Std	Std	Std	Std
Protect	Std	Std	Std	None	Std
ROM (wds)	1K-4K	1K-4K	None	None	None
Core Size (wds)	8K-32K	8K-64K	32K	32K	64K
PERIPHERALS					
Max Speed for					
Card Reader (cpm)	1,000	1,000	1,000	1,000	400
Line Printer (lpm)	600	600	600	600	600
Mag Tape Drive (ips)	75	75	75	None	None
Disc Subsystem					
Capacity (wds/drive)	512K, 10M	512K	512K 2.5M, 10M	512K	512K, 2.5M
Access Time (μ sec)	–	–	45	750	75

*Assigned from bank of 28 registers.
**34 standard, 16 with optional floating-point firmware.

IBM 1130 and he has had no downtime. This firm ran benchmarks written in FORTRAN using real-number arithmetic and no I/O and found the META 4 outperformed an IBM 370/135. This company had a fast 32K-word memory on the 1130, and FORTRAN programs with no I/O, ran 15 times faster on the META 4 than on the 1130. The firm wanted spooling to a card punch and a plotter. The META 4 system maintained the system cycle time, even with the spooling operations. With the flexibility shown by the META 4 system, the firm plans to add time-sharing terminals to the present 4030. The user investigated the IBM 370/125, DEC's PDP-11/45, the General Automation 18/30, and the option of enhancing the 1130. This user feels the decision to go with Digital Scientific has been a good one for the company.

A consulting firm for aerospace, government, and business agencies uses the META 4 Model 4030 for "scientific number-crunching." The system analyzes data from experimental tests and models physical processes. The META 4 is particularly effective in scientific simulation, handling numerical solutions of partial differential equations. The user looked at the General Automation 18/30, as did most of the users interviewed. This firm was primarily interested in maximum software compatibility with the 1130, which Digital Scientific assures. The user wanted the performance of a Univac 1108 or a CDC 6600 but without the expense of these large systems. The META 4, in this user's estimation, provides comparable performance, a bit slower, and certainly less expensive.

A software house specializing in IBM 1130- and 1800-compatible software uses a Model 4030 for software development and rents the machine to a service bureau for eight hours a day. This user thinks the META 4 is an excellent system, faster, and more capable than an IBM 1130. This user has had the system for over two years and has experienced no problems.

A major advertising agency uses the META 4 Model 4030 for scientific, statistical, and research processing. The firm finds the META 4 quite satisfactory for its needs and faster than the 1130. This system has been installed for over four years; the firm experienced some start-up problems but these have long since disappeared. The firm had minor mechanical problems with the first printer supplied; it was not rugged enough to withstand the beating it was given. Later printers proved more sturdy. One reason this firm chose the META 4 is its IBM-1130 compatibility. Many marketing research companies use 1130-type systems and they share programs among themselves.

Users of the META 4 Model 4040 are generally very pleased with their IBM 1800 emulators. One uses the

Model 4040 in a process control environment. It controls seven or eight laboratory stations handling tests for integrated circuits and frequency selective devices. This company had an IBM 1800 but found it was too slow and required too much space. Price and speed were the deciding factors for the META 4. This firm has recently added 40K bytes of memory and would like to add a high-speed line printer. The user has had problems with the console and systems printers, saying it was rare when both work simultaneously. He considered this a minor problem and stated he had no big problems with the system.

A scientific institute uses the META 4 as a flexible data base management and data acquisition system. This user had found the performance of the META 4 superior to that of his previous IBM 1800. Installed over two years ago, he has experienced no hardware downtime with the META 4 and no software problems. Benchmarks developed for the system ran ten times faster on META 4 than the IBM 1800. This user wanted hardware multiply and divide, which the IBM system did not have and needed to handle complex mathematical equations. The META 4 cost is half the price of the 1800.

A major automobile manufacturer uses the META 4 to test exhaust emission, engine endurance, and carburetor flow. This system was recently installed, so new acceptance tests are still being run. So far, the system is doing well aside from some initial burn-in problems, with no problems with software, previously run on an IBM 1800.

Digital Scientific's maintenance is described as good to excellent by most users; a few users are a little disappointed with response time and competency. One user was impressed with DSC's uniformly bright, knowledgeable, and experienced customer engineers. Another describes the service as competent but response time varies; it is usually within acceptable norms, however. A third user found that the customer engineers lack experience. A simple wiring error was at fault for one user's system failures and repeated visits by DSC brought no solution. This user found the error and corrected it himself.

CONFIGURATION GUIDE

The basic META 4 processor with an 8K-word memory consists of three models: the 4030 emulates the IBM 1130; the 4040 emulates the IBM 1800; and the 4031 provides for user-supplied emulation. The 4030 and 4040 differ in the standard emulation and I/O backplane controllers; thus, they support different I/O options. The Model 4030 processor options include a real-time clock, hardware (firmware), floating-point arithmetic, 1K-word (16 bits) ROM modules, and a storage access channel (SAC). Six interrupt lines, three index registers, two accumulators, and 39 instructions are standard features. The floating-point option adds 16 instructions for a total of 55.

Model 4040 includes a real-time clock and 14 interrupt levels as standard features, and, like the 4030, it provides ROM modules and floating-point arithmetic options. Nine DMA data channels are standard features; a set of five OEM channels (to attach non-IBM devices) and a selector channel are available. An I/O typer and controller can supplant the standard console.

Memory can be expanded in 8K-word increments up to 32K words on the 4030 and 64K on the 4040, but memory modules added above 32K words carry an additional field installation charge.

IBM specifies a maximum of 10 I/O devices on an 1130 and up to 12 data channels on an 1800. DS allows up to 28 devices to be attached to either system, but not all devices can go on both. Communications adapters are available for the 4030 for instance, and analog/digital I/O subsystems can be attached to the 4040.

Table 2 lists the peripherals available for the 4030 and 4040 as compared to those available for the 1130 and 1800. Digital Scientific supplies little software for the META 4 because the system is designed to run the software available for the 1130 and 1800. Only the software listed in Table 3 is available.

Table 2. Digital Scientific: META 4: 4030 and 4040 Peripherals

Device	DSC 4030	IBM 1130	DSC 4040	IBM 1800
Disc (512K wds)	1448	2310	1448	1810
Disc (100M wds)	1445	NA	NA	NA
M/7 (37 ips)	3412	NA	3412	2401/02
M/7 (75 ips)	3416	NA	3416	2401/02
Card rdr (600 cpm)	3463	2501	3463	NA
Card rdr (1,000 cpm)	3465	2501	3465	NA
Printer Keyboard	NA	NA	4133	1053/ 1816
P/T Reader	3431	1054	3431	1054
P/T Punch	3421	1055	3421	1055
Printer (600 lpm)	3482	NA	3482	NA
Printer (300 lpm)	3484	1403	3484	1443
Plotter	3442	1627	3442	1627
Digital Input	NA	NA	4200	Misc
Digital Output	NA	NA	4232	Misc
Analog Input	NA	NA	4258	1851
Analog Output	NA	NA	4234	1856
Process Interrupt	NA	NA	4214	Misc
Bisync Communications	4101	BSC adapter	NA	NA
Multiterminal Communications Adapter	4108	RPQ	NA	NA
Real-Time Clock	4185	NA	NA	NA
Floating-Point Firmware	9078	NA	NA	NA

COMPATIBILITY

The META 4 systems are compatible with IBM's 1130 and 1800 computers at the instruction level; they

Table 3. Digital Scientific META 4: Software

Package	Description
Microassembler	Converts symbolic microcode to machine language; requires 8K words of memory, card reader, printer, disc
System Utilities	Object deck punch, ROM debug; require 8K words of memory, disc, card reader, console printer

are also I/O-compatible in that IBM peripherals can be used with the META 4. DSC supplies compatible peripheral subsystems and some compatible controller interfaces to provide better price/performance. Controllers that effectively create 1130 SAC channels or 1800 data channels are attached to the META 4 backplane to allow any IBM controller to be attached.

The IBM 1130 instruction set is a subset of the 1800. Although the 1800 has a fuller complement of peripheral offerings, 1130 and 1800 programs can run on each other's systems if the peripheral environment is the same, and if the 1800 programs do not use instructions unavailable on the 1130. Unlike IBM's 1130, the DSC 4030 has provisions for handling 1800 instructions (among others) on the 1130 emulator.

MAINTENANCE

Digital Scientific handles maintenance through area service offices across the United States. The standard maintenance contracts provide for periodical preventive maintenance visits and emergency on-site service. Contracts can cover one, two, or three shifts during the week or on weekends. Users who have purchased systems can also obtain maintenance on an hourly basis instead of through a monthly contract. Provision is not made for a dedicated on-site engineer on a contractual basis although a large remote installation may have the undivided attention of the area engineer.

TYPICAL PRICES

Model Number	Description	Monthly Rental $ YR*	Purchase $	Monthly Maint. $
	CENTRAL PROCESSOR AND WORKING STORAGE			
	Processor and Options			
4001-X[1]	META 4 Basic Processor	—	10,225	—
4011	Memory and I/O Register	—	1,500	—
4012	I/O Register	—	550	—
4013	Double-Bus Accumulator	—	350	—
4025	Scratch-Pad Memory	—	3,000	—
4150	Microprogrammer's Panel Firmware	—	975	—
1425	Read-Only Memory	—	2,725	—
9000	ROM Pattern Boards	—	400	—
9100	Custom Artwork	—	400	—
9101	Custom ROM Pattern Board	—	25 each	—
	IBM 1800 Emulator			
4040	Basic Processor	1,157	32,800	219
4118	OEM Channels (set of 5)	117	5,000	34
4125	Selector Channel (4040 prereq)	327	9,250	62
9078	Floating-Point Arithmetic	29	1,000	—
4133-0	I/O Typer and Controller	124	3,500	24
	IBM 1130 Emulator			
4030-1	Basic Processor — 8K	1,170	33,175	222
-2	Basic Processor — 16K	1,431	40,575	271
-3	Basic Processor — 32K	1,981	56,200	375
4031	Processor without Emulator	759	21,500	144
4130	Storage Access Channel	43	1,200	8
4185	Real-Time Clock	23	625	5
9078-1	Floating-Point Arithmetic	29	1,000	—
	4031 and 4040 Core Memory Subsystems			
4068-1	8K	351	9,925	67
-2	16K	611	17,325	116
-3	24K	901	25,550	171
-4	32K	1,162	32,950	220
-5	40K	1,475	41,830	279
-6	48K	1,736	45,230	329
-7	56K	2,026	57,455	384
-8	65K	2,286	64,855	433
4069	Auxiliary Core Feature for 4068	283	8,000	54
	MASS STORAGE			
	For 4040			
1444-2	Disc Subsystem (512K words)[2]	342	9,500	70
1448-2	High-Speed Disc Subsystem (512K)	406	11,500	77
	For 4030			
1445-1	Disc Subsystem (10M words)	775	21,000	175
-2	Additional Drive (20M word total)	604	16,500	132
1448-1	Disc Subsystem (512K words)	406	11,500	77
	INPUT/OUTPUT MAGNETIC TAPE[2]			
3410-2A	Single Drive (7-track; 37.5 ips; for 4040 only)	397	11,250	75
3410-2B	Dual Drive (7-track; 37.5 ips; for 4040 only)	608	17,250	115
3412-2A	Single Drive (9-track; 37.5 ips)	405	11,450	77
3412-2B	Dual Drive (9-track; 37.5 ips)	623	17,650	118
3416-2A	Single Drive (9-track; 75 ips)	492	13,950	93
3416-2B	Dual Drive (9-track; 75 ips)	711	20,150	135
	Punched Card[2]			
3463-1/2	Card Reader (600 cpm)	210	6,950	40
3465-1/2	Card Reader (1,000 cpm)	281	7,950	53
3472-2	Controller for IBM 1442 Model 5, 6, or 7	177	5,000	34
3463-1	Card Reader (600 cpm)	210	5,950	40
3472-1	Controller for IBM 1442 Model 5, 6, or 7	105	2,500	33
3474-1	Controller for Univac VIP 1710 Punch	106	3,000	20
	Paper Tape Equipment			
3421-X	Punch (50 cps)	129	3,640	25
3431-X	Reader (400 cps)	111	3,120	21
3432-X	Reader with Spooler	155	4,365	30
	Printers[2]			
3482-2	Printer (600 lpm)	864	24,500	164
3484-1/2	Printer (300 lpm)	442	12,500	84
3482-1	Printer (600 lpm)	731	19,875	163
3486-1	Printer (165 cps)	362	10,250	69
	Plotters[2]			
3443-X[1]	XY Plotter Controller for DSC 3442, Houston DP-1, CalComp 500, and IBM 1627	36	1,000	7

TYPICAL PRICES (Contd.)

Model Number	Description	Monthly Rental $ 1YR*	Purchase $	Monthly Maint. $
INPUT/OUTPUT MAGNETIC TAPE(2)				
3442	XY Plotter (3443-X required)	177	4,975	34
3444-1	Controller for CalComp 700 Communications (for 4030 only)	53	1,500	10
4101-1	Binary Synchronous Communications Adapter	152	4,275	29
4108-1	Multiple Terminal Communications Adapter (8 lines)	169	4,775	32
0401	Cabinet	27	750	5
4100-X	I/O Chassis Extender	89	2,500	17

Notes:
(1) X = 1 for 1130 Emulation System.
X = 2 for 1800 Emulation System.
(2) Subsystems include interface to META 4; generally submodel 1 refers to 4030 and 2 to 4040.
*Rental prices include maintenance.
— Not Applicable.

HEADQUARTERS

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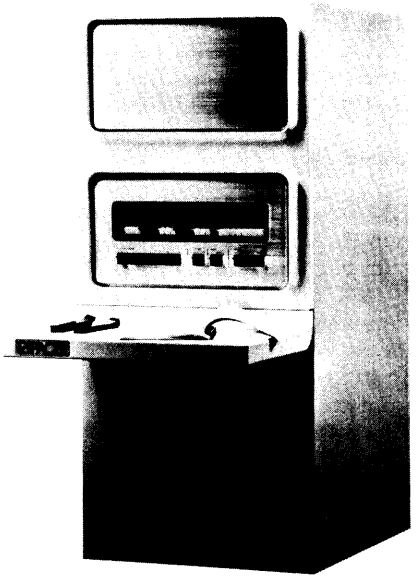


OVERVIEW

The EAI PACER, a single-address, word-oriented binary computer, features a 1-microsecond cycle time, 16-bit parallel data path, and flexible peripheral-interrupt facilities. PACER is a general-purpose minicomputer that handles real-time process control applications as well as hybrid computation, communications, and batch processing. It utilizes compact MSI and LSI circuitry and submicrosecond planar memories. All options are prewired and plug-in. A built-in universal controller accepts plug-in device controllers and/or plug-in data acquisition components.

EAI supports the "you-name-it, we-support-it" minicomputer concept, based upon the continuing cooperative effort that must exist between manufacturer and user for a successful business association. For example, ProPACE™, an automated system for monitoring data reduction, display, and control of process gas chromatographs, is designed for operation in petroleum refineries and petrochemical and natural gas processing plants. PACER graphic systems use the proven Dataplotter® for structural design, roadwork design, schematic drawings, printed circuit layouts, and Pert charts. System software, such as TOS or DOS, is already field proven, as is PACER'S predecessor processor, EAI 640, which was announced in November 1966. Since its first delivery in April 1967, approximately 200 systems have been installed.

ProPACE™, a trademark of EAI.
Dataplotter®, a registered trademark of EAI.

PACER, a direct descendant of the 640, was announced in March 1972 and features the improved economical circuitry and design of fourth-generation electronics. It also offers internal design improvements such as "transfer mode," "user zone zero," a new memory protect scheme, improved software, two memory ports, and two optional DMA channels. PACER is also about 50% faster than the 640.

Configuration

PACER is designed modularly and compactly; system configuration requires consideration of certain physical constraints. For example, no more than 64 device controllers can be attached to one system.

All controllers and components, except for the peripheral units themselves, are housed in the central processor rack or the 1910 expansion rack. The central processor rack contains:

- Central processor.
- Memory and optional memory.
- Four standard channels.
- Channel clocks.
- Alarm channel.
- Optional direct memory access channels.
- Universal I/O module.
- Up to five minicontrollers.

Except for magnetic tape and disc units, communications devices, and the floating-point processor, all peripheral units (except some ADC/DAC devices that are integral parts of a minicontroller) are cabled to minicontrollers. The optional interval timer is treated as a minicontroller.

The 1910 expansion rack houses up to nine expansion units. When the expansion rack is used, one of the minicontrollers in the central processor rack must be the 1801 long line adapter that extends the I/O bus lines 100 feet and conditions line signals. The following peripheral devices require the indicated number of expansion units.

Device	Number of Expansion Units
Paper tape reader	1.5
Paper tape punch	3.0
Cartridge tape unit	1.5
I/O universal modules	3.0

Each universal module provides power and housing for eight minicontrollers and four communications line units. One of the controllers can be the 1850 communications subcontroller.

Basic Configuration. The central processor, 8K words of memory, and an ASR Teletype make up the basic configuration supported by PTS, the paper tape software system.

Extended Configuration. The cartridge tape system (COS), the magnetic tape system (TOS), and the disc operating system (DOS) are batch processing systems that require the peripheral specified as the program loading device. Though these systems can operate in as little as 8K words of memory, the user would be hard pressed for machine time in a moderately active installation.

Consider that the executive requires about 1K to 5K words of memory, the core image loader 0.5K words, source language processors from 3K to 6K words, and diagnostics and utilities from 0.8K to 1.5K words. It is reasonable to assume, therefore, that an extended configuration should include a minimum of 16K words of memory if more than one type of activity is to be processed by the system at any time.

Compatibility

The PACER is upward compatible with the EAI 640; that is, programs that will run on the 640 will run on the PACER. The only possible exceptions are special application programs that depend on the processor's cycle time in a hybrid system. Programs developed for the 640, however, will not take advantage of features unique to PACER. System software developed for PACER, such as the Real-Time Operating System, will not run on the 640.

Competitive Position

The EAI PACER, like the EAI 640, will be marketed for hybrid analog and digital, laboratory automation, and graphic system applications. EAI has a well-earned reputation for its fine hybrid systems utilizing EAI analog devices, which are fully software supported. In addition, EAI has developed turnkey hardware/software systems for laboratory automation and graphic displays.

Major competitors with the EAI PACER are DEC's PDP-11, IBM's 1800, and, particularly in Europe, the Xerox Sigma 3.

PACER has a clean, modern image as a system. Its design follows a middle of the road philosophy that indicates conservative reliability. This, combined with EAI's reputation for analog devices and good sales and field support, should assure EAI's continued success.

MAINFRAME

PACER's real-time multitasking system depends upon its I/O and interrupt processing capabilities and requires 16K words of core.

The demand, however, to utilize the central processor fully increases with competitive and economic pressures. As CPU utilization increases, more core is required. PACER, limited to 32K words of core memory, overcomes this constraint by temporarily rolling out background programs when foreground tasks require more memory.

EAI relies on a viable configuration and good languages. An articulate command system, the dynamic availability of the functional library routines, and the interactive debug facilities stand the user in good stead. The software can be effectively utilized from a selection of local and remote terminals. This well-rounded approach makes the PACER an effective computing system.

Central Processor

EAI PACER is a stored program, general-purpose digital computer that features a 1-microsecond cycle time. The 16-bit, word-oriented processor provides single- and double-precision fixed-point arithmetic in two's complement notation. Floating-point arithmetic is implemented by the optional FP processor that interfaces to the central processor via standard I/O channels. Floating-point operands are single-precision, 32 bits.

Memory consists of 8,196 words of magnetic core expandable to 16K or 32K words. All memory modules have two ports of entry. Two direct memory access channels are optionally available for high-speed data transfers between memory and peripheral devices. Up to 64 devices can be connected to a system and each can be individually serviced via 64 self-identifying priority interrupt levels.

Other CPU features include seven internal priority interrupts: memory protect, power failure detection with automatic restart, an interval timer, and four optional channel timers. An alarm channel signals device-inoperable conditions to the operator. Major central processor characteristics are summarized in Table 1.

Table 1. EAI PACER 100: Mainframe Characteristics

CENTRAL PROCESSOR	
No. of Internal Registers	10 (1 accumulator, 1 extension register, and 1 index register)
Addressing	
Direct (no. of words)	512
Indirect	32,768
Indexed	32,768
Instruction Set	
Number (std, opt)	91 std, none opt*
Binary Arithmetic	Std w/multiply & divide
Floating-Point Arithmetic	Optional*
Priority Interrupt System	
Lines	4
Levels	64
MAIN STORAGE	
Type	Magnetic core
Cycle Time (μsec)	1.0
Basic Addressable Unit	Word
Bytes per Access	Two
Min Capacity (bytes)	16,384
Max Capacity (bytes)	65,536
Increment Size (bytes)	16,384 or 32,768
Parity	None
Protect	Yes
ROM	
Use	Bootstrap
Capacity (bytes)	128
I/O CHANNELS	
Programmed I/O	Yes
DMA Channels (no.)	2 optional
Multiplexed I/O (No. of subchannels)	4
Max Transfer Rate	
Within Memory	250K words/sec
Over DMA	1M words/sec

Notes —

* Floating-point processor operates as an I/O device and uses I/O device function codes for load, store, add, subtract, multiply, divide, and negate.

Floating-Poing Processor (FPP). The optional FPP operates asynchronously to the processor as a peripheral device on the standard I/O channel. The FPP is buffered; thus the processor can load FPP operands while FPP computation is in progress. Data is exchanged between the FPP accumulator (32 bits) and the CPU accumulator (16 bits) by two consecutive I/O instructions. Typical execution times in microseconds, excluding data transfer and normalization of values, are as follows:

Instruction	Execution Time (μsec) Min	Max
Add	1.5	6.0
Subtract	1.5	6.0
Multiply	5.7	9.4
Divide	9.5	10.2

All floating-point operations have a post normalize option, and multiply has a "round" option.

Data Structure. Based upon a 16-bit word, two 8-bit characters or one 15-bit number with sign are stored per word. Double-precision fixed-point or single-precision floating-point operations use two words, 32 bits. I/O devices use a binary or ASCII code. Conversion between codes is done by library routines. Table 2 summarizes the data structures.

Table 2. EAI PACER 100: Data Structure

Data Name	Representation
Character	7 bits ASCII
Byte	8 bits
Halfword	8 bits
Word	16 bits
Word (double length)	32 bits (double-precision)
Instructions	16 bits
Decimal Operand	None
Binary Operand	15 bits + sign bit
Floating-point operand (short)	32 bits: 8-bit signed exponent, 24-bit signed fraction
Floating-point operand (long)	None

Standard Registers. The accumulator (A) and extension accumulator (Q) are 16-bit general-purpose registers used for arithmetic and logical operations, I/O control operations, and the transfer of data. One 16-bit index register, X, is provided; 15 bits are used for indexing; the sign bit acts as a post-index indirect addressing flag. The contents of the index register can be exchanged with any core location without affecting either accumulator. This is a useful feature because either the register or any core location can be automatically incremented and conditionally tested by a single instruction. An array of pointers and/or loop counters can, therefore, be used as an indirect vector table, with or without indexing; it can be used as a convenient audit trail for debugging or as a general method for convenient file modification.

The mask register (K) or program status word (PSW) contains the interrupt-enable bits, the condition code bits, the arithmetic multiprecision and carry bits, and the operating mode (transfer/user) bits. It is modified via the accumulator by utilizing a control instruction and is generally unavailable to the user except through the software executive system. Testing the arithmetic indicators is done via instruction and does not require direct access to the K register by the user.

The base/limit register is controlled by the executive program. This register is loaded with the lower and upper boundaries of the current user program. Due to the eight-bit size of a halfword, the base and limit are expressed as multiples of 256 words. The base value of this register is automatically added to the displacement of any user instruction. Address references that exceed the values in the base/limit register are flagged as memory protect violations. The base value is also utilized when the executive employs the transfer mode.

The program counter (P), operand (R) and instruction (I) registers, and the memory data (M) and memory address (S) registers are control registers that are used by the hardware.

Addressing Facilities. PACER provides absolute, indexed, relative, and indirect addressing facilities. In addition, an executive transfer mode provides for effective communication with the executive in a multiuser environment.

Memory referencing instructions use the following format:

Function	Mode	Displacement
4 bits	3 bits	9 bits

The mode bits indicate absolute or relative addressing, no indexing or indexing, and direct or indirect addressing.

Absolute Addressing. The displacement field of an instruction is treated as a nine-bit positive number (absolute mode) when the relative addressing mode bit of the instruction is reset. The nine-bit number yields a range of 0 to 512 addresses that fall into zone zero. Zones 1 through n are addressed by indexing, or by relative or indirect addressing. In a multiple-user environment, PACER provides each user with his own zone zero. This is achieved by adding 256 times the base value contained in the base/limit register to the displacement of all instructions that indicate absolute addressing when the processor is operating in the user mode.

Transfer Mode. In a multiuser environment, the executive must communicate with user programs. When an interrupt occurs, the executive suspends the current user program, and processes the causes of interrupt. Before processing can begin, the executive must temporarily store the current user's variables in the user's communication area, i.e., zone zero. PACER uses the transfer mode to do this. In transfer mode, the base value in the base/limit register still points at the user's zone zero — and the executive data transfer instructions (Load/Store Accumulator) use this base value to find the user's zone zero. Transfer mode and user mode bits are set by the executive in the program status word (PSW). The transfer mode bit is reset by each Load or Store instruction; thus the executive must set it each time it is used for a transfer.

Relative Addressing. The displacement field of an instruction is treated as a signed 8-bit value when the relative addressing mode bit of the instruction is set. The 8-bit value yields a range of 0 to 512 addresses that vary from -256 to +255. This displacement is added to the current value of the P counter to provide an actual address.

Indexed Addressing. The displacement value is added to the low-order 15 bits of the index register. When combined with indirect addressing (IA instruction bit set), indexing succeeds indirect addressing. If the high-order bit of the index register is set, however, indexing precedes indirect addressing.

Indirect Addressing (IA). PACER offers preindexing IA and postindexing IA for memory reference instructions. When the indirect mode bit of the instruction is set, the absolute or relative address points at the operand address.

Only 15 bits are required to address any cell in main memory. The high-order bit of the operand address is used as a multilevel IA indicator. If it is set, another level of IA occurs; if it is reset, indexing occurs when specified or the address is used as the operand address. If the high-order bit of the index register is set, another level of IA occurs.

IA requires an extra machine cycle for each level of indirect addressing.

Instruction Set. PACER provides 91 standard instructions. Instructions to control the floating-point processor are implemented as I/O instructions. Noteworthy instructions include those that reset control bits in the PSW, the exchange instructions that swap the accumulator with other registers, the combination index and skip instructions, and the link and trap instructions. The host of skip instructions that sense almost every condition are convenient for processing alternating conditions. Table 3 provides sample of generic instructions and their typical execution times.

Table 3. EAI PACER 100: Instruction Set

Type	Number	Typical Execution Time (μsec)
Load and Store	10	2.0
Fixed-Point Binary	5	2.0 (add) 6.0 (multiply) 6.6 (divide)
Floating Point	4	6.0 (add)* 9.0 (multiply)* 10.2 (divide)*
Logical	5	2.0
Branch	11	1.6 or 1.2
Shift	8	1.4 + 0.2 N
Compare	1	2.2
Move	—	—
I/O	10	—
Miscellaneous	12	1.2

Notes:

* FP optional instructions showing worst-time unnormalized computation.
N Number of bits shifted.

Interrupt Control. An interrupt causes PACER to store the contents of the program counter automatically in the location addressed by the device interrupt pointer; the content of the accumulator is then stored in the pointer location plus one. The next location (pointer address plus two) contains the first instruction executed in the interrupt servicing routine. The pointer itself is in a fixed memory location assigned to each interrupt. PACER provides 64 distinct interrupt pointers for external interrupts and seven for internal interrupts.

PSW contains the enable/disable bits for each interrupt level.

Interrupt Level	PSW Bit Position	Interrupt Description
1	0	Trap Instruction
2	1	Illegal Instruction
3	2	Square Root Instruction
0	3	Memory Protect Violation
4	4	User I/O Fault
5	5	Interval Timer Overflow
7	6	Channel 0 Interrupt
8	7	Channel 1 Interrupt
9	8	Channel 2 Interrupt
10	9	Channel 3 Interrupt
6	10	Alarm Channel Interrupt
11	11	Allow User I/O
12	12	Carry/Borrow Bit
13	13	Multiple Precision Bit
14	14	Condition Code
15	15	Condition Code

PSW is the K (or mask) register. The master interrupt flip-flop enables or disables the entire interrupt scheme of the processor except for power failure interrupt which will occur regardless of any interrupt setting.

Internal Interrupts. These have the highest priority except for power failure. These interrupts are disabled if the master interrupt flip-flop or PSW bits 0 to 5 are reset.

The power failure interrupt occurs if line voltages exceed a 105- to 135-volt range. There is sufficient time (500 microseconds) to store the contents of the hardware registers before the computer stops. The program counter and accumulator are automatically stored on interrupt.

The trap instruction clears bits 0 through 7 and modifies bits 8 through 15 of the accumulator. Bits 8 through 15 designate 1 of 256 code possibilities that determine the reason for the programmed interrupt.

Illegal instruction occurs when PACER determines the current operation code is invalid.

Square root trap occurs when the square root instruction that is valid for the EAI 640 but invalid in the PACER is attempted. It links to a software routine to perform the function to provide compatibility with the 640.

Memory protect violation occurs when a program in user mode attempts to address a memory location outside the range specified in the base/limit register. Control passes to the executive.

Privileged instructions are normally prohibited when the processor is operating in the user mode. When PSW bit 11 is set, however, the user can perform his own I/O operations. Privileged instructions include any I/O instruction except those for the FP processor, reset master interrupt, exchange status word, or exchange base/limit register.

External Interrupt. I/O devices are connected to one of the four channel interrupts; channel zero has the highest priority. Although I/O interrupts can be disabled, they remain pending until serviced. When a device generates an interrupt on the I/O bus, the processor — upon recognition of the signal — stores the program counter and the accumulator and branches to pointer plus two. This location should contain a branch to the device service routine.

Besides the channel interrupts, which indicate that I/O service is required, the alarm channel interrupt indicates that an attached device is inoperable and cannot perform any service in its current condition.

MAIN STORAGE

Basic storage in the PACER's main memory consists of 8,192 words of random access magnetic core. Memory can be expanded to either 16,384 or 32,768 words. Storage cycle time, which is the minimum time between two successive read/write operations, is 1 microsecond.

Memory protect is provided via the base/limit register which can protect memory in 256-word blocks.

Memory parity checking is considered unnecessary because memory has an MTBF (mean time between failures) of 32,000 hours.

Two direct memory access ports are basic to the memory modules. The two optional direct memory access channels can plug directly into these ports and transfer data simultaneously with each other on a cycle-stealing basis.

Maximum data transfer rate within memory is 250,000 words per second using straight line coding.

I/O CONTROL

Three modes of I/O are available to the PACER processor: word, record, and buffered record. Word and record modes operate via the standard channel, while buffered record mode operates via an optional direct memory access (DMA) channel.

Word Mode. The data in (DI) and the data out (DO) instructions transfer one word of data (16-bit parallel) between the accumulator and a specified device on the standard data channel. An instruction is required to transfer each word. Word mode is used to service low-speed I/O devices via the interrupt system while the program operates concurrently.

Record Mode. The record in (RI) and the record out (RO) instructions transfer one or more words of data (16-bit parallel) directly between main memory and a specified device on the standard data channel. The RI/RO instructions use a four-word control packet stored in memory, which contains a device function word, final address plus one, starting address, and I/O termination address. Upon termination, the address of the last word transferred is stored in the last word of the packet. Record mode is used to service very high-speed I/O devices using the standard (unbuffered) data channel. It interlocks the processor for the duration of the complete record transfer.

Buffered Record Mode. Two DMA channels can plug into the DMA memory ports and signal interrupts via I/O channels 1 and 2. In this mode, data is assembled/disassembled automatically by the channel. These channels operate on a cycle-stealing basis and can transfer a maximum of one million 16-bit words per second. (The processor is effectively locked out at this speed.) Adding DMA channels to the system does not affect the maximum number of peripherals the system supports (64 devices).

Simultaneity. The processor operates concurrently with I/O devices in word and buffered record modes, but is locked out in record mode. The standard channel and the buffered channel can operate simultaneously, but all references to memory are interleaved regardless of source.

Interval Timer. The interval timer expansion is a form of minicontroller that provides a high-resolution real-time clock and up to four pulse generators to drive the channel clocks.

The real-time clock is a 16-bit counter that can be loaded by program or manually with a thumbwheel. It increments every microsecond and generates an interrupt when reaching zero.

Pulse generators provide intervals of 1, 2, 10, 20, 100, 200, and 1,000 milliseconds for the channel clocks. Four memory locations in executive zone zero are used as clock counters. The channel clocks increment every time they are pulsed and generate an interrupt when reaching zero. Channel clocks can accept an external source for pulse signals.

PERIPHERALS

The 1810 universal controller provides efficient and economical systems control for multiple low-speed peripherals. 1810 can control the following devices:

- High-speed paper tape.
- Card reader.
- Line printers.
- Magnetic tape.
- Graphic terminals.
- Communications.
- Line unit.
- Plotters.
- DAC packs.
- ADC packs.
- Bit packs.

The controller is mounted in the 1910 expansion rack. A 1810 long line adapter utilizes one of five universal controller positions in the central processor. It is a prerequisite for the first 1810.

The long line adapter is required to buffer and condition the I/O bus lines when signals are transmitted to external controllers. Signals can be transmitted up to 100 feet to a maximum of 64 controllers.

In addition to disc and magnetic tape units, PACER offers economical cartridge tapes as an external storage system. Each tape, depending on the number of interrecord gaps, holds from 90K words (40-word records) to 157K (1,000-word records) words. A cartridge contains two tapes; it is easily loaded and requires no takeup reels. A file protect switch provides manual lockout control.

Table 4 lists the characteristics of the low-speed and high-speed peripherals.

Special Peripherals

Table 5 summarizes the characteristics of the special DAC/ADC equipment applicable for data acquisition and industrial process control. This table also contains the characteristics of the data communications devices provided with the PACER. The 1414 Alphanumeric CRT and keyboard, the ASR and KSR Teletypes, and the 1620 Electrostatic printer are included in Table 4. These devices are utilized as communications terminals as well.

SOFTWARE

PACER users can avail themselves of four different software packages designed to provide the most effective use of a hardware configuration: PTS, the paper tape system; COS, the cartridge operating system; TOS, the magnetic tape operating system; and DOS, the magnetic disc operating system. All of these systems contain the same software packages except for PTS, which does not support a system monitor.

In addition, EAI offers the Real-Time Operating System (RTOS) for real-time foreground/background processing as an optional feature. RTOS costs $3,000 for the software and installation.

Table 6 lists the available software packages.

Operating Systems Monitor. This monitor provides automatic operating system functions for batch processing in the COS, TOS, and DOS software packages. A job stream is entered via TTY or punched cards. I/O directives and control directives are simplified and interpreted by the monitor to provide the required job or file function.

Languages

All of the languages support punched cards, paper tape, magnetic tape, disc, and communications.

Assembler. The assembler is two-pass and allows 91 mnemonics and 21 pseudo-operations. It provides a source listing, absolute/relocatable object code, a symbol table, and diagnostics.

Table 4. EAI PACER 100: Standard Peripherals

Device	Characteristics	Comments
LOW-SPEED PERIPHERALS		
Console		
Teletype		
1411	33 ASR; 10 cps	With paper tape
1413	35 ASR; 10 cps	With paper tape
1412	35 KSR; 10 cps	With keyboard only
CRT		
1414	A/N display; 10 cps with Teletype; 218 cps alone	64 ASCII char set; 6 x 9 inch CRT; 20 lines of 80 characters; can be used as system I/O device with Teletype or as remote terminal
Paper Tape		
Reader		
1430	300 cps	5-/7-/8-level code
Punch		
1440	120 cps	5-/7-/8-level code
Card Reader		
1500	300 cpm	Binary read; 400-card hopper/stacker
Line Printer		
1600	356 lpm; 800 char/line	64-char set; ASCII Code; top-of-form control; single line advance and perforation step-over
1611	245-1,110 lpm; 132 char/line	64 ASCII char set
1612	700 lpm; 132 char/line	6 lpi; paper tape loop format control
1614	1,200 lpm; 132 char/line	
1620	120 cps electrostatic; 80 char/line	Used with 1414 for hard copy; direct replacement for printer portion for ASR and KSR Teletypes
Plotters		
Model 130	300 increments/sec; 0.01-in. increment std; 0.005-in. optional; plotting area 11 inches by 144 feet	Require 1900 Interface
Model 140	450 increments/sec; 0.005-in. increment std; plotting area 11 inches by 144 feet	
Model 330	450/900 increments/sec; 0.005/0.0025-in. increment; plotting area, 34 inches by 120 feet; 1 pen std., 4 pens opt	—
Model 340	Same as Model 330; except plotting speed of 900/1,800 increments/sec	—

Table 4. (Contd.)

Device	Characteristics	Comments
HIGH-SPEED PERIPHERALS		
Magnetic Tape Cartridge 1700	4 tapes/unit in 2 cartridges; 10 ips; 900 bpi; 1.8-kb/sec transfer rate	Approx 90K words per 150-foot tape at 40 words per record
Standard 1712	9-track; IBM NRZI; 25 ips; 800 bpi; 20 kb/sec transfer rate	Uses 1713 transport; 1 included; 4 transports/controller
1724	9-track; IBM NRZI; 45 ips; 800 bpi; 36 kb/sec transfer rate	Uses 1734 transport; 1 included; 4 transports/controller
1726	9-track; IBM NRZI; 75 ips; 800 bpi; 60 kb/sec transfer rate	Uses 1736 transport; 1 included; 4 transports/controller
Magnetic Disc 1262	360,448 words/disc; 375-kb/sec transfer rate; avg access time, 17 msec	Uses 1260 Controller; 4 drives/controller; data stored on 64 tracks in 44-word sectors; 128 sectors/track

Fortran IV. An ASA Standard Fortran compiler provides a source listing, relocatable code, a symbol table, diagnostics, and a memory map.

PACER Fortran IV features a data type called scaled fraction that assumes all values are between ± 1. Scaled fraction quantities are more compact than floating-point quantities (one word versus two words) and are considerably faster in execution (5 to 6 times) than floating point. Hybrid problems are generally time-critical and do not require a high degree of accuracy. This facility makes EAI's Fortran, which also allows mixed-mode arithmetic, rather unique.

Hybrid Operations Interpreter (HOI). This interactive, algebraic interpreter was created specifically for scientists and engineers engaged in hybrid computation. The Digital Operations Interpreter (DOI), a subset of HOI, is similar to Fortran and allows linkage to Fortran subroutines. An internal program dump is available so that the user may retain hard copy documentation for reference.

Utilities

Text Editor. The text editor provides a total source program file maintenance capability. Commands can be issued via Teletype console, paper tape, or punched cards.

Oedipus. Oedipus is an interactive octal debugging aid with program and data file services. It includes multiple breakpoints, memory or register snapshots, and on-line patch facilities.

Loaders. A core image loader handles absolute code. A core image generator links multiple program segments into a single object file for subsequent loading by the core image loader. A linking loader is provided for immediate link load and execute.

Library. The Fortran Run Time Library provides mathematical functions, integration package subroutines, I/O drivers, and data conversion and formatting routines. More than 150 subroutines are available.

Table 5. EAI PACER 100: Special Peripherals

Device	Characteristics	Comments
SPECIAL PERIPHERALS		
Digital to Analog	10 bits; ±10V output; (8-, 10-, 12-bit resolution)	Provides 4 D/A converters output amplifiers
Analog to Digital		
Pack A	16 bits; ±10V input range	Autorange ADC and scanner for up to 64 channels, expandable to 1,024 channels
Pack B	12 bits; ±10V input range; conversion time, 20 msec	Single channel
Pack V	12 bits; 100,000 words/sec	High-speed ADC with multiplexor
Bit Pack		
Digital Input	16 bits; filtered input	Accommodates 16 interrupts, pulse or level
COMMUNICATIONS		
Graphic Display		
1414 Alpha CRT Terminal	218 char/sec; 6 x 9 inch display; 20 lines x 80 char	64 ASCII char set; can be used with Teletype or 1620 Printer for hard copy; Teletype reduces speed to 10 char/sec
1415 Graphic Display System	Full-duplex; 9,600-baud; 11-inch CRT; 7-bit + parity code; up to 1 hour storage time; 50 msec erase time	Graphic Display; 1,024 x 1,024 point matrix; A/N Display; 39 lines of 85 characters each; 1 line scratchpad
1416 Graphic Input Unit (expansion for P-415)	Excursions; side to side, 66° ±4°; corner to corner, 94° ±4°; digitize time 20 msec	Joystick; resolution within 1 point
1417 Hard-Copy Unit (expansion for P-415)	Copy time, 18 sec; copy size, 8-1/2 x 11 inches	Copies alphanumeric or graphic data stored on the display
1418 Analog Data Direct Display (expansion for P-415)	2.8 centimeters/sec drawing rate	Allows direct display of analog input; ±10V; full-scale; separate display and store modes
1420 Graphic Display System	11-inch storage tube; display area 7.5 x 5.6 inches; 9,600 baud rate; full duplex	ASCII code; 7 data bits + parity 63 printing char; 35 lines of 72 char each; vectors can be drawn between any two points
1421 Hard-Copy Unit (expansion for P-420)	Copy time, 18 sec; copy size, 8.5 x 11 inches; warmup time 20 min.	Copies alphanumeric or graphic data stored on 1420
1850 Communications Subcontroller	Provides control for up to 4 1885 Line Units; 1885 provides RS232C serial interface	Plugs into 1810 universal controller 1855 can be used with Data Modem, Teletype 33 or 35, 1414, and 1420

Table 6. EAI PACER 100: Software

Software Package	Configuration Required	Comments
Paper Tape System (PTS)	8K words of memory, Teletype ASR 33	Supports all systems software except the Systems Monitor
Operating Systems		
Cartridge (COS)	8K words of memory, Teletype ASR 33, and cartridge unit	Supports all systems software
Magnetic Tape (TOS)	8K words of memory, Teletype ASR 33, and magnetic tape unit with 2 or more transports	Supports all systems software
Disc (DOS)	8K words of memory, Teletype ASR 33, and disc unit with 1 or more drives	Supports all systems software
Real-Time (RTOS) — not included in systems software	16K words of memory, Teletype device, disc, and 1 other mass storage device (paper tape or tape cartridge)	Provides control for real-time, foreground/background processing with memory protection for all programs; supports all systems software
Operating Systems Monitor	Same as for the operating system	Provides automatic batch processing under control of directives from TTY or punched cards
Language Processors		
Symbolic Assembler	Same as for the operating system	Two-pass; manual and monitor control options; absolute or relocatable object code; supports extensive I/O features
Fortran IV	Same as for the operating system	ASA Fortran plus extended features; one-pass; relocatable
Hybrid Operations Interpreter (HOI)	Same as for the operating system	A hybrid on-line interactive language interpreter for checking hybrid equations output code
Digital Operations Interpreter (DOI), a subset of HOI	Same as for the operating system	Similar to Fortran; for preparation and execution of scientific problems; operates in big desk calculator or in stored program mode
Utilities		
Text Editor	Same as for the operating system	Provides for editing source files from mass storage device or paper tape; records can be deleted, altered, or replaced
Utilities Package	Same as for the operating system	Transfers files from any standard peripheral to another with automatic code conversion under on-line or off-line control
Oedipus	Same as for operating system	Compact, on-line, octal, interactive debugging aid
Loaders		
Core Image Loader	Same as for operating system	Operates under manual or monitor control
Core Image Generator	Same as for operating system	Translates absolute or relocatable object code from language processor to core image file under manual or monitor control
Library		
Fortran Run Time Library (RTL)	—	Includes mathematical functions, integration package subroutines, I/O drivers, data conversion and formatting routines, and I/O
I/O Subroutine Drivers	—	For all system devices including displays, plotters, and data communications
Numerical Integration Package (NIP)	—	Solutions for up to 60 ordinary linear differential equations using Runge-Kutta, Runge-Kutta-Mersen, and modified Euler algorithms
Diagnostics	—	Hardware checks for all system components
Applications	—	Hybrid applications software

Numerical Integration Package. This package solves up to 60 first-order, ordinary, linear differential equations. Single-precision, double-precision, and scaled fraction modes are provided with either Runge-Kutta, Runge-Kutta-Merson, or Euler algorithms.

Diagnostics. A comprehensive set of hardware check routines tests the arithmetic, control, and memory sections. All standard peripherals including communications, digital, and analog equipment are also tested.

Applications

EAI provides a function manipulation library as hybrid applications software. Included are: function generation of one, two, and three variables; function storage and playback for the solution of partial differential equations; and transport delay subroutines. In addition, hybrid debug and hybrid interface diagnostics are provided.

Real-Time Operating System (RTOS)

RTOS is a real-time multiprogramming system that supervises the running of real-time programs in the foreground concurrently with program development or batch processing in the background.

RTOS consists of the following major components:

- Real-Time Monitor (RTM).
- System support program.
- User programs.

RTOS partitions memory into three segments: one for the monitor, one for the foreground job, and one for the background job. The monitor swaps the background job out of core if a foreground job requires more than the allotted memory. Once the foreground job no longer requires additional memory, the background job is swapped back into core to continue processing.

RTM provides memory protection for all programs by means of the hardware base/limit register feature.

All system support and user programs are executed in the user mode; only RTM operates in monitor mode. All digital I/O for user programs must be performed through the system IOCS; a special class of hybrid I/O can be executed in user I/O mode.

RTM services all interrupts although user tasks can be assigned to timer and data channel interrupts by a Job Control Language (JCL) command or a trap function call at run time.

The RTM task scheduler assigns priority to each task of a user's job according to the user's specification at run time. The user can alter task priority dynamically.

User programs communicate with RTM by using the trap instruction, which places an eight-bit code in the accumulator and causes an interrupt. RTM decodes the byte in the accumulator to determine what service the user program requires.

RTOS will execute the following systems programs as foreground or background jobs as directed by JCL commands:

- Fortran IV compiler.
- Symbolic assembler.
- Hybrid Operations Interpreter.
- Digital Operations Interpreter.
- Core image generator.
- Oedipus.
- Text editor.

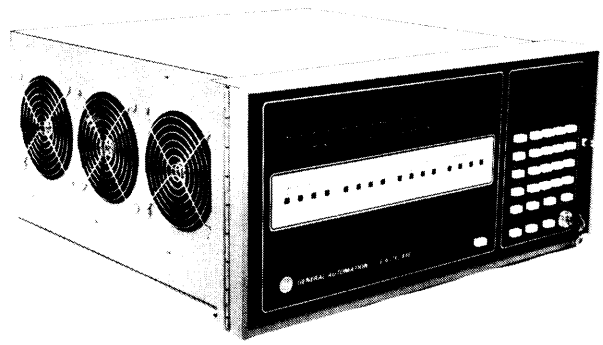
A disc file maintenance routine repacks the disc to reclaim deleted file space.

User jobs can consist of one task or a series of tasks. RTM suspends or aborts user programs when errors are detected.

A mini version of RTOS will be provided for systems dedicated to multitask foreground processing only. Mini RTOS consists of a task scheduler, IOCS, several Teletype commands, and a clock handling routine. It requires only 3K words of memory for its use.

GENERAL AUTOMATION

GA-16 Series



GA-16/440 Computer

OVERVIEW

The GA-16 Series consists of four microprogrammed, compatible computer systems — GA-16/110, 220, 330, and 440 — developed for the OEM market and for incorporation into systems currently designed around the SPC-16. The GA-16 Series is program compatible with the SPC-16 and surrounds it in power and performance. The low end of the GA-16 Series falls below the SPC-16 and the top end above it. The GA-16/330 is most comparable to the SPC-16/40 while the GA-16/440 is more powerful than either the SPC-16/60 or SPC-16/80.

The big news about the GA-16 Series is the same kind of good news users have been getting from other manufacturers: bigger memories, smaller size, lower cost, COBOL, and a more sophisticated operating system. Soon, the only thing mini about minicomputers will be the physical word length, cost, and physical size. Table 1 lists the GA-16 Series mainframe characteristics.

The GA-16/110, 220, and 330 all use the same microprocessor, implemented using LSI nMOS technology. The GA-16/440 uses a different microprogrammable processor implemented with MSI bipolar technology using tri-state Shottky logic. The 110 and 220 use the same nMOS RAM memory while the 330 and 440 currently use core memory. The nMOS RAM modules are available in three kinds of 4K- and 8K-word modules: without parity, with one parity bit per byte, or with six Error-Detection and Recovery (EDR) bits.

The GA-16/110 is mounted on a single board (7¾ by 11 inches) that contains Control Read-Only Memory (CROM), Register Arithmetic and Logic Unit (RALU), and 1K RAM. Separate boards are used for 4K or 8K words of nMOS RAM, Memory Parity and Protect (MPP) option, plug-in system power supply, and plug-in auxiliary power supply for memory retention in case of power shutdown or loss. Memory can consist of RAM, ROM, and PROM. It can range from 512 bytes of RAM to 64K bytes. ROM and PROM are piggyback modules that fit on a RAM module; thus all systems must have some RAM.

The 220 CPU uses two boards: one for the CROM and one for the RALU. The 220 memory is the same as that used for the GA-16/110. The GA-16/220 has all the features of the GA-16/110 with the following additional features:

- Microconsole ROM.
- TTY Controller and Serial I/O Port.
- SPC-16 DMA channel.

Although the GA-16/330 uses the same microprocessor and is available as a board-only system like the 110 and 220, it is also packaged as a complete, freestanding computing system like the 440. Also like the 440, the 330 is configured with core memory, which has a cycle time of 720 nanoseconds. Core is available with or without byte parity. The 330 is offered in three kinds of standard configurations: CPU and memory on a board, packaged without power, or fully packaged. Memory ranges from 8K to 64K bytes.

The 440 is a fully packaged system. The 440 configured with a memory management unit can support up to 2M bytes of core memory.

The basic instruction set for all four systems is completely compatible with the SPC-16. Only the GA-16/110 does not have the SPC-16 compatible DMA channel. The basic instruction set includes unsigned integer multiply/divide. An optional high-speed arithmetic unit can provide

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HEADQUARTERS

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Table 1. GA-16 Series: Mainframe Characteristics

CENTRAL PROCESSOR[1]	GA-16/110	GA-16/220	GA-16/330	GA-16/440
Technology	LSI nMOS	LSI nMOS	LSI nMOS	MSI bipolar & tri-state Shottky
Microprogrammed	Yes	Yes	Yes	Yes
Control Memory	CROM	CROM	CROM	MSI bipolar
No. of Registers	16	16	16	16
Word Length, bits	16/16 + 2 parity/16 + 6 EDR	16/16 + 2 parity/16 + 6 EDR	16/16 + 2 parity	16/16 + 2 parity
Addressing, bytes				
Direct/Indirect/Indexed	32K/64K	32K/64K	32K/64K	32K/64K
Mapping	128K	128K	128K	2M
Instruction Set				
Implementation	Firmware	Firmware	Firmware	Firmware
Types	Singleword	Singleword	Singleword	Singleword/Doubleword
Number	91+	91+	91+	91+
Floating-Point	Opt	Opt	Opt	Opt
Hardware Stacks	Opt	Opt	Opt	Yes
Instruction Execution Times, μsec				
Fixed-Point[2]				
Add/Subtract	5.0	5.0	4.5	1.6
Multiply[3]	23.5	23.5	21.2	11.9
Divide[3]	22.5	22.5	20.3	13.6
Floating-Point[4]				
Add/Subtract	Opt	Opt	Opt	3.1-4.7
Multiply				4.8-7.9
Divide				7.6-8.7
Writable Control Store	No	No	CROM	ROM/PROM
Interrupts				
Levels	64 std; unlimited, opt	64 std; unlimited, opt	64 std; unlimited, opt	64 std; unlimited, opt
Type[5]	NI, stack,I/O, external	NI, stack, I/O, external	NI, stack, I/O, external	NI, stack, I/O, external
MAIN STORAGE				
Type	nMOS/bipolar RAM/PROM/ROM[6]	nMOS/bipolar RAM/PROM/ROM[6]	Core	Core
Cycle Time, μsec	.300	.300	0.720	0.720
Basic Addressable Unit	Word/byte	Word/byte	Word/byte/bit	Word, double-word/ byte/bit
Bytes/Access	2	2	2	2
Cache Memory	No	No	No	No
Capacity, bytes				
Min	256 (RAM) + 1.5 ROM	8K	32K	32K
Max	128K	128K	128K	2M
Increment Size, bytes	8K/16K	8K/16K	32K	32K
Ports/Module	1		1	1
Error Checks	Parity, opt/EDR, opt	Parity, opt/EDR, opt	Parity, opt	Parity, opt
Memory Protection	Opt	Opt	Opt	Opt
Memory Management	No	No	No	MMS
Interleaving	No	No	No	No
INPUT/OUTPUT				
Max Devices Addressable	64	64	64	64
Programmed I/O, bytes/sec	240K	240K	240K	240K
DMA	Yes	Yes	Yes	Yes
DMA xfer rate, bytes/sec	2M	2M	2M	2.2M
PRICE of System with No Memory	1,920	2,305	–	–
32K-byte Memory	3,045	3,435	5,250	11,800
64K-byte Memory	5,525	5,915	8,250	75,150

Notes:
(1) GA-16/110, 220, and 330 use same microprocessor.
(2) Single Precision – one word.
(3) Unsigned; signed multiply/divide optional.
(4) Floating-point operations are via a separate processor.
(5) NI= interrupts that can't be inhibited; stack = stack underflow or overflow; I/O = equals real-time clock, TTY not busy, or console interrupt; external = peripheral device interrupts.
(6) Some RAM required; ROM and PROM are piggyback modules on RAM.

signed multiply/divide. A separate floating-point processor that connects to the system via the I/O bus is also optional for all systems.

Currently, operating systems for the new GA-16 Series consist of the SPC-16 operating systems upgraded to handle new features of the GA-16; the new Control IV operating system is for the GA-16/440 only.

Control I — DBOS (Disc-Based Operating System).
Control II — RTX (Real-Time Executive).
Control III — RTOS (Real-Time Operating System).
Control IV — RTMS (Real-Time Multiprogramming System) with memory management for up to 2M bytes of memory.

The GA-16/110 can support Control II, which is designed for real-time dedicated applications. The GA-16/220 and 330 can support Control I, II, and III. The GA-16/440 can support Control I, II, III, and IV. COBOL is now available to run under all program-preparation operating systems: Control I, III, and IV.

Quantity discounts for the new systems are the same as those that have been available for the SPC-16.

Deliveries for the GA-16/440 began in June. Over 100 have already been produced, and General Automation is in full production of 440 Systems. The GA-16/110 is scheduled for delivery in December 1975. The GA-16/220 and 330 are scheduled for delivery in January 1976.

The nMOS LSI semiconductor chips for the GA-16/110/220/330 are made by Synertek.

Competitive Position

The GA-16 Series, called the Solution Series, is an important system for General Automation. It includes replacements for the LSI-16, which was designed around Sapphire On Silicon (SOS) technology, as well as expansion for the SPC-16 line. The LSI-16 was withdrawn from the market early this year because low yields prevented its production at a competitive price. General Automation was probably ahead of competitive SOS technology by one or two years. The GA-16 uses the popular LSI nMOS technology for the 110, 220, and 330, and MSI bipolar technology for the 440. If GA's earlier gamble with SOS had succeeded, however, the company would be hailed today as innovative and creative. Instead, the company suffered financial losses and reverberations at high management levels. The company has traditionally provided solutions rather than hardware, and it has been especially strong in the automotive industry, which also suffered last year. In the past few years, the company has diversified into data management and real-time systems and into the OEM market. A General Automation spokesman earlier stated that the SOS experience was not a total waste because it gave the company experience in designing a system around semiconductor technology. The GA-16 reflects that experience.

As shown in Tables 2 and 3, the models in the GA-16 Series are price/performance competitive with similar products from other manufacturers. The GA-16/110 and 220 will meet the Computer Automation LSI 3/05 as well as the Naked Minis and the Digital LSI-11 in the market place. The GA-16/220 will also compete with the Digital PDP-11/05.

The GA-16/330 competes with new Data General Nova 3, Digital PDP-11/40, Interdata 7/16, and small configurations of Hewlett-Packard HP 21MX. The GA-16/440 will have many competitors: Digital PDP-11/45, Data General ECLIPSE and Nova 830, Hewlett-Packard HP 21MX, Computer Automation Megabyter, Modular Computer Modcomp II, and Varian Data V70 Series.

Table 2 shows how very competitive comparable systems are, differing only by about $40 in price. The systems shown in Table 3 vary more in price, but much of the variation is represented by built-in features in one system that

Table 2. GA-16/110 and 220 Compared With Some Competitors

	Computer Automation LSI-3/05	GA-16/110	Digital LSI-11	GA-16/220
Word Length, bits	16	16/16 + 2 parity/ 16 + 6 EDR	16	16/16 + 2 parity/ 16 + 6 EDR
Inst. Times, μsec				
Add	6.0	2.5	3.5-12.0	2.5
Multiply	No	21.0	24-64	21.0
Divide	No	20.0	78	20.0
Fl.-P. Add	No	Opt	42.0	Opt
Fl.-P. Multiply	No	Opt	52-92	Opt
Fl.-P. Divide	No	Opt	151	Opt
Max Memory, Bytes	32K	128K	64K	128K
No. of G.P. Registers	8	16	8	16
Max DMA Rate, bytes/sec	1.7M	2M	1.7M	2M
Price, $				
CPU + Memory				
8K bytes	1,145	1,185	1,536	1,575
32K bytes	2,650	3,045	3,411	3,435
64K bytes	—	5,525	5,911	5,915
128K bytes	—	10,485	—	10,875

Table 3. GA-16/330 and 440 Compared With Some Competitors

	Data General Nova 3	GA-16/330	Digital PDP-11/45(2)	GA-16/440	HP 21MX
Word Length, bits	16	16/16 + 2 parity	16/16 + 2 parity	16/16 + 2 parity	16
Inst. Times, μsec					
Add	1.8	4.6	1.8	0.8	1.9
Multiply	6.9(1)	21.2	4.7	11.1	12.8
Divide	7.5(1)	20.3	8.6	12.8	17.0
Fl.-P. Add	7.7*	*	6.5*	3.1-4.7*	22-54*
Fl.-P. Multiply	11.3*	*	8.2*	4.8-7.9*	48-57*
Fl.-P. Divide	13.7*	*	9.9*	7.6-8.7*	41-76*
Max Memory, bytes	64K/256K	128K	253,952	2M	512K
No. of G.P. Registers	4	16	16	16	4
Max DMA rate, bytes/sec	2M	2M	2M	2M	1.2M
Price, $					
CPU + Memory					
32K bytes	4,400	5,250	23,900	11,800	7,650
64K bytes	7,100	8,250	32,000	15,150	11,800
256K bytes	34,200	–	55,500(3)	38,750	36,150
512K bytes	–	–	–	71,850	–

*Optional, at extra cost.
Notes:
(1) Operands are unsigned integers on std.
(2) Core memory assumed, the PDP-11/45 can use faster MOS or bipolar memory.
(3) Maximum memory is 253,952 bytes.

can be stripped out of another. Which system is the greater bargain depends on a user's specific configuration and software needs.

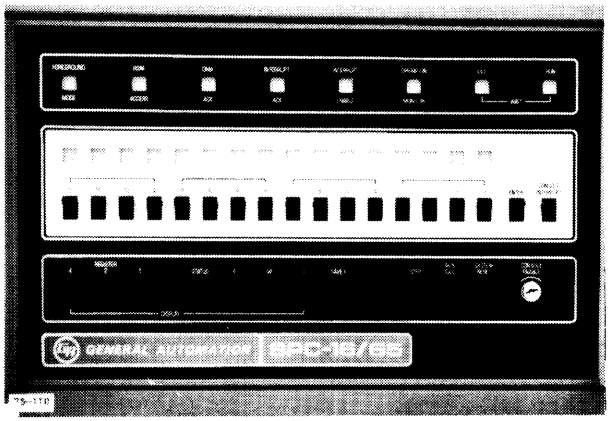
The Solution Series has been well-planned. Although it contains no radical departures from the SPC-16, it does provide more performance at a lower cost, and enlarges the market GA can now compete in.

PRICE DATA

Equipment	Purchase Price $
GA-16/110	1,185
1 Board,CPU	585
4K wds RAM	620
Packaged W/O Memory	1,920
GA-16/220	1,595
2 Boards, CPU	975
4K wds RAM	620
Packaged W/O Memory	2,305

GA-16/330 CPU Board With Core Memory	Board Only $	Packaged W/O Power $	Fully Packaged $
4K wds	3,250	4,150	4,450
8K wds	3,650	4,450	4,950
16K wds	3,950	4,950	5,250
32K wds	6,950	7,450	8,250

GA-16/440	W/O MMS 16 bits $	W/MMS 18 bits $
Basic System With Core Memory		
16K wds	8,950	11,800
32K wds	11,950	15,150
64K wds	17,950	21,850
Core Memory Only		
64K wds of 18-bit core for expansion	16,900	
Floating Point Processor	5,000	
High-Speed Arithmetic	1,500	



OVERVIEW

General Automation introduced the SPC-16 Series as the "super performance" 16-bit industrial automation computers in its family of fourth-generation equipment. Featuring three models that differ only in core speed — 800, 960, or 1,440-nanosecond cycle time per 16-bit word — the company offers each model "bare-bones" OEM (SPC 16/45, 16/65, 16/85) or packaged (SPC 16/40, 16/60, 16/80) with a full set of features for real-time applications. Each SPC-16 model is a dual-speed computer in that its read/write core memories are interchangeable with faster read-only memories operating at 400, 480, and 720-nanosecond cycle time per word, respectively. Construction features multilayer printed circuit boards, medium-scale integrated circuits, and an operating environment of 0°C to 50°C with up to 90 percent relative humidity.

The SPC-16 mainframe characteristics are listed in Table 1.

General Automation recently announced its DM 100 Series, SPC-16/65-based systems. The DM 120 operates as a remote job entry (RJE) workstation that can communicate with other DM 100s or IBM Systems 360/370s. The DM 130 is a data base management system that operates in a multiprogramming/multitasking environment. It can support up to four CRT workstations or perform batch compilations or communications in background. A DM 130/2 is a dedicated small business computer available from a distributor network on a turnkey basis. The DM 140, the most powerful system in the series, can support up to 32 remote CRT workstations in the foreground concurrently with background batch compilations or communications.

Table 1. General Automation SPC-16 Series: Mainframe Characteristics

CHARACTERISTICS	SPC-16 Series
CENTRAL PROCESSOR	
No. of Internal Registers	8 std; 8 opt
Addressing Direct (no. of words)	32K
Indirect	32K
Indexed	32K
With Paging	128K
Instruction Set Number	78 std; 5 opt
Decimal Arithmetic	No
Floating-Point Arithmetic	Opt
Priority Interrupt Levels	64
MAIN STORAGE	
Type	Core
Cycle Time (msec)	1.44; 0.960; 0.800 (1)
Basic Addressable Unit	Word, byte, bit
Bytes per Access	2
Min Capacity (bytes)	8K
Max Capacity (bytes)	64K; 256K (2)
Increment Size (bytes)	4K, 8K, 16K
Parity	No
Protect	Opt
ROM	
Use	Program and/or loaders
Capacity (bytes)	32K
I/O CHANNELS	
Programmed I/O	Yes
DMA Channels (no.)	Opt (8)
Multiplexed I/O	No
Max Transfer Rate (words/sec)	
Within Memory	173K; 260K; 320K
Over DMA	700K; 1,040K; 1,250K

(1) Cycle times determine whether model number is 40/45, 60/65, or 80/85 respectively.
(2) The first number refers to Models 40, 60, and 80, while the second refers to 4 , 65, and 85.

COMPETITIVE POSITION

In the past two years GA has been expanding its markets by adding sales and service offices in the United States and abroad and by providing better terms for OEM users. With an installed base of over 1,000 minicomputers, a substantial amount of system software, new compatible systems to effect cost performance savings, and its edge in the end-user market, GA is a strong competitor.

To encourage OEM users, General Automation rents SPC-16 systems to potential OEM customers while they are designing their systems. OEM users can pass on their leftover warranty time to their customers. In addition, the period for counting time under quantity discount

contracts does not begin until the OEM user makes the first delivery. Quantity discounts of up to 40 percent are available.

GA stresses its strong systems engineering and applications expertise in the face of its competition.

General Automation is apparently going the same system route as other minicomputer manufacturers. Its new DM-100 Series systems (based on SPC-16/65), parallel the M230, M260, and S250 data management systems offered by Hewlett-Packard. Its DM-130/2, offered as a turnkey system via a distributor network, follows the same route Microdata has taken with its Reality system.

In addition, GA is offering a DM-200 Series of systems, functionally similar to the DM 100 Series, but based on the GA-18/30 computer, which has been sold as an IBM System 1130 upgrade since 1968. These systems will also emphasize data management functions, but they are oriented toward industrial applications. The 1130 upgrade system, now called the 230/2, will be distributed on a turnkey basis like the 130/2.

These systems will compete with the small business computers offered by the large mainframe manufacturers, as well as those offered by other minicomputer manufacturers.

USER REACTIONS

The SPC-16 users we interviewed were using their systems for a wide variety of applications. A large petroleum manufacturer was using a SPC-16 for high-speed data acquisition of seismologic data used in petroleum exploration — the system had discs magnetic tapes, and punched I/O cards and tape as well as plotters. A manufacturer of discs, tapes, and punched tape peripherals has several operating in engineering and testing applications (using their own peripherals). An OEM manufacturer uses dual processors to run a Telex switching system it markets. Another user had two SPC-16s operating online to IBM System 360/65s (special interface) to run an automated warehouse. A branch of a large western university uses a processor with multiplexor as a front end for 20 terminals communicating with a Burroughs 1700; another college was using it as an RJE terminal for an IBM System 370/165.

Users bought their systems for a variety of reasons related to their applications, but one common reason noted by several was the ease of programming. Several users (one of the colleges, the OEM manufacturer, and the petroleum company) were doing their own programming even at the systems level and found the instruction set well suited to their needs. The college found it ideal for communications; the petroleum company believed the Operate On Memory feature on the DMA channel was unique at the time it purchased its systems.

Table 2. General Automation SPC-16 Series: Peripherals

Peripheral Device	Description
MAGNETIC TAPE	
3331, 3332, 3333 Magnetic Tape Subsystems	9-track; 25, 37.5, 75 ips; 800 bpi; 20K, 30K, 60K bytes/sec; 2,400-ft reel
3334, 3335, 3336 Magnetic Tape Subsystems	7-track; 25, 37.5, 75 ips; either 556/800 or 200/556 bpi; 2,400-ft reels; master unit includes 1 drive, can handle 3 more slave drives
FIXED-HEAD DISCS	
3342 Head/Track Storage Drive and Controller	128K or 256K-word capacity; access time 8.5 msec; transfer rate 2 MHz; requires 2 subunit slots
MOVABLE HEAD DISCS	
3341 Disc Storage System	Capacity 3.2M wds/drive; 10 disc surfaces; seek time, 10-65 msec; avg latency 12.5 msec; master unit has 1 drive; can control up to 3 more slave drives
3343 Disc Storage Subsystem	Capacity 12.8M wds/drive; 20 surfaces; seek time, 10-65 msec; avg latency, 12.5 msec; peak transfer rate; same configuration and submodels as 3341
3346 Disc Storage System	Capacity 2.5M wds/drive; 4 surfaces; seek time 14-85 msec; latency 20 msec; one fixed and 1 removable disc
3347 Disc Storage Subsystem	Capacity 1.25M wds/drive; 2 surfaces; seek time 14-85 msec; latency 20 msec; one fixed and 1 movable disc
3349 Floppy Disc Subsystem	Capacity 147K wds/drive; 288 wds/sector, 8 sectors/trk, 64 tracks
CONSOLE TYPEWRITERS	
3362 Teletype Model ASR 33	10 cps; includes pt read/punch
3363 Teletype Model ASR 35	10 cps; includes pt read/punch uses no subunit slot
PAPER TAPE	
3321 Paper Tape Reader and Controller	8-channel tape; 400 cps
3322 Paper Tape Punch and Controller	8-channel tape; 75 cps
3323 Paper Tape Reader/Punch and Controller	Combines 3321 and 3322; requires 2 slots
3325 Paper Tape Reader/Punch and Controller	8-channel tape; 300-cps reader; 75-cps punch; fan fold option; requires 1 subunit slot
PUNCH CARD (std 80-col card)	
3315 Card Reader and Controller	300 cpm; light duty

Table 2. (Contd.)

Peripheral Device	Description
PUNCH CARD (std 80-col card) (Contd.)	
3316, 17, 18 Card Reader and Controller	400, 600, 1,000 cpm; heavy duty
3314 Card Punch and Controller	35 cpm; includes keyboard
LINE PRINTERS	
3353 Line Printer and Controller	Up to 132 cols/line, 600-lpm; ASCII code
3357 Line Printer/Card Reader and Controller	Printer: 132 cols, 600 lpm; reader; 80-col cards, 400-cpm
3354-1000 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 7 x 8 dot matrix, 6 lpi; 125 lpm; card reader 300, 400, 600, 1,000 cpm
3354-1200 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 5 x 7 dot matrix, 6-8 lpi, 200 lpm; card reader, 300, 400, 600, 1,000 cpm
3355 Line Printer/Card Reader and Controller	600-lpm printer, 132 cols; 1,000-cpm card reader (80 cols); print 6-8 lpi option
3358 Line Printer/Card Reader and Controller	600-lpm printer, 132 cols; 6-8 lpi 300-cpm card reader (80 cols)
A/D & D/A Available	
DATA COMMUNICATIONS	
1561 Asynchronous Communication Controller	For RS232-compatible data set (Bell 103 and 102); full-duplex; 75 to 2,400 bps rates available; 1, 2, or 4 lines
1571 Synchronous Communication Controller	For Bell 201 or equivalent data set; double-buffered, full-duplex; external timing permits wide range of data rates
1581 Series Asynchronous Communications Controller	Interface for full-duplex lines; std rates are same as 1561; 1, 2, or 4 lines
1567 Automatic Calling Unit Subsystem	Provides interface for 4 automatic calling units
1590 Communication Multiplexor Common Equipment	Double-buffered, full-duplex interface for async lines; same baud rates as 1581; up to 16 or 32 lines

CONFIGURATION GUIDE

All processors can address up to 64 peripheral device controllers. Table 2 lists the available peripherals.

Software packages available for the SPC-16 and the configurations they require are listed in Table 3.

Table 3. General Automation SPC-16 Series: Software

Model No.	Characteristics	Comments
BSP-16	Basic systems program package	Minimum configuration: CPU, 4K-word memory and Teletype
FSOS-16	Freestanding operating system, job-oriented, tape supported	Minimum system: CPU, 8K-word memory; HSPTR/CR, TTY
RTX-16	Real-time executive, runs under FSOS-16 or DBOS-II	CPU, 8K words of memory, TTY
DBOS-II	Disc-based operating system	CPU, 16K words of memory, disc, TTY
RTOS-II	Real-time operating system; multiprogramming, foreground/background	CPU, 24K words of memory, disc, TTY
CAP-16	Basic assembler	CPU, 4K words of memory, TTY
CAP-16M	Macro assembler	CPU, 8K words of memory, TTY
FORTRAN IV Compiler	Extended ANSI specifications; real-time compiler with code optimization	CPU, 12K words of memory, TTY
Commercial FORTRAN Compiler	FORTRAN with COBOL-like extensions, string manipulation	CPU, 12K words of memory, TTY
BASIC Interpreter for FSOS, DBOS, and RTOS	Single-user conversational language, or multiple users, real-time conversational mode	Dedicated CPU; 8K, 16K, and 24K words of memory, respectively; disc and TTY

COMPATIBILITY

The SPC-16 Series computers are all compatible. Programs developed for one system can run on another, except in rare instances where the cycle time is used in some way by the program. The SPC-16 is not program compatible with either the SPC-12 family or the GA 18/30.

MAINTENANCE

General Automation maintains its own systems out of its 25 sales and service offices in the United States.

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TYPICAL PRICES

Model Number	Description	Purchase Price $	Monthly Maint. $
	CENTRAL PROCESSORS AND WORKING STORAGE(1)		
1640-1101 1640-1102	SPC-16/40 Processor (4K 16-bit words of core memory expandable to 16K in chassis; 17 hardware registers including 8 programmable; real-time clock; operations monitor alarm; power fail/auto restart interrupts; system console panel; system console TTY controller; I/O bus port with logic for programmed I/O; unlimited priority interrupts; DMA port with arithmetic and logical functions for opt 0.694-mHz data channel; enclosure; cooling unit and 47-63 Hz power supply; processor cycle time, 1.4μ sec)	5,550	60
1640-1202	SPC-16/40 Processor (same as 16/40-1101 except 8K words of core memory, expandable to 32K in chassis; uses 4K, 8K and 16K boards, but only one 4K board/processor)	6,950	70
1640-1203	SPC-16/40 General-Purpose Computer-8K	6,000	70
1640-1304	SPC-16/40 Processor (same as 1640-1202 except has 16K words of core memory)	8,950	82
1640-1305	SPC-16/40 General-Purpose Computer-16K	6,950	82
1640-1306	SPC-16/40 Processor (same as 1640-1202 except has 24K core memory)	10,450	122
1640-1308	SPC-16/40 Processor (same as 1640-1202 except has 32K core memory)	11,450	134
1640-1309	Same as 1640-1305 except has 32K of memory	9,950	134
1660-1101	SPC-16/60 Processor (same as SPC-16/40 except can accept opt 1.04-mHz data chan; memory cycle time is 960 nsec)	6,550	60
1660-1102	SPC-16/60 General-Purpose Computer-4K	6,050	60
1660-1202	SPC-16/60 Processor (same as 16/60-1101 except 8K words of core memory, expandable to 32K in chassis; uses 4K and 8K boards, but only one 4K/processor)	7,950	70
1660-1203	SPC-16/60 General-Purpose Computer-8K	6,400	70
1660-1305	SPC-16/60 General-Purpose Computer-16K	7,250	82
1660-1309	SPC-16/60 General-Purpose Computer-32K	10,250	134
1680-1101	SPC-16/80 Processor (same as SPC-16/40 except can accept opt 1.25-mHz data chan; processor cycle time is 800 nsec)	8,550	70
1680-1102	SPC-16/80 General-Purpose Computer-4K	8,550	70
1680-1202	SPC-16/80 Processor (same as 16/80-1101 except has 8K words of core memory, expandable to 32K in chassis; uses 4K and 8K boards, but only one 4K/processor)	10,150	85
1680-1203	SPC-16/80 General-Purpose Computer-8K	9,050	80
1680-1305	SPC-1680 General-Purpose Computer-16K	12,550	92
1680-1309	Same as 1680-1305 except with 32K of memory	19,550	141
1645-1101	SPC-16/45 Processor (4K words of core memory expandable to 16K in chassis, 32K in chassis with memory expansion board, or 64K with memory expansion chassis; 17 hardware registers including 8 general-purpose; I/O bus port with logic for programmed I/O; unlimited priority interrupts; DMA port with arithmetic and logical functions for opt 0.694-mHz data chan; power failure memory protection; visual real-time debug aid; enclosure; cooling unit and 47-63 Hz power supply; processor cycle time, 1.4μ sec)	3,950	55
1645-1102	SPC-16/45 General-Purpose Computer-4K	5,100	60
1645-1202	SPC-16/45 Processor (same as 16/45-1101 except 8K words of core memory expandable to 64K in chassis)	5,350	70
1645-1203	SPC-16/45 General-Purpose Computer-8K	5,550	70
1645-1304	SPC-16/45 Processor (same as 1645-1201 except has 16K memory)	7,350	82
1645-1305	SPC-16/45 General-Purpose Computer-16K	6,500	82
1645-1306	SPC-16/45 Processor (same as 1645-1201 except has 24K memory)	8,850	122
1645-1308	SPC-16/45 Processor (same as 1645-1201 except has 32K memory	9,850	134
1645-1309	SPC-16/45 General-Purpose Computer-32K	9,500	134
1645-1412	SPC-16/45 with 4K words of 16-bit core using 3 16K-word memory boards (includes memory expansion chassis, memory location display board, power and cables. Expansion to 64K requires additional memory location display board	14,150	196
1645-1413	SPC-16/45 General-Purpose Computer with 64K Memory Expansion Module	14,250	196
1645-1416	Same as 1645-1412 except with 64K-words of memory, using 4 16K-word memory boards	16,650	253
1645-1417	Same as 1645-1413 except with 64K of memory	17,250	253
1645-1512	Same as 1645-1412 except with 128K-word memory expansion module (allows additional of up to 128K words of memory using either 8K- or 16K-word memory boards)	15,050	219
1645-1516	Same as 1645-1512 except with 64K-word memory using 4 16K-word boards	17,550	271
1645-1520	Same as 1645-1512 except with 80K-word memory using 5 16K-word boards	20,050	323
1645-1524	Same as 1645-1512 except with 96K-word memory using 6 16K-word boards	22,550	375
1645-1528	Same as 1645-1512 except with 112K-word memory using 7 16K-word boards	25,050	427
1645-1532	Same as 1645-1512 except with 128K-word memory, using 8 16K-word boards	27,550	479
1665-1101	SPC-16/65 Processor (same as SPC-16/45 except can accept opt 1.04-mHz data chan; processor cycle time is 960 nsec)	4,950	55
1665-1102	SPC-16/65 General-Purpose Computer-4K	5,600	60
1665-1202	SPC-16/65 Processor (same as 16/65-1101 except has 8K words of 16-bit core memory, expandable to 64K in chassis)	6,350	70
1665-1203	SPC-16/65 General-Purpose Computer-8K	5,950	70
1665-1305	SPC-16/65 General-Purpose Computer-16K	6,800	82
1665-1309	SPC-16/65 General-Purpose Computer-32K	9,800	134
1665-1413	SPC-16/65 General-Purpose Computer with 64K Memory Expansion Module -48K	14,550	196
1665-1417	SPC-16/65 General-Purpose Computer -64K	17,550	253
1685-1101	SPC-16/85 Processor (same as SPC-16/45 except can accept opt 1.25-mHz data channel; processor cycle time is 800 nsec)	6,950	65
1685-1102	SPC-16/85 General-Purpose Computer -4K	8,100	70
1685-1202	SPC-16/85 Processor (same as 16/85-1100 except has 8K words of core memory, expandable to 64K in chassis)	8,550	90
1685-1203	SPC-16/85 General-Purpose Computer-8K	8,600	80
1685-1305	SPC-16/85 General-Purpose Computer-16K	12,100	92
1685-1309	SPC-16/85 General-Purpose Computer-32K	19,100	144
1685-1413	SPC-16/85 General-Purpose Computer with 64K Memory Expansion Module -48K; 800 ns memory cycle time; contains 49,152 words of 16-bit core memory. 1.25 MHz data channel and 115 VAC, 47-63 Hz. Product includes computer, memory expansion chassis, 2 memory location display boards and necessary power and cables.	27,850	206

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
1685-1417	SPC-16/85 General-Purpose Computer-64K (same as 1685-1413 except with 64K of memory)	34,850	263
	Additional 4K-Word Memory Modules[2]		
16XX-0100	1,440 nsec (for SPC-16/40 or /45)	2,600	26
16XX-0100	960 nsec (for SPC-16/60 or /85)	2,800	26
16XX-0100	800 nsec (for SPC-16/80 or 85)	3,000	30
	Additional 8K-Word Memory Modules		
16XX-0200	1,440 nsec (for SPC-16/40 of/45)	4,000	40
16XX-0200	960 nsec (for SPC-16/60 or/65)	4,200	40
16XX-0200	900 nsec (for SPC-16/8000/185)	4,600	46/45
	Additional 16K- and 128K-word memory modules		
1640-0400	1440 nsec (not for models 1640-1159/2159)	4,600	60
	Processor Options[2]		
16XX-0002	Foreground/Background Processing	250	—
16XX-0004	Extended Processor Option (adds hardware mult/div and foreground/background capability)	500	7
16XX-0015	I/O Enclosure Expansion	N/C	—
16XX-0090	Memory Protect	250	—
16XX-0016	Hardware High-Speed Multiply/Divide (mounts in 2 slots of 1615-1101 I/O expansion chassis)	1,500	16
16XX-0080-0088	Initial Program load (32-wd; semiconductor ROM programmed to load from high speed paper tape reader; TTY; card reader; disc; floppy disc and head-per-track disc)	NC	—
16XX-0070-0077	Initial Program load (64-wd; semiconductor ROM programmed to load from disc; card reader; high-speed paper tape; TTY; floppy disc)	NC	—
	Processor Options (for SPC-16/45, 65, 85 only)[2]		
16XX-0050	Programmer's Console	550	5
16XX-0001	System Console Teletype Controller (for use with ASR 33 or 35)	250	2
16XX-0008	Real-Time Failsafe Group (real-time clock; operations monitor alarm; system safe line; power fail/auto restart interrupts)	350	5
16XX-0095	Memory Expansion Chassis (control logic for addressing 48K words; can expand memory from 32K to 64K words for — 1200/ — 1300 models; 1645 uses 8K or 16K boards; 1665/1685 use 8K boards)	1,300	10
16XX-0096	Memory Location Display Board (control logic for addressing 48K to 64K words; for systems using 8K boards only)	500	5
	I/O Expansion Options		
1615-X101*	I/O Expansion Chassis (provides chassis, power I/O cable and cable interface card for 19 I/O subunits)	1,200	20
1615-1102/2102	I/O Expansion Chassis 2 (same as 1615-1101/2101 except has unterminated CIT)	1,200	20
1615-0202	Cable Interface Driver (CID; for I/O Expansion on SPC-16/40, 60, 80 processors)	450	20
1615-0203	Cable Interface Translator (signal and control translator within I/O Expansion Chassis; required for I/O Expansion Chassis)	310	10
1615-0208	Multiple High-Speed Data Channel	600	7
1615-0209	Multiple High-Speed Data Channel (8 channels; 16/40/60/80/prereq)	500	7
1615-0210	Computer to Computer Interface (CCIF) (up to 4 computers may be interfaced; 1615-020X prereq)	1,750	30
1615-0211/0212/0213/0214	CCIF Interface Panels (for 16/40/45; 1615-0210 and system enclosure prereq)	310	0
1615-0220	Arithmetic Processing Unit (double precision floating point and integer operations; 1615 expansion chassis-prereq)	5,000	65
1615-1230/1231	Auto Bus Transfer Unit — CIT Unterminated/CIT Terminated	6,000	34
1960-7000	CCIF Interconnection Cable 10 ft	190	0
1960-7001	CCIF Interconnection Cable 25 ft	250	0
1960-7999	CCIF Interconnection Cable, customer specifies length	150 + $4/ft over 10 ft.	0
	MASS STORAGE		
	IBM 2311 Equivalent Disc Drive		
3341-1000	Drive and Controller for up to 4 drives (3.2M 16-bit words; 45-msec avg access time; includes disc pack)[3]	19,500	125
3341-X110*	Additional Disc Drive	13,500	75
3341-6200	Disc Controller	6,000	NC
	Head-per-Track Disc Drive		
3342-1142-1242	Drive and Controller (128K 16-bit words; 8.5-msec avg access time)[3]	8,000	60
3342-1144-1244	Drive and Controller (256K 16-bit words; 8.5 msec avg access time)[3]	9,300	65
3342-1246	Same as 3342-1242 except 512K words storage	11,500	70
3342-6200	Disc Controller	3,000	NC
3343-1000/1001	Drive and Controller (up to 4 drives per controller; random and sequential access: 12.8M 16-bit words; 45-msec avg access time; includes disc pack)[3]	24,500	175
3343-1110/1111	Additional Disc Drive for 3343-1000/1001	15,500	100
3343-6200	Disc Controller	9,000	NC
	1 Fixed, 1 Removable Pack Disc Drive		
3346-1000	Drive and Controller (up to 4 drives per controller; 2.5M 16-bit words; 60-msec avg access time)[3]	11,000	115
3346-1110	Additional Disc Drive	7,000	100
3346-6200	Disc Controller	4,000	NC
	Floppy Disc Drive		
3349-1000	Drive and Controller (up to 4 drives/controller; capacity of 144K words, 16-bit words; access time 10 ms; includes 1 floppy disc cartridge)	3,750	31

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
3349-1110	Disc Drive (includes 1 floppy disc cartridge)	1,250	16
3349-1220	Mounting Hardware and Power Supply (115 vac, 60 Hz)	500	8
3349-6200	Controller (will handle up to 4 disc drives)	2,500	15
	INPUT/OUTPUT		
	System Console Teletype		
3362-1000/ 1001	ASR 33 (60 Hz/50 Hz; 115 vac)	1,250	35
3363-1000	ASR 35 (60 Hz; 115 vac)	4,500	62
3363-2000	ASR 35 (50 Hz; 220 vac)	4,600	62
	Unidirectional Reader (8-chan paper tape; 400 cps)		
3321-6200	Controller	1,100	NC
3321-1000	Reader and Controller (4)	2,500	18
3322-1000	Punch and Controller (4)	3,000	25
3322-1010	Punch and Controller (with fanfold release and takeup bins) (4)	3,200	25
	Reader/Punch		
3323-1000	Reader/Punch and Controller	5,000	40
	Punched Card (std 80-col cards; heavy duty; 1615-0209 prereq)		
3316-1000	Reader and Controller (400 cpm)	4,500	35
3318-1000	Reader and Controller (1,000 cpm)	7,000	45
3314-1000	Punch and Controller (with interpreter and keyboard)(3)	11,000	110
	Line Printer (600 lpm; up to 132 col)		
3353-1000	Printer and Controller (uses ASCII code)	13,900	110
3353-1001	Line Printer and Controller (with 6/8 lpi option)	14,500	110
3354-1203	Line Printer/Card Reader (200-lpm; printer; up to 132 col; 300-cpm, 80-col reader)	10,400	85
3354-1206	Line Printer/Card Reader (same as 3354-1203 except has 600-cpm reader)	12,400	95
3354-1209	Line Printer/Card Reader (same as 3354-1203 except has 1,000-cpm reader)	13,200	100
3355-1000	Line Printer/Card Reader and Controller (600-lpm printer, up to 132-col and 1,000-cpm reader, 80 col)	19,100	150
3355-1001	Line Printer/Card Reader and Controller (same as 3355-1000 except has 6/8-lpi option)	19,700	150
3356-1001	Line Printer/Card Reader and Controller (same as 3356-1000 except has 6/8-lpi option)	18,900	145
3357-1000	Line Printer/Card Reader (600-lpm printer, 400-cpm reader)	17,000	140
3358-1000	Line Printer/Card Reader and Controller (600-lpm printer, 300-cpm card reader)	16,400	135
3355/3356/ 3357/3358- 6200	Line Printer/Card Reader Controller	3,000	NC
3331-1011	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 25 ips)	10,000	100
3331-6201	MTT Controller (25 ips; will handle up to 4 transports)	4,000	NC
3332-1011	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 37.5 ips)	11,000	100
3333-1011	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 75 ips)	14,000	150
3333-1120	Mag Tape Transport (Add-On) (75 ips)	10,000	125
3334-1002	Mag Tape Transport and Controller: (controller will handle up to 4 transports; 1 transport included; 7-track 25 ips, 556/800 bpi)	10,000	100
3334-6201	MTT Controller (25 ips; will handle up to 4 transports)	4,000	NC
3335-1002	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 37.5 ips)	11,000	100
3335-1112	Mag Tape Transport (Add-On) (37.5 ips)	7,000	75
3335-6201	MTT Controller (37.5 ips; will handle up to 4 transports)	4,000	NC
3336-1002	Mag Tape Transport and Controller (controller will handle 4 transports; 1 transport included; 75 ips)	14,000	150
3336-1112	Mag Tape Transport (Add-On) (75 ips)	10,000	125
3336-6201	MTT Controller (75 ips; will handle 4 transports)	4,000	NC
3371-1001/ 1002/1003	Plotter and Controller (Drum type incremental plotter, 0.01 inch/step; 0.005 inch/step or 0.1 MM/ step; 11 inch carriage)	7,400	60
3372-1001/ 1002/1003	Plotter and Controller (29.5-inch carriage, 1- or 0.005-inch/step or 0.1 MM/step; includes basic plot package)	10,900	65
3374-1000	Plotter and Controller (34-inch drum; 3 programmable pens; 2,000 steps/sec; .002-inch/step)	16,400	115
3380-1110	A/N Display (RS232; 115 VAC; 60 Hz; split screen with foreground/background intensity control and full editing capability; 1,998-char set; 27 lines; 74 col/line)	3,300	36
	DATA COMMUNICATIONS		
	Async Controller		
1561-0X01	Async Communication Controller, RS232 (provides 1 double-buffered, full-duplex line between an SPC-16/40/45 series computer and an RS232-compatible async data set)	700	5
1561-0X02	Async Communication Controller, RS232 (provides 2 double-buffered, full-duplex lines)	1,000	7
1561-0X04	Async Communication Controller, RS232 (provides 4 double-buffered, full-duplex lines)	1,500	12
1571-0001	Sync Communication Controller, RS232 (provides 1 double-buffered, full-duplex line)	700	7
1571-0101	Sync Communications Controller, RS232 with Transmit Clock Capability	800	7
1567-0004	Automatic Calling Unit Controller	900	9
1581-0X01	Async Communications Controller, Current Loop	600	6
1581-0X04	Async Communications Controller, Current Loop (same as 1581-0X02 except for 4 full-duplex lines)	1,225	8
1581-2X02	Async Communications controller, Current Loop (same as 1581-2X01 except for 2 full-duplex lines)	775	6
1581-2X04	Async Communications Controller, Current Loop (for 4 full-duplex lines)	1,325	6
1581-3X01	Async Communications Controller, Current Loop, 60 ma (provides interface with limiting resistors for 1 full-duplex line; permits program selection of the number of stop bits, char size, and baud rate; standard baud rates provided are: 75, 110, 134.5, 150, 300, 600, 1,200, 9,600 baud; requires external power)	600	6

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
1581-3X02	Async Communications Controller, Current Loop, 60 ma (provides interface with limiting resistors for 2 full-duplex lines; permits program selection of the number of stop bits, char size, and baud rate; standard baud rates provided are: 75, 110, 134.5, 150, 300, 600, 1,200, and 9,600 baud; provides external power)	725	6
1581-3X04	Async Communications Controller, Current Loop, 60 ma (provides interface with limiting resistors for 4 full-duplex lines; permits program selection of the number of stop bits, char size, and baud rate; standard baud rates provided are: 75, 110, 134.5, 150, 300, 600, 1,200, and 9,600 baud; requires external power; includes loop back test)	1,225	8
	Communication Multiplexor Equipment		
1530-1000/ 1001	DMA Async Communications Multiplexor	5,500	35
1590-1X00	Communication Multiplexor Common Equipment 16 Lines, 115 VAC	3,475	32
1590-1X01	Communications Multiplexor Common Equipment, 32 Lines, 115 VAC	4,000	35
1591-0004	Line Adapter, RS232C Modem Interface	500	6
1592-0004	Line Adapter, Current Loop, 20 ma	400	6

Notes:

NC No Charge — Not Applicable
*X = 2 for 220-vac, 50-Hz operation, otherwise X = 1.

1. Processors, most processor options, and controllers for peripheral devices are discountable. RPQ from manufacturer; not available for rental from manufacturer.
2. XX = SPC-16 Series processor Models 40, 60, 80, 65, or 85, unless stated otherwise.
3. Requires 1615-0209 High-Speed Data Channel.
4. Requires 1615-X101* for use with SPC-16/45, 65, 85 processors.

OVERVIEW

The General Automation 18/30 Industrial Supervisory System is an 18-bit (16 bits plus parity and protect bits) minicomputer aimed at the same markets as IBM's 1130 and 1800 systems, particularly the former. The General Automation (GA) computer features an instruction set that is compatible with both the 1130 and 1800: the 18/30 has 32 basic instructions, whereas the 1130 has 29; the 1800 has 31. The GA processor implements most of the features found on the IBM 1800, but it is aimed more at the 1130 market because the 1800 installations tend to be more customized and hence, more difficult to replace.

Both of the well-established 18/30 configurations are disc-based systems. DMS-1 (formerly Mini DMS) uses a small 512K-word fixed disc while DMS-2 (formerly Super DMS) uses large 2311- or 2314-type disc pack drives. The company recently announced two new operating systems called CMS Foreground/Background Communication System and DPS Data Entry System. A remote job entry system was announced at the same time. Earlier operating systems, such as TSS (Time-sharing), RTMS (Realtime), RTX (Realtime), and DBOS (Disc) are no longer supported.

GA's peripheral line includes magnetic tape transports, paper tape and punched card I/O devices, printers, plotters, communication devices, analog/digital subsystems, and discs. The product line is nearly as extensive as IBM's and some GA 18/30 devices are faster than those available for the 1130 and/or the 1800. (The 1130 is essentially a limited version of the 1800.) The GA 18/30 is almost equivalent to an 1800 with greater peripheral capabilities, thus, moving from an IBM 1130 to a GA 18/30 upgrades the system and reduces costs. About 500 GA 18/30 systems have been installed.

The 18/30 is marketed as a supervisory system related to other GA products for industrial control as well as for an 1130 replacement system. The company aims its products at three levels of control. The LSI-12/16 "microcomputer" and the older SPC-12 series complement each other at the lowest level, controlling one or many machines performing the same functions. The LSI-12/16 is usually a component and must be ordered in quantities of 100 or more; the SPC-12 is better characterized as a controller (frequently freestanding) that can be bought in smaller quantities. The members of the SPC-16 product line are more powerful foreground/background processors and can control a number of real-time jobs in the foreground with simultaneous batch program development in the background. The 18/30, with its totally different IBM 1130/1800-compatible instruction set, is a supervisory system that monitors and controls a variety of manufacturing processes, frequently via communication with the LSI-12/16, SPC/12, and SPC-16 computers. The four systems are compared in Table 1. The LSI-12/16 impacts (and extends) the bottom of the SPC-12 market and the SPC-16 competes at the top, thus the SPC-12 is being pushed into the background although it is still supported.

General Automation markets its minicomputer systems through its 25 direct sales offices in the United States and Canada. Its subsidiaries also market systems directly in Belgium, England, France, Switzerland, Italy, and West Germany. It has a manufacturing facility in West Germany and sales offices in four cities. European headquarters for the company are in France. GA also has distribution agreements with Standard Telephone and Cables in Australia, Koyo International in Japan, Hwa Sheng Electronic Company in Taiwan, and Industrial Electronic Instruments in India.

PERFORMANCE AND COMPETITIVE ANALYSIS

The GA 18/30 is currently marketed both as an IBM 1130-replacement system and as part of a total system at the highest level of control in industrial and process control applications.

The IBM 1130 and 1800 as well as other replacement systems are particular competitors of the 18/30. The Digital Scientific Meta 4 System competes in this regard; it is a microprogrammed computer that uses a ROM for 1130/1800 emulation. Both GA and Digital Scientific supply faster throughput by using a faster cycle time and equivalent or faster peripheral devices. GA is a much larger company than Digital Scientific. Some of the characteristics of the four systems are compared in Table 2.

As a supervisory system for process control, the 18/30 competes generally with manufacturers dedicated to process control applications like Leeds and Northrup, Westinghouse, and General Electric. The 18/30 also competes with manufacturers such as IBM and Honeywell who can set up combinations like the IBM 1130 with System 7 and the Honeywell 16 Series with GE-PAC systems. For some applications the 18/30 competes with a large number of systems that can do analyses of process, engineering, and manufacturing inputs, such as the PDP-11, Data General 840, Sigma 3, and many others.

The recent introduction of two new operating systems and a remote job entry package gives a positive marketing thrust to the 18/30 complementing GA's lower level SPC-16 and the LSI-12/16 systems. The CMS foreground/background communication operating system, in particular, should enhance the 18/30's capabilities as an industrial supervisory system.

Applications for the 18/30 cover a variety of industries and businesses. In manufacturing, the system is suitable for control and monitoring of production machines, control of high-speed packaging, shop floor data control, and industrial testing. In the automotive industry, where GA has a substantial installed base, the 18/30 can be used for production testing analysis of internal combustion engines and exhaust emission. In the electronics industry, it can be used for peripherals testing, electronic

Table 1. A Comparison of Specifications of General Automation Computers

MODEL NUMBER	SPC-12	LSI-12/16	SPC-16	18/30
CENTRAL PROCESSOR				
No. of Programmable Registers	7	7	8 std; 8 opt	15
Addressing (no. of words)				
Direct	4K	4K	32K	32K
Indirect	16K	32K	32K	32K
Indexed	16K	32K	32K	32K
With Paging	—	—	64K	—
Instruction Set				
Number (std; opt)	52	52	78;5	32(2)
Decimal Arithmetic	No	No	No	No
Floating Point	Subroutine	Subroutine	Opt	Subroutine
Priority Interrupt Levels	1-64	1-64	64	8-61
MAIN STORAGE				
Type	Core	Semiconductor	Core	Core
Cycle Time (μ sec)	2.16	2.64	1.44; 0.960; 0.800(1)	0.960
Basic Addressable Units	8-bit word, 16-bit doubleword	8-bit word 16-bit doubleword	Word, byte, bit	Word
Bytes per Access	1	1	2	2
Min Capacity (bytes)	4K	1K	8K	16K
Max Capacity (bytes)	16K	32K	128K	64K
Increment Sizes (bytes)	4K;8K	1K;2K;4K;8K	8K	8K
Parity	No	No	No	Std
Protect	Opt	Opt	Opt	Std
ROM	Yes	Yes	Yes	No
Use	Bootstrap	Program and/ or Loaders; PROM patching	Program and/or Loaders	—
Capacity (wds)	64	8K	128K	—
I/O CHANNELS				
Programmed I/O	Yes	Yes	Yes	Yes
DMA Channels (No.)	Opt	No	Opt(8)	5
Multiplexed I/O	No	No	No	No
Max Transfer (wds/sec)				
Within Memory (K bytes)	460	375	173;260; 320(1)	260
Over DMA (K bytes)	460	—	700; 1,040; 1,250(1)	833

(1) Submodels 40(45), 60(65), and 80(85) respectively.
(2) Additional instruction forms for double precision.

testing, testing and analysis of circuits, and controlling production of PC boards and coil windings. The 18/30 can also automate warehousing and material handling systems, operate steel furnaces, and test product tensile strength. Laboratory/medical applications include physiological monitoring, spectrometer operation, gas chromatograph control, and amino-acid analysis. The chemical industry can use the system to analyze problems in ammonia and ethylene processing, plastic production, and processing dyes. Communication uses include telemetry data acquisition, automatic control of audio/visual processes in broadcasting, education, television, and synchronous data exchange. Petroleum, transportation, banking, printing, and retail industries also use the 18/30 in a variety of applications.

User Reactions

A western engineering firm replaced its 1130 with the GA 18/30 after also considering an IBM System/3. The computer was used mainly for analyses and modeling of engineering processes; it used card reader input and

Table 2. Differences among GA, IBM, and Digital Scientific Computers

Model	GA 18/30	D.S. Meta 4	IBM 1130	IBM 1800
CENTRAL PROCESSOR				
No. of Instructions	32	44	29	31
No. of General-Purpose Registers	2	Up to 28	2	2
No. of Index Registers	3	Up to 28	3	3
Real-Time Clock	Yes	Yes	No	Yes
I/O				
Programmed I/O	Yes	Yes	Yes	Yes
DMA (no. of channels)	5 std	9	5 std	3 std, 6 opt
MEMORY				
Cycle Times (μ sec)	0.96	0.90	2.2;3.6	2.0; 4.0
Bits per Cycle				
Data	16	16	16	16
Parity	Std	Std	Opt	Std
Protect	Std	Std	None	Std
ROM	None	1K-4K wds	None	None
Max Core Size (wds)	32K	64K	32K	64K
PERIPHERALS				
Max Speed for				
Card Reader (cpm)	1,000	1,000	1,000	400
Line Printer (lpm)	600	600	600	600
Mag Tape Drive (ips)	75	37.5	None	2400 std feature
Disc Subsystem Capacity (wds/drive)	512K;2.5M;10M	512K	512K	512K; 2.5M
Access Time (msec)	45	160	750	75

printer output. The GA system was chosen primarily because it was cost-effective. It had a competitive edge over an XDS System and IBM's System/3 because it did not have conversion problems. The GA 18/30 and DS Meta 4 were close contenders. The 18/30 was chosen partly because of GA's size and apparent financial stability. The user felt he would get better service from GA than from DS. He is pleased with the way the system has worked out; he has experienced no compatibility problems.

A western engineering and landscaping firm bought the 18/30 when they found it was cheaper to buy the system than to rent it. When the money had been allotted for a system, the data processing manager checked around for alternatives, but decided on an 18/30. He considered Meta 4 but mistrusted their policy of custom interfacing any type of peripheral—he felt this might cause more problems than those encountered by a company with a standard peripheral line. He also believed that General Automation's software was superior. If anything, this user's GA 18/30 system has exceeded expectations; conversion was smooth and easy and the throughput is even more than the hardware speeds indicate. This user now has a 32K-word system with two 2314-type discs, tape drive, card reader, and printer. He has joined in forming a users' group (GUAGE) that is useful and active; GUAGE is not particularly dominated by General Automation.

Another 18/30 user is a southern firm that does a lot of work in civil engineering and construction; this company bought the system for much the same reasons as the western engineering firm. This firm had been a member of CEPA, an 1130 civil engineering users' group, and discovered that IBM had around 6,000 1130 systems world-wide but, as the 1130 was approaching the end of its useful life, IBM would not provide a replacement system for it or a system for users to move up to. This user was very happy with the 18/30 and said it was "a terrific system." General Automation, moreover, is giving the system full support and is continuing to expand its capabilities.

CONFIGURATION GUIDE

The center of an 18/30 system is the 1804 processor, marketed in several standard configurations. All include 8K words of core with both parity and memory protect, hardware multiply/divide, double precision arithmetic, high-speed scratchpad memory, 16 programmable registers, operator's console, power supply, enclosures, and cooling unit. The 1804 processor has five automatic data channels (DMA), eight priority interrupts, automatic power shutdown/restart, parallel teletypewriter controller, memory parity and storage protect interrupts, operations monitor, three system timers, system safe and reset signals, and parallel data channel with line drivers and receivers. The 1804 is available with 8K, 16K, and

32K words of memory. Memory can be added to a system in 4K-word modules, up to the maximum of 32K words.

The basic interrupt system can be expanded in increments of eight levels, up to a total of 59 external interrupt levels. Each level can connect to 16 devices, allowing for a maximum of 944 peripheral devices. Peripherals include discs, magnetic tape drives, teletypewriters, printers, card and paper tape readers and punches, plotters, digital and analog I/O subsystems, and communication data set controllers. GA will sell the "minicontroller" alone if a user wants to interface his own peripherals.

Two hardware/software "package" configurations are offered: the DMS-1 and DMS-2. Both use the DMS software as their basic operating system; DMS-2 can also use the Real-time Multiprogramming System. Both systems are disc-based systems with a master disc drive included in the package price. The standard DMS-1 disc is a cartridge drive, while DMS-2 uses a 2311-type master. Both masters can be expanded with added slave drives. Also included are a card reader and line printer, console typewriter/keyboard, and the system enclosure. Card reader speed is 300 cards per minute for DMS-1 and 600 cards per minute for DMS-2. Printer speeds are 125 lines per minute for DMS-1 and 600 lines per minute for DMS-2. Higher-speed card readers and printers can be substituted for the standard items for an additional charge; DMS-2 can also be specified with a 2314-type (10M words) disc. Some peripherals are restricted to either "package" or "unpackaged" systems—the 125 line-per-minute printer and the cartridge disc are found only on DMS-1, for example, but most peripherals can be attached to all systems.

COMPATIBILITY

The 18/30 is compatible with IBM's 1130 and 1800 computers at the machine instruction level. Several of the older operating systems corresponded enough to IBM operating systems to provide compatible operating environments. The TSS Time Shared Supervisory system runs programs executable under IBM's 1800 TSX system; DMS runs programs executable under the IBM 1130 DM2 after local generation. DMS is currently supported; TSS is not. The 18/30 is not meant to be plug-compatible in the sense that it can interface directly to IBM peripherals. A number of GA's peripherals are faster than those allowed by IBM for its 1130 and 1800. This is one of the attractions of the system for users who want to upgrade an 1130 or 1830 installation.

MAINFRAME

Central Processor

The DMS-1, DMS-2, CMS, and DPS configurations are all variations built around a single processor, the Model 1804. The DMS configurations include built-in discs and various slow-speed peripherals combined into a single package with the appropriate software. The DMS-1 system parallels some of the IBM 1130 systems with built-in discs; DMS-2 expands on the 1130 system by including much larger discs.

The 18/30 CPU is constructed of small- and medium-scale integrated circuits; unlike the LSI-12/16 and SPC-16, the 18/30 is not a microprogrammed system.

Data Structures. The basic 18/30 unit of data is the 16-bit data word with one parity and one protect bit appended. Fixed-point binary arithmetic is performed in two's complement form. Floating-point operations are performed by subroutines. Instructions can be one or two words long. Table 3 lists the formats.

Registers. One 16-bit register (A) serves as an accumulator for single-precision arithmetic; a 16-bit extension register (X) is used with the accumulator for double-precision arithmetic and extended shifts. The 18/30 also has 3 index registers, XR1, XR2, and XR3; they can be used as base registers for single-word instructions or for address modification of doubleword instructions. Sets of five channel address registers (CAR 1 through CAR 5) and scan control registers (SCR 1 through SCR 5) are associated with the five DMA channels, one register pair per channel. The accumulators, index registers, and DMA registers are all programmable.

Four other registers are used during the execution of most instructions, but are not directly programmable. The memory location register (L) contains the source or destination memory location associated with an instruction or data being stored or fetched. The operation register (O) contains the instruction currently being executed. The memory data register (M), which uses 18 bits instead of the 16-bit length of all the rest, transfers data and instructions in and out of memory.

Two 1-bit registers, carry and overflow, are associated with the accumulator. These two special registers can be programmed or "set."

Table 3. General Automation 18/30: Data Structures

Data Name	Representation
Character	6 or 8 bits
Byte	8 bits
Halfword	8 bits
Word	16 data bits + parity + protect
Word (double length)	32 bits
Instruction	16 or 32 bits
Binary Operand	16 or 32 bits
Floating-Point Operand (short)	2 words (8-bit exponent, 23-bit fraction, 1 sign bit)
Floating-Point Operand (long)	3 words (8-bit exponent), 31-bit fraction, 1 sign (8 unused bits)

Instruction Set. The 18/30 instruction set consists of 32 basic instructions; some are further subdivided for a total of 68 instructions; over 400 modifications are possible. Arithmetic, logical, load and store instructions operate on both single and double precision operands. Almost all instructions, regardless of precision, can be implemented by a singleword or a doubleword format, controlled by a flag in the first instruction word. Doubleword instructions allow indirect and indexed addressing. The 18/30 has three basic register/register instructions not used on the 1130, two are used on the 1800; one is unique to the 18/30. Because the 18/30 cycle time is 960 nanoseconds, its instruction execution times are generally faster than those for either IBM system. Table 4 lists typical instruction execution times.

Table 4. General Automation 18/30: Typical Instruction Execution Times

Instruction Groups	No. of Instructions	Typical Execution Times (μ sec) (1)
ARITHMETIC/LOGICAL		
Add/Subtract (single)	2	2.4
Add/Subtract (double)	2	3.6
Floating Add	Subroutine	200.0
Multiply	1	12.0
Floating Multiply	Subroutine	350.0
Divide	1	13.2
Floating Divide	Subroutine	350.0
Logical	3	2.4
LOAD/STORE		
Single	6	2.4
Double	2	3.6
SKIP/BRANCH/SHIFT		
Skip	17(2)	1.20-1.32
Branch	15(2)	1.32-2.40
Shift	7	1.2 + 1.2 (N/4) (3)
Register Transfer	4	2.4
I/O & CONTROL		
I/O Transfer	8(2)	4.8(4)
DMA Transfer	2(2)	1.2(4)
Control	2	1.2

Notes:

(1) Add 1.2 μ sec for each level of indirect addressing.

(2) Number includes all variations of basic instructions as if each were a separate instruction.

(3) N/4 means number of shifts divided by 4, rounded off to next highest integer.

(4) Maximum access on highest priority channel is 1.32 μ sec.

Addressing. The singleword instruction uses base-relative addressing; the displacement field in the instruction word is added to one of the four registers that can be specified to generate the address. The doubleword format has a 16-bit address field, thus it can directly address all 32K words of memory (actually 64K words are logically possible). In addition, one level of indirect addressing and indexing can be specified in this format. If both indexed and indirect addressing are specified in the same instruction, indexing is performed before indirect addressing. Indirect addressing adds 1.2 microseconds to the instruction execution time; indexing adds no time.

Input/Output Control

Two types of I/O channels are standard on the 18/30, a parallel data channel and a set of five automatic data channels. Both channels are controlled by a single multipurpose instruction, Execute I/O (XIO). Two subinstructions are used for internal control, Sense and Control. Sense reads a device status word into the accumulator, and Control changes the operating condition of a device or feature. The Read and Write subinstructions transfer one word between an I/O device and memory via the parallel data channel. The Initialize Read and Initialize Write subinstructions set up the conditions to transfer a block of data between memory and a DMA device via the automatic data channels. The device controller performs the actual transfers, which proceed on a cycle stealing basis.

All five DMA channels can operate concurrently. Although I/O devices can be connected to any channel, devices that need to operate simultaneously must be assigned to separate channels. When more than one channel requests service at the same time, requests are serviced on the basis of channel priority with channel one having the highest priority. Maximum access time for channel one is 1.36 microseconds; maximum access time for channel five with all other channels operating is 21 microseconds.

All DMA block transfer operations are controlled by I/O tables in memory. When a series of blocks is transferred, the tables are chained together by the last entry in the table for the current block. Two registers are associated with each direct memory data channel, the channel address register and the scan control register. The channel address register contains the starting address of the data to be transferred, and the scan control register contains the number of data words to be transferred. Each DMA channel has a separate interrupt.

Interrupt Control. The basic system has one internal, one trace, and six external interrupt levels. Groups of eight external levels can be added up to a maximum of 59 levels. One device is usually assigned to each level, but up to 16 devices can connect to one interrupt level, thus the system can conceivably handle up to 944 devices.

All interrupt levels are assigned on a priority basis with the internal interrupts having the highest priority. External interrupts are assigned priority in accordance with user requirements.

Upon initiation of an interrupt, the contents of the instruction register are automatically saved in a preassigned location. The interrupt routine must save all pertinent registers and data, and restore this information upon completion of the interrupt.

When the external priority interrupt and relative time clock interrupt occur simultaneously, the relative time clock interrupt has priority. The automatic restart interrupt is standard and is activated by the automatic restart feature of the computer during a power-on sequence. Standard priority interrupts can also be controlled by the program through selective masking.

MAIN MEMORY

Working storage consists of magnetic cores with a cycle time of 960 nanoseconds per 18-bit word (16 bits plus parity and protect bits). Both DMS systems have standard configurations with 8K, 16K, and 32K words. All systems can be expanded to a maximum of 32K words in 4K-word increments. All basic memory sizes use circular (wraparound) addressing so that the address following the highest address is always 0000.

The memory parity bit is set for odd parity (including the storage protection bit) each time a word is written into memory, and it is checked each time a word is read out of memory. Protection is set on a word-by-word basis.

PERIPHERALS

Currently, peripherals include low-speed devices such as Teletypes, printers, and card and paper tape I/O (Table 5); disc and magnetic tape mass storage devices (Table 6); and special systems such as plotters and analog/digital I/O (Table 7). The device characteristics are summarized in Tables 5, 6, and 7. In addition to the controller/peripheral combinations listed, GA will supply the controller only if the user supplies the peripheral.

DATA COMMUNICATIONS

Communications equipment consists only of a series of Bell modem controllers and a universal interface. Specifications for these devices are presented in Table 8.

Table 5. General Automation 18/30: Low-Speed Peripherals

Device	Characteristics	Comments
1362 Teletypes	ASR 33, with controller; half- or full-duplex	Requires 1810-0202 for up to 4 TTYs and 1 or 2 slots
1363 Teletypes	ASR 35 with controller; half- or full-duplex	Requires 1810-0202 for up to 4 TTYs and 1 or 2 slots
PRINTERS		
1353 Line Printer	600 lpm; 132 cols; ASCII code; integral controller	Requires 2 slots
1361 Selectric Keyboard/Printer	15 cps; integral controller	Requires 2 slots
PUNCH CARD		
1311, 16, 17, 18 Readers	300, 1400, 600, 1,000 cpm, 80 cols, integral controller	Requires 1 slot
1313 Punch	100 cpm, 80 cols, integral controller	Requires 2 slots
71-121B Punch	35 cpm, 80 cols, integral controller; can be off-line keypunch/verifier	—
PAPER TAPE		
1321 Reader	400 cps, fanfold or reel, integral controller	Requires 1 slot
1322 Punch	75 cps, fanfold or reel, integral controller	Requires 1 slot

Table 6. General Automation 18/30: Mass Storage Peripherals

Device	Characteristics	Comments
DISCS		
1341 Disc Subsystem	2311-equivalent; 2.5M-wd capacity per drive, 45 μsec avg access, controller and 1 drive	Requires 5 slots, can control up to 4 drives Can attach 3 slaves
1343 Disc Subsystem	2314-equivalent; 10M-wd capacity per drive; 45 μsec avg access; controller and 1 drive	Requires 8 slots; can control up to 4 drives
1344 Disc Storage	512K-wd capacity, 1st drive included with processor	Can control up to 4 drives
MAGNETIC TAPE		
1331, 1332, 1333 Subsystems	9-trk, 800 bpi, 25, 37.5, 75 ips, 20, 30, 60 kb/sec; 2,400-ft reel; drive with controller	Requires 6 slots; can control 2 drives
1334, 1335, 1336 Subsystems	7-trk; 25, 37.5, 75 ips; 2,400-ft reel; drive with controller; 200/556/800 bpi	Requires 6 slots; can control 2 drives

SOFTWARE

The 18/30 currently operates under a Disc Monitor System (DMS). Two new operating systems, a Communications Monitor (CMS) and a Data Entry System have recently been announced. Formerly, GA supported the Real Time Multiprogramming System (RTMS-18), now superseded by CMS. The real-time executive (RTX-18) and its related RTOS-18 operating system, disc-based operating system (DB-S), and Time-Shared Supervisory (TSS) System have all been superseded. Table 9 presents the configuration requirements for the current operating systems.

Operating Systems

DMS. DMS is a disc-oriented batch processing system that can support most system peripherals except the analog/digital I/O. It is compatible with IBM's 1130 DM2, allowing programs executable on the 1130 to run after local generation. DMS uses a-roll-in/roll-out feature to handle real-time situations, and it permits segmenting of large programs. GA claims that DMS users gain at least twice the processing speed and about 15 times the throughput at half the cost of equivalent 1130 systems.

Language Processors

GA offers three different versions of the symbolic assembler, depending on the configuration required, as outlined in Table 9. The assembler is compatible with both the IBM 1130 and 1800 assemblers.

Fortran. The Fortran compiler is an ANSI Fortran IV compiler with extensions for commercial processing.

Other Software

Important utilities include a generalized utility system for operating a freestanding limited system and for debugging: core image converter, DMS/BSC communications package subroutine library, and test and verify programs. An 1130/Loader Executive permits loading and execution of programs generated on an IBM 1130.

Table 7. General Automation 18/30: Special Peripherals

Device	Characteristics	Comments
PLOTTERS		
1371 Drum Plotter	CalComp 565; 300 steps/sec; 11-in. drum; 0.010 or 0.005 in. or 0.100 mm step	Requires 1 slot
1372 Drum Plotter	CalComp 563; 28-in. drum; 0.120 or 0.005 in. or 0.100 mm step; 200, 300 steps/sec	Requires 1 slot
DIGITAL I/O		
1411 Digital Differential Input	Interface and addressing for 16 digital inputs; accepts up to 32 vdc max	Requires 1810-200 and 1 slot
1412 Buffered Bipolar Power Drive	Interface and addressing for 16 power drivers; outputs for synchronizing with external equipment; rated at 40 vdc, 125 ma	Requires 1810-200 and 1 slot
1413 Generalized Input Buffer	16-bit input register	Requires 1 slot
1414 Generalized Output Buffer	16-bit output register	Requires 1 slot
1431 Digital Input Relay Receiver	Interface and addressing for 16 inputs	Requires 1810-200 and 1 slot
1432 Buffered Contact Output	Interface and address for 16 Form-A contact outputs; outputs for synchronizing external equipment; rated at 50 rdc, 500 ma, 25 vac max	Requires 1810-200 and 1 slot
ANALOG I/O		
1441 Analog I/O Unit	12-bit, 0 to + 5V ADC/DAC; 3.3 μsec/bit conversion rate	Requires 2 slots
1451 High-Level Single-Ended Input MUX	0 to + 5V	Requires 1441 and 1 slot
1452 High-Level Differential Input MUX	8 channels analog input, 0 to + 5V, 2V common mode	Requires 1441 and 1 slot
1453 Low-Level Differential Input MUX	8 channels analog input 0 to +200 mv, 2V common mode	Requires 1441 and 1 slot
1481 Analog Output Holding Amplifier	8 channels, + 5V output, droop 5 mv/sec @ 25 degrees C	Requires 1441 and 1 slot

Table 8. General Automation 18/30: Data Communications Peripherals

Device	Characteristics	Comments
1541 Data Set Controller	103A2 and 801ACU; half- or full-duplex	Requires 1810-0200 and 2 or 3 slots
1542 Data Set Controller	202C2 and 801 ACU; half- or full-duplex	Requires 1810-0200 and 2 or 3 slots
1551 Data Set Controller	103A2 only; half- or full-duplex	Requires 1810-0200 and 2 or 3 slots
1552 Data Set Controller	202C2 only; half-or full-duplex	Requires 1810-02200 and 2 or 3 slots
-112B	Half-Duplex	Requires 2 slots
-122B	Full-duplex	Requires 3 slots
1553 Data Set Controller	201B1; 4-wire; 2,400 baud max; synch; half- or full-duplex	Requires 1810-0200 and 1 or 2 slots
1920-6000 Universal Interface	For up to 40 dual in-line 16-pin ICS	Requires 1 or 2 slots

Table 9. General Automation 18/30: Software

Package	Characteristics	Comments
OPERATING SYSTEMS		
CMS Communications Monitor System	Real-time multiprogramming foreground/background operating system	
DMS Disc Monitor System	Disc-oriented batch processing	8K words of memory; disc; card reader; Teletypewriter
DPS Data Preparation System		
Generalized Utilities System	Basic stand-alone system	4K words of memory
LANGUAGE PROCESSORS		
Fortran Compiler	Fortran IV	8K words of memory, card reader; Teletype
18/30 Uniapt	Implementation of Apt continuous path NC-part program language	Requires 16K memory; mass storage; paper tape reader & punch; card reader; line printer; Teletype
Assemblers		
ASM 1, 2, and 3	Compatible with IBM 1130/1800 card/paper tape assembler	Requires 4K-wd memory; card or paper tape reader/ punch; Teletype or printer
OTHER SOFTWARE		
BSC Binary Synchronous Communication	Can support double buffered controllers	Requires 8K words or memory
Core Image Converter	Constructs programs from main lines generated by Fortran compiler and assemblers	Requires 8K words of memory; paper tape reader; Teletype
1130 Loader/Exec Pkg	For loading and executing programs generated on an IBM 1130	Requires 4K words of memory; Teletype

HEADQUARTERS

General Automation
1055 South East Street
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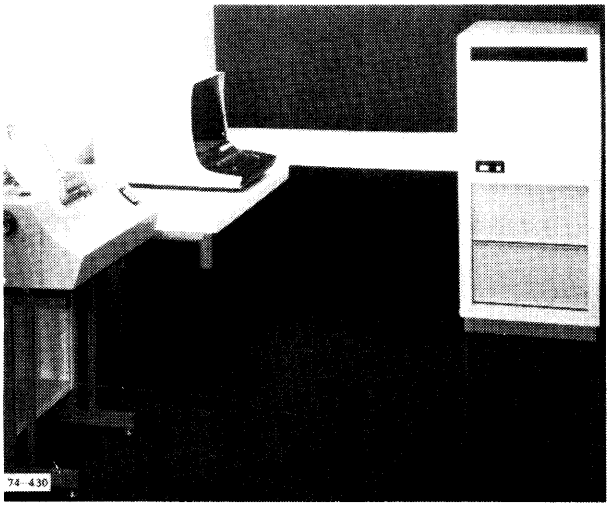
GRI COMPUTER

GRI-99 Series, Models 10, 30, 40, and 50



OVERVIEW

The GRI-99 systems are moderately small general-purpose minicomputer systems suitable for functions ranging from dedicated controller applications and time-related applications to customized process control. Rather than aiming the systems at the general marketplace, GRI is directing the GRI-99 Series to OEM markets. The GRI-99 Series is very modular with respect to hardware but currently offers very little applications software.

There are four models in the GRI-99 Series: 10, 30, 40, and 50. The models differ in the processor features, the type of system console included, and the number of devices that can be connected. The Model 10 is the least powerful and offers the fewest features; each higher-numbered model offers progressively more power and options. The Model 10, then, is a stripped-down system suitable for dedicated controller applications. The Model 30 is an economical and versatile system particularly suited for real-time applications and for systems dedicated to complex tasks. The Model 40 is like the Model 30, but it has extended mathematics and floating-point arithmetic capabilities. The Model 50 includes context switching, stack processing, bit manipulation, block (byte string) extended arithmetic for effective data transfer and multiprogramming, and disc I/O facilities. Characteristics of the models appear in Table 1.

All systems are organized around an asynchronous bus that connects all system elements, functioning much like the PDP-11 Unibus. Although it is not a microprogrammed system in the usual sense of the word, customized macroinstructions are easily added to the system via ROM modules accessed by an External Instruction (EI). Other system elements such as extra registers can be added in the same manner.

GRI provides a variety of peripheral devices to choose from, including discs, Teletype, display, paper tape and card I/O, printers, magnetic tape systems, communications devices, and extensive A/D, D/A, and digital I/O interfacing. The Grisette II cassette tape system is used to provide a hardware/software combination enabling the user to create an automatic load-and-go system, using an auto loader feature. Peripherals available are listed in Table 2.

System software includes a cassette tape real-time executive operating system, a relocatable assembler, source text editor, utility package, and diagnostic and math packages. GRI has developed a small business system called System 99, which runs under a single-user or multiuser disc operating system that supports RPG II and Basic compilers, as well as various utilities. The System 99 is based on the Model 50.

The GRI-99 Series was introduced in 1972 and is successor to GRI's 909 Series first delivered in 1970. The earlier 909 Series had the distinction of being the first system on the market with the asynchronous single bus architecture, which has since been made famous by DEC's PDP-11. Texas Instruments (960A/980A) also uses roughly the same type of architecture. Many of GRI's early users chose the system because of this innovative architecture.

COMPETITIVE POSITION

Although the company does sell to end users, GRI's main impact is in OEM markets. Companies strong in the 16-bit OEM market include Computer Automation, Microdata, and General Automation. Computer Automation and General Automation recently strengthened their positions by delivering low-cost, compatible microcomputers that are very competitive in the market for dedicated controllers (the primary target for GRI-99 Model 10).

The introduction of Model 50 to the GRI line has considerably expanded the series' capabilities. Model 50 is the base of GRI's System 99, a small business system. Although it seems oriented for a wider market, GRI is currently marketing System 99 to OEM manufacturers, manufacturers' software houses, and distributors. GRI currently has around 2,000 installations, including a substantial number in Europe and Japan.

USER REACTIONS

Most of GRI's users chose the systems because of their architecture, and most find the systems quite satisfactory.

Manufacturer

One of GRI's first users was a manufacturer of customized process control systems designed mostly for public utilities. The company based its system on the GRI-909 because of the bus structure, which at the time was unique. The company also has considered Lockheed's MAC 16, Honeywell's H316 and Data General's Nova; the PDP-11 was not announced until about a year later.

Table 1. GRI: Mainframe Specifications

MODEL	10	30	40	50
CENTRAL PROCESSOR				
Control Memory	No	No	No	No
Microprogrammed	No	No	No	No
No. of Registers	10	11	17	19
Max No. of Devices	9	Unlimited	Unlimited	Unlimited
Instruction Set				
Number	229	229	233	245
Floating-Point Firmware	No	Opt	Std	Std
Block Manipulation/Stack Handling	No	Opt	Std	Std
Extended Arithmetic	No	Opt	Std	Std
Consoles				
Blank Panel	Std	Opt	Opt	Opt
Operator's Console	Opt	Std	Opt	Opt
Programmer's Console (5-register display)	Opt	Opt	Std	Std
Priority Interrupt Levels	16			
Number of Addressable Devices	64			
Addressing				
Direct (no. of words)	32,768			
Indirect	1 or 2 levels			
Indexed	Yes			
MAIN STORAGE				
Type	Core			
Cycle Time (μsec)	1.76 core; 0.88 ROM			
Basic Addressable Unit	16-bit word, 8 bit byte; block on Model 40			
Bytes/Access	2			
Capacity (min/max, words)	4K-32K			
Increment Sizes (bytes)	4K; 8K			
Parity	No			
Protect	No			
ROM				
Use	Bootstraps; extension to instruction set			
Capacity	32 words			
INPUT/OUTPUT CHANNELS				
Programmed I/O (wds/sec)	80,000			
DMA				
No. of Channels	1			
Max Transfer Rate (wds/sec)	568,000			

When GRI switched to the 99 Series, this user followed suit, so that now roughly half of its 37 to 40 installations are based on the 99. The company obtains the processors and an occasional disc from GRI. This user designs the rest of the peripherals in-house and does all the programming. A programmable bus switch has been incorporated into a number of its systems, allowing redundant systems to be set up. This user likes the engineering of the GRI systems (although the grounding on the original 909 was better) and stated that GRI's support has been quite satisfactory.

Laboratory

A large laboratory on the East Coast has a 909 and a 99, both obtained because of the system's bus structure and the 16-bit word length. At the time the decision was made, the PDP-11 had not been announced, and 16-bit machines were not so prevalent. The laboratory recently obtained a second GRI system because it was quite satisfied with the performance of the first one. Also, the user had designed a number of unique interfaces and wanted to retain compatibility. Although interested in the new 99/50 processor, because it had a lot of new features they could use, this user was hesitating because the upgrade would mean that could not be maintained.

Configuration Guide

GRI-99 processors are housed in a standard 19-inch cabinet with provisions for optional feature cards. Two major firmware options and up to nine firmware or interface modules can be added to the system; six slots are included in the basic system and five more can be added within the chassis. The number of peripherals interfaced

Table 2. GRI-99 Series Peripherals

LOW-SPEED PERIPHERALS
- 43101 Paper Tape Reader (300 cps; requires 43100 interface)
- 43102 Paper Tape Punch (75 cps; requires 43100 interface)
- 43103 Paper Tape Reader/Punch (300/75 cps; requires 43100 interface)
- 43110 Card Reader 300 or 400 (80-col cpm; tabletop unit; requires 43110 interface)
- 43131 Printer (dot matrix; 100 cps; requires 43130 interface)
- 43132 Printer (dot matrix; 135 cps; requires 43130 interface)
- 43133 Printer (dot matrix; 270 cps; requires 43130 interface)
- 43134 Printer (300 lpm; 132 cols; 64-char set; requires 43130 interface)
- 43135 Printer (356-1,100 lpm; 132 cols; 64-char set; requires 43130 interface)
- 43141 Teletype 33 ASR (10 cps; 43143 interface; 43140 TTY modification)
- 43142 Teletype 35 ASR (heavy duty; 10 cps; requires 43143 interface)

HIGH-SPEED PERIPHERALS
- 43211 Grisette II Duplex Read/Write Cassette Tape System (1 drive; 50-ft, or 300-ft cassettes; needs 43210 controller)
- 43212 Same as 43211 (but 2 drives included)
- 43221 Cartridge, Disc Drive (1 removable cartridge; 1.2M wds/cartridge, 20 *u*sec latency up to 4 drives/43220 controller)
- 43222 Dual Cartridge Disc Drive (1 fixed, 1 removable cartridge/drive (2.4M words per drive); 20 *u*sec latency; up to 4 drives/43220 controller)
- 43223 Dual Cartridge Drive (like 43222 except 5.3M words/drive)

SPECIAL PERIPHERALS
- 43144 Display (1,600 char; 20 lines, 80 char each; requires 43145 RS232 I/O interface, up to 2,400 baud)
- 42400 Digital I/O Interfaces (can include 42400 gate input card with 16 unfiltered gates, general output register; 42402 binary input multiplexor with 32 lines (2 groups of 16 unfiltered input gates) per card; the 42403 binary output MUX/Relay drivers with 2 16-bit registers, 42404 binary output MUX/Logic output drivers with 2 16-bit registers for driving TTL or DTC Logic; 42405 pulse input detector for 8 inputs; 42406 10-MHz interval timer; 42407 10MHz watchdog timer with dual output that includes a contact closer and audible alarm)
- 42408 DMA Selector Channel (provides control for high-speed block transfers via DMA)
- 43300 Series Analog/Digital and Digital/Analog Conversion Equipment

Table 2. (cont.)

Unipolar Equipment (includes 43300 A/D 8-bit converter with 6.1-msec conversion at ±5V; 43301 A/D 8-bit A/D converter with 15.5-msec conversion at ±5V; 43302 10-bit converter with 13.5-msec conversion time at ±5V; 43303 10-bit A/D converter with 21-msec conversion time at ±5V; 43304 8-bit A/D converter with 15.5 *u*sec with 6.1-msec conversion time at ±10V; 43306 A/D 10-bit converter with 21-*u*sec conversion at ±10V; 43307 10-bit A/D 10-bit converter with 13.5-*u*sec conversion at ±10V; 43308 A/D 12-bit converter with 23.6-*u*sec conversion at ±10V; and 43309 12-bit A/D converter with 15-*u*sec conversion at ±10V)

Bipolar Equipment (43310 8-bit A/D converter with 15.5-*u*sec conversion at ±V; 43311 8-bit A/D converter with 21-*u*sec conversion at ±5V; 43313 10-bit A/D converter with 15.5-*u*sec conversion at ±5V; 43314 12-bit A/D converter with 23.5-*u*sec conversion at ±5V; 43315 12-bit A/D converter with 15-*u*sec conversion at ±10V; 43316 8-channel MUX; 43317 16-channel MUX; 43311 24-channel MUX; 43319 32-channel MUX; 43320 sample and hold with 5-*u*sec setting and 50-nsec aperture; and 43321 ±28V auxiliary power supply)

D/A Conversion (43322 8-bit D/A converter with 39.22 MV accuracy and ±10V range; 43323 10-bit D/A converter with 9.78 MV accuracy and ±10V range; 43324 12-bit D/A converter with 2.442 MV accuracy and ±10V range; 43325 8-bit D/A converter with 39.37 MV accuracy and ±5V range; 43326 10-bit D/A converter with 9.785 MV accuracy and ±5V range; and 43327 12-bit converter with 2.443 MV accuracy and ±5V range)

can be further expanded by attaching external I/O extension chassis with 16 more slots each. Four slots are available for memory expansion with either 4K- or 8K-word memory modules.

The power monitor/auto restart, the console-mounted autoload switch, and the operating key-lockout-security device optional features must be specified when ordering the computer. Similarly, models cannot be upgraded in the field to the next highest model number.

The following can be field-installed:
42204 Blank console with power switch.

42205 Operator's console with LED display.
42206 Programmer's console like the 42205 but with LED display of five registers.
42207 Extended arithmetic, including six registers.
42208 Byte swap pack.
42209 Byte binary pack for skip tests on equal, less than, and not equal.
42210 Six general-purpose registers.
42211/42212 Real-time clocks.
42213 Auto loader for Grisette II cassette subsystem.
42214 Teletype ROM bootstrap.
42215 High-speed reader ROM bootstrap.
42216 Custom auto loader (to 32 instructions).
42217 Power for I/O extension chassis.
42218 I/O extension chassis with 16 slots.

Consoles do not require mainframe slots. The extended arithmetic option uses both of the processor's firmware ports, and the six general-purpose registers use one (note, however, that the arithmetic option includes six registers). The byte swap pack and the 8-bit binary comparator can use either an I/O or a firmware port. All other processor options except the expansion chassis power require one I/O port.

The GRI 99/50 represents a variation from the configuring rules because it is almost a complete package. The smallest system configuration consists of one GRI 99/50 processor, 16K words of core memory, one disc unit, one line printer, and one video display terminal. In its maximum configuration, it consists of one 99/50 processor, 32K words of core memory, four disc units, five video terminals, two line printers, one 80-column card reader/punch, one 96-column card reader/punch, one reel-to-reel magnetic tape drive, and one paper tape reader/punch.

Software for the business system is bundled and includes an executive, I/O service routines, RPG II, and run-time subroutines.

COMPATIBILITY

The GRI-99 Series processors are upward-compatible from Model 10 through Models 30, 40, and 50. All use the same peripheral devices. The GRI-99 is not compatible with any other line of computers. The GRI-99 Model 50 uses some of the peripheral device addresses that are unused on other models. If a user has assigned these addresses to special-purpose devices, the 99/50 will not be upward compatible with that GRI-99 or 909 system.

MAINTENANCE AND SUPPORT

Maintenance is usually provided by the OEM customer to the end user. The OEM customer keeps a supply of spare parts and sends defective parts back to GRI for repairs. GRI supplies maintenance contracts for users in the Boston area. Raytheon services GRI computers in other areas.

GRI provides training courses in programming and maintenance at its home office throughout the year.

PRICE DATA

Model Number	Description	Purchase $[1]
	CENTRAL PROCESSOR AND WORKING STORAGE	
GRI-99	Basic Processor	
41202*	99/18 (8K words of memory)	5,115
41204*	99/38 (8K memory and operator console)	5,505
41206	99/48 (8K memory, 6 additional general-purpose registers, programmer console and floating-point firmware)	6,170
41208	99/58 (8K memory, power switch, operator panel, arithmetic operator, 10 general-purpose registers, 1 additional processor port, 3 memory ports, 4 I/O ports, 223 classes of instructions)	6,410
	Memory (1 memory port required)	
4160	8K x 16-Bit Random Access Core Memory	2,625
	Processor Options	
42200	Input/Output Port Expansion	106
42201	Power Monitor/Auto Restart	60
42202	Autoload Switch	70
42203	Operating Key Lockout	50
42205	Operator's Console	683
42206	Programmer's Console	822
42207	Extended Arithmetic Operator	575
42208	Byte Swap/Pack	140
42209	8-Bit Byte Binary	120
42210	Six General-Purpose Registers	270
42211	Real-Time Clock	205
42212	Real-Time Clock	175
42213	Autoloader for Grisette II Cassette Tape System	335
42214	ROM Bootstrap Loader (for TTY)	335
42215	ROM Bootstrap Loader (for high-speed reader)	335
42216	Custom Auto Loader	200
42217	Additional +5 vdc, 25 Amps (for use with I/O extensions)	500
42218	I/O Port Extension Chassis	975
	MASS STORAGE	
	Disc	
43220	Moving-Head Cartridge Disc Drive Controller and Interface (controls up to 4 disc drives)	4,000
43221	Moving-Head Disc Drive (1.2M words)	5,395
43222	Same as 43221 Except 2.4M-Bit Words (1 fixed, 1 removable disc)	6,530
43223	Same as 43222 Except 5.3M Words	7,475
	INPUT/OUTPUT	
	Magnetic Tape	
43211	Grisette II Full-Duplex Read/Write Tape System	1,170
43212	Grisette II Full-Duplex Read/Write Tape System (includes 2 recorders)	1,270
	Punched Card	
43111	Card Reader (300-cpm, 80-col)	3,850
43112	Card Reader (300-cpm, 80-col)	3,150
	Printers (freestanding)	
43131	100-cps Matrix Printer	3,980
43132	135-cps Matrix Printer	6,740
43133	270-cps Matrix Printer	7,980
43134	Line Printer (300-lpm, 132-col, 64-char)	11,875
43135	Line Printer (356-1, 100 lpm (zone), 132-col, 64-char)	14,850

PRICE DATA (Contd.)

Model Number	Description	Purchase $(1)
	INPUT/OUTPUT (CONTD.)	
	Teletype and Display Terminals	
43141	Teletype Model 33 ASR	1,875
43142	Teletype Model 35 ASR	4,850
43144	20 Lines, 80-Char Video Display	Factory Quote
	Paper Tape	
43101	Paper Tape Reader (300 cps)	1,830
43102	Paper Tape Punch (75 cps)	3,550
43103	Paper Tape Reader, Punch	4,695
	DATA COMMUNICATIONS	
43120	Universal Async Serial Character Input/Output Interface	383
43121	Universal Synchronous Serial Character Input/Output Interface	410
44005	Connector Contact Crimping Tool	165
44107	Arithmetic Operator	450

** Specify power requirements for other than 60 Hz, 115 vac; add $100 each unit, except for processors.*

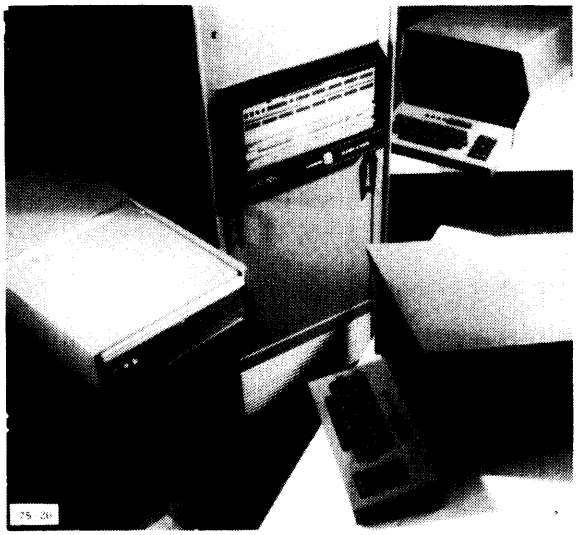
Note:
(1) Sold OEM only; quantity and OEM discounts available. Rentals not available. Maintenance not supplied by GRI except in Boston area, available through Raytheon and suppliers of end-user system.

HEADQUARTERS

GRI Computer Corp.
320 Needham Street
Newton MA 02164

HARRIS CORP.

Slash Series System Report



OVERVIEW

The Harris Slash series is a 24-bit-word minicomputer line, designed for high-speed, real-time, scientific applications requiring minicomputer to midicomputer size and power. The five basic models are Slash/1, 3, 4, 5, and 7; a ruggedized Slash/5R model is available for harsh environments. The Slash series models differ from each other primarily in size, speed, and price. Table 1 distinguishes between the models as far as memory speed and capacity.

All basic Slash series models are marketed in a modular fashion that appeals particularly to OEM manufacturers and other highly sophisticated users. Many Harris customers are in government installations or universities. However, in addition to the basic Slash series, Harris has introduced two lines of "packaged" systems aimed toward business-oriented mini users. The S100 series is based on the Slash/4 and the S200 on the Slash/7. Both operate under the Vulcan multiprogramming operating system. The S200 series adds virtual memory capabilities to the S100 systems. Vulcan is a demand paging system that supports time sharing, real-time processing, and batch processing. An impressive array of high-level languages (FORTRAN, COBOL, RPG II, SNOBOL, and FORGO) and a variety of RJE software packages are supported. All S100 and S200 software, with the exception of the RJE software, is bundled.

The Slash series was originally marketed by Datacraft as the 6024 systems. Datacraft became a subsidiary of Harris in 1974 and now is part of the Harris Computer Systems Division, which designs and sells core memory modules as well as computers. The Slash series has gained acceptance

Table 1. Harris Slash Series: Model Distinctions

Model	Memory Cycle Time (μsec)	Memory Capacity (words)
Slash/1	0.600	64K
Slash/3	1.000	64K
Slash/4	0.750/0.200	256K
Slash/5	0.950	64K
Slash/5R	0.950	64K
Slash/7	0.750/0.200	256K

in several major universities in scientific and time sharing environments. Although Harris emphasizes scientific, control, and data acquisition applications, the Slash series is also marketed for use with communications, optical character recognition, and microfilm processing. Marketing of the Slash series is handled in France, West Germany, the United Kingdom, the Netherlands, and Belgium, as well as through eight offices in the United States.

Slash/1 was announced in August 1968 as a 600-nanosecond digital computer. In December 1969 Slash/3, a less expensive, reduced-speed version of Slash/1, was announced. Restricted in speed and I/O expansion, the Slash/3 processor is fully compatible with Slash/1. The Slash/5 was announced in January 1971; it is software and I/O compatible with its predecessors. Slash/5 originally featured 1200-nanosecond memory and was restricted to 32K words. Today, its memory cycle time is 0.950 nanosecond and memory capacity is 65K words. Slash/5R, a ruggedized version of Slash/5, was delivered in the first quarter of 1973.

Slash/4 was also introduced in 1973; it has a 750-nanosecond cycle time and a 256K-word memory capacity. This system was an important step because it extended the size and power of the systems into the midicomputer range. It features bit processing, increased I/O capabilities, and optional multiported semiconductor memory with a 200-nanosecond cycle time. A virtual memory version, the Slash/4 VMS, adds virtual memory to the system, forming the basis of the S100 series.

HEADQUARTERS

Harris Corporation
Computer Systems Division
1200 Gateway Drive
Fort Lauderdale FL 33309
(305) 974-1700

All Slash series models are 24-bit-word computers; each word can store three bytes. The 24-bit word length provides capabilities unavailable with 16-bit-word computers and vies with 32-bit-word machines for many applications. Slash/4 is upward software and I/O compatible with the other systems, but virtual memory addressing prevents some Slash/4 software from running on the earlier models.

Slash/7, the most recent addition to the line, was initially delivered at the end of 1975. It is the first system designed and built under Harris manufacture. Slash/7 has a number of features that enhance throughput over Slash/4 systems. An asynchronous CPU and memory interleaving allow an effective memory cycle time of 425 nanoseconds on 675-nanosecond core modules. An instruction prefetch feature further expedites instruction execution times. Like Slash/4, the Slash/7 uses a separate I/O processor for high I/O throughput, in keeping with the performance levels of the rest of the system.

Of the six models, only Slash/4, 5, 5R, and 7 are actively marketed. Slash/1 and 3 have been superseded. Table 2 lists system specifications.

PERFORMANCE AND COMPETITIVE POSITION

Harris occupies an almost unique position in the upper range of the minicomputer market. Its Slash series computers use a 24-bit word; while most minicomputer systems, such as Data General ECLIPSE, HP 3000, and Digital PDP-11, use a 16-bit word. Other notable exceptions

Table 2. Harris Slash Series: Processor Characteristics

Model	Slash/1	Slash/3	Slash/4	Slash/5	Slash/7
Central Processor					
No. of Programmable Registers	5	5	5	5	5
No. of Instructions					
Std	596 + SAU, BP	584 + SAU, BP	602 + SAU, BP	592	602 +
Opt	—	—	—	—	—
Fixed-Point Arithmetic					
Add/subtract	Hardware	Hardware	Hardware	Hardware	Hardware
Multiply/divide	Hardware	Hardware	Hardware	Hardware	Hardware
Add time (μsec)	1.2	2.0	1.5	1.9	0.95
Floating-Point Arithmetic	Opt hardware	Opt hardware	Opt hardware	Software	Opt hardware
Addressing					
Direct (no. of words)	65,536*	65,536*	65,536*	65,536*	65,536
Indirect	65,536	65,536	262,124	65,536	262,124
Indexed	65,536	65,536	65,536**	65,536	65,536**
Max no. of I/O Devices	224	224	384	208	7
Priority Interrupt System					
Internal Traps	0-7	0-7	0-7	0-7	0-7
External Interrupt Levels	4-72	4-24	4-48	4-24	4-48
Memory					
Type	Core	Core	Core, semiconductor	Core	Core, semiconductor
Word Length (bits)	24 + 1 parity bit	24 + 1 parity bit	24 + 1 parity bit	24 + 1 parity bit	—
Cycle Time/Word (μsec)	0.6	1.0	0.75 (core); 0.20 (semiconductor)	0.950	0.75 (core); 0.20 (semiconductor)
Capacity (words)					
Max	65,536	65,536	262,124 (core); 32,768 (sc)	65,536	262,124 (core); 32,768 (sc)
Min	8,192	8,192	8,192	8,192	32,768
Increments	8,192	8,192	8,192	8,192	32,768
Parity	Std	Std	Std	Std	Std
Protect	Opt	Opt	Opt	Opt	Opt
I/O Channels					
No. of Channels	14	14	24	13	12
No. of Devices/Channel	16	16	16	16	16
Programmed I/O Channel	Std	Std	Std	Std	Std
Direct Memory Access	Opt	Opt	Opt	Opt	Opt
No. of DMA Channels (max)	14	14	12	13	12
Multiplexed I/O Channel	NA	NA	NA	NA	NA
Max Transfer Rate (wd/sec)					
Within memory	416,667	250,000	333,335 (core)	263,158	
Over DMA	1,666,667	1,000,000	1,333,333/port (core); 5M/port (SC or IOP with multiple channels)	1,052,632	1,600,000/port (core); 5M/port (IOP with interleaved channels or SC memory)

Notes:
*With special instructions
**Byte indexed to 192K bytes

are the Digital PDP-8 with its 12-bit word and the Digital PDP-15 with its 18-bit word. Some systems at the top of minicomputer lines are using 32-bit words, for example, Interdata 8/32 and Systems SEL 32. Others use mixed 16-/32-bit words, such as Microdata 3200, MODCOMP IV, Interdata 7/32, and PRIME 300.

Compared with the 16-bit word, the 24-bit word places less constraint on the number of instructions that can be implemented and the number of memory locations that can be directly addressed. In addition, the precision of the 24-bit word allows Slash series computers to perform single-precision operations for many applications that require double-precision operations on a 16-bit-word system.

Furthermore, each 24-bit word can store three bytes of information. Thus, an 8K-word memory for a Slash computer can store the same amount of data as a 12K-word memory for the typical 16-bit word mini. At the same time, the Slash computers can compete with larger 32-bit-word systems for certain applications that don't require 32-bit precision.

Because Datacraft was a small company, it concentrated on producing systems primarily for real-time and scientific applications. The larger Harris Corporation has already increased the sales and marketing staffs for the Slash series. Unlike Perkin-Elmer, which acquired Interdata and has since allowed it to function almost autonomously, Harris runs its Computer Systems Division. Most of Datacraft's top management is no longer with the company. Harris has a long history of expanding through acquisition, and a computer division was a logical addition to its line of products.

Slash/4 is the workhorse of the series. It can range in size from a small system with 8K words of memory for under $25,000 to a medium-scale system with 256K words (768K bytes) of memory and a cost of several hundred thousand dollars. Slash/5 is oriented mainly toward the OEM market. Although it is available by special order in a small configuration with only 4K words of memory, it can be expanded to a rather substantial system with 64K words (192K bytes) of memory. Slash/5R is a special version of Slash/5 that can be used for applications requiring a ruggedized system to withstand vibration and a harsh or abnormal environment. Slash/7 is an optimized Slash/4 with greater processing power, speed, and throughput.

The Slash series competes with the Digital PDP-11/40, -11/45, and -11/70, as well as PDP-15; the CDC 1700; HP 21MX and HP 3000; Interdata Models 7/32 and 8/32; Varian V73; Modular Computer System's MODCOMP IV; PRIME 300; Data General ECLIPSE; and SYSTEMS SEL 32. All of these systems were designed to operate in real-time environments. For certain applications, such as combined real-time batch and time sharing, Slash/4 and 7 systems can also compete with the Digital PDP-10.

Slash/4 and Slash/7 systems, which have optional multiport semiconductor memory, compete most directly with the PDP-11/70 with its four high-speed data channels. Both Slash/4 and 7 have an optional I/O processor interface that can support four I/O processor channels. I/O transfer rate via the Slash/4 and 7 semiconductor memory can be 2.5 million words per second per channel or up to 5 million words per second for the four I/O processors interlaced. The user can connect directly to the third port of the semiconductor memory and achieve an I/O rate of 5 million words per second, provided the port is not needed for a second CPU and the first CPU does not require access to the semiconductor memory at that time.

The new Slash/7 systems compete in the same market as the Slash/4, but at a higher level, by extending the Slash/4's power. Although Slash/7 has the same memory capacity as Slash/4, it is considerably faster and more powerful because of hardware features allowing faster instruction execution time, faster effective memory cycle time, and higher I/O throughput. Harris sees the Slash/7 as particularly cost-effective in large simulation applications where several Slash/7s might replace seven or eight smaller and/or slower systems. The Interdata 8/32 and SEL 32 are strong contenders in the simulation market.

Harris's packaged S100 and S200 series compete with Digital's PDP-11/70, Interdata's 8/32 Megamini, and SYSTEMS SEL 32. For sheer processor power, the Harris systems are quite competitive. What sets the S100 and S200 off from these other midicomputers is primarily the software, but the packaging is also different. The other midis don't support RPG II, and only Digital also supplies COBOL as a standard item.

Vulcan for both the S100 and S200 is a sophisticated operating system, which supports not only BASIC and FORTRAN IV but also RPG II and COBOL. The software combined with the packaging make the S100 and S200 more directly competitive with the HP 3000CX Mini Data Centers: HP 50CX, 100CX, 200CX, and 300CX. The HP 3000CX software, which is extensive, is generally unbundled except for the operating system, utilities, and SPL compiler. S100 and S200 software is bundled. The Harris and HP software offerings are very similar, with one notable exception. Hewlett-Packard offers an extensive data base management system (DBMS), IMAGE 3000 with the QUERY 3000 option. IMAGE 3000 is based on the TOTAL DBMS.

In a complex real-time environment the S200 can be front-ended by an S100. In a similar environment an HP 3000CX is front-ended by an HP 21MX system.

S100 and S200 are less expensive than the HP 3000CX for comparable configurations. This is even more apparent when a substantial amount of software is needed. Certainly the main memory and disc capacities are much larger for the S100 and S200. Both the S100 and S200 systems offer a large variety of peripherals, so the performance can be matched to the application. Plus, the 24-bit word of the S100 and S200 is a distinct advantage over the 16-bit word of the HP 3000CX for certain applications.

USER REACTIONS

Because most Slash systems are used for aircraft simulation or for research projects, a large number of them are connected in some way to the federal government. Harris has been gradually increasing its proportion of nongovernment users, however. To date more than 400 Slash/4 and Slash/5 systems have been installed, and Harris continues to fill Slash orders at the rate of around 15 per year.

User contacts comprised three nongovernment users who had either Slash/3 or 5 systems. One user is a major university that has nine Slash systems in operation and one on order. All users have found the systems fast and reliable, and all like the 24-bit word for data manipulation. The systems are used for such varied applications as computer network control, computer-aided instruction, data reduction from satellite, observatory management, ship-based polar exploration, batch processing, data base management, laboratory equipment management, data reduction from a mental retardation center, and link to an MS 6000 microfilm system. Maintenance for one of the systems is provided through Singer and rated excellent. None of the users made any negative comments about the systems.

CONFIGURATION GUIDE

All Slash systems except Slash/7 use the same basic configuration: a Slash processor with 8K words of memory (24 bits plus 1 parity bit per word); hardware multiply, divide, and square root; priority interrupt system with four external interrupts; five registers, of which three are index registers; 8-bit-wide parallel I/O bus; and basic software Slash/7 configurations begin with 32K words of memory.

Core memory can be expanded in increments of 8K words for all models except Slash/7, which adds memory in 32K-word increments. Core can be purchased in multiple-port (one to five ports) as well as single-port modules. In addition, up to 32K words of the Slash/4 memory can be multiport (up to five) semiconductor memory with a 200-nanosecond cycle time. Maximum memory capacity is 64K words for all models except Slash/4 and Slash/7, which both have maximum memory capacity of 256K words.

An I/O processor interface is available as an option for use with the triple-port semiconductor memory. The I/O processor interface can handle up to four I/O processors. The following options are available for the Slash series:

- Program restrict and instruction trap (used with memory protect in multiprogramming environment).
- Address trap (address query for software debugging).
- Stall alarm.
- Interval timers.
- Direct memory access (DMA) — three types available; up to 16 devices can interface to each DMA unit.
- Priority interrupt levels — up to a maximum of 24 levels for Slash/3 and Slash/5, 48 for Slash/4 and Slash/7, and 72 for Slash/1.
- Bit processor (BP) — to retrieve or store bits within a word in memory (unavailable for Slash/5 or 5R).
- Scientific arithmetic unit (SAU) — provides floating-point arithmetic (unavailable for Slash/5 or 5R).
- Hardware bootstrap units for paper tape, card reader, disc, and magnetic tape.
- Additional I/O channels — 8-bit-wide channel with up to three integral controllers, dual 8-bit-wide channels, 24-bit-wide channel; maximum of 14 channels for Slash/1 and 3, 24 channels for Slash/4 and Slash/7, and 13 for Slash/5 and 5R.
- I/O processor for Slash/4 and Slash/7.

The Slash/1 and 3 can support 14 DMA channels; the Slash/4 and 7 can support 12 DMA channels; and the Slash 5 can support 13 DMA channels.

All models use the same peripheral devices. Mass storage devices include fixed-head disc units, moving-head disc packs, and disc cartridges. Conventional peripherals include Teletype ASR and KSR 33, 35, and 38; paper tape reader and punch; card reader; card reader/punch; card punch/keypunch/verifier/interpreter; and magnetic tape drives. Two drum plotters can also be interfaced: One uses a 12-inch drum and the other a 30-inch drum.

Data communications facilities include a synchronous interface for transmission at 1200 to 9600 baud, an asynchronous interface for transmission at 112.5 to 9600 baud, and a multiplexor that can connect to eight synchronous or 16 asynchronous units via line interface units.

Table 3 summarizes specifications for the peripherals.

The basic software package for the Slash computers includes a Resident Operating System (ROS), MACRO Assembler, FORTRAN support library, utility package hardware diagnostics, and cross-reference package. If magnetic tape is included in the configuration, then a Tape Operating System (TOS) is used instead of ROS.

For disc systems the Disc Operating System (DOS II) or Disc Monitor System (DMS) controls system operation. DMS supports real-time processing, time sharing, interactive terminals, and batch processing. FORTRAN IV, RPG II, BASIC, FORGO (FORTRAN Compile and Go compiler), and SNOBOL can run under DOS II or DMS. In addition, FORTRAN IV and FORGO can run under ROS or TOS.

Slash/4 and Slash/7 can run under Vulcan, a disc-based, virtual memory system, with appropriate hardware changes to support virtual memory. Configuration requirements for the major software packages are listed in Table 4.

Vulcan requires certain hardware adjustments to a system for demand paging. These can be made in the field. A Slash/4 or 7 user who upgrades to run Vulcan is

actually changing the Slash system into an S100 or S200 system. Basic S100 and S200 systems include 32K words of memory, a 120-Hertz clock, a stall alarm, a chain block controller (CBC), I/O controller, disc bootstrap, bit processor, CRT, 300 card-per-minute card reader, 200 line-per-minute printer, and 10.8 million-byte disc.

COMPATIBILITY

Slash/1, 3, 5, and 5R systems are completely compatible. Slash/4 and Slash/7 are software and I/O compatible with other Slash systems except for the optional paging scheme (virtual memory configuration) of systems with more than 64K words of memory. The Slash/4 is upward software compatible from the other models. Slash/7 is completely compatible with Slash/4.

Table 3. Harris Slash Series: Peripherals

Device	Description
Terminals	
2100 Series	ASR, KSR 33/35/38 TTYs; 10 cps
2300 & 8600 Series	CRT displays; 24 lines, 80 char
2200 Series	Silent 700 terminals
Punched Cards	
3010/20/30	330/600/1,000-cpm readers
3200	500-cpm reader; 100-cpm punch
3300	Keyboard/verifier/punch; 3172 interpreter; 35 cpm
Punched Tape	
2005/2020	300-cps readers
2010	75-cps punches
2030	75-cps punches
2015	300-cps reader; 75-cps punch
Printers	
4030/4040	200-lpm line printers
4050/60/70	400/600/1,000-lpm line printers
4700 Series	Printer-plotters; 300-1,200 lpm
Magnetic Tape	
6660/70	9-track; 800/1,600 bpi; 75 ips
6040/50/60	9-track; 800/1,600 bpi; 100/150/200 ips
6210/20/30	7-track, 556/800 bpi; 100/150/200 ips
6630	7-track; 550/800 bpi; 45 ips
6640	9-track; 800 bpi; 45 ips
6650	9-track; 1,600 bpi PE; 45 ips
Discs	
5120/5130	Moving-head discs; 28/56M capacity
5230-5260	Moving-head cartridge discs; 2.7/10.8 capacity
5420/40/70	Fixed discs; 430Kb/860Kb/2,150Kb capacities
5500 Series	Disc pack subsystem; 40M bytes/pack
Process I/O	
9400	A/D subsystem; to 128 channels; A/D, D/A, digital and high-level analog input systems
Communications	
9031MUX	Up to 16 async, 8 sync lines or 2/1 combination
9010	Sync controller; 1,200-9,600 baud
9020/1/4	Async controller; 112.5-9,600 baud

Table 4. Harris Slash Series: Software

Package	Description
DMS	Disc Monitor System; a foreground multiprogramming system with background batch processing capability; requires console, binary input device (2), 24K words of memory for min system
Vulcan	Virtual memory operating system; disc-based; requires 32K words of memory, Slash/4 and 100 series or Slash/7 and 200 series configuration; console must be CRT, disc, mag. tape
DOS	Disc Operating System; uses a disc loader & utilizes a nonresident service area to bring in required modules; requires binary input device*; 8K words for min system
TOS	Tape Operating System; uses a mag. tape loader; console; 3.5K words for op system, 8K words for min system
ROS	Core Resident Operating System; uses paper tape or card I/O loader; requires 3,500 locations plus I/O areas; console; min system requires 8K-word memory
FORTRAN IV	FORTRAN IV compiler; a superset of ANSI FORTRAN IV; requires 4,600 + *n* locations (*n* = size of the data pool); needs 8K words above operating system, except DMS or Vulcan
FORGO	Compiler (FORTRAN Load and Go); provides extensive debugging features; needs 8K words above min DOS/TOS/ROS; no extra needed for DMS or Vulcan
RPG	RPG II; 8K above TOS or DOS; no extra memory needed for DMS or Vulcan
BASIC	Dartmouth BASIC for user; only available with DMS or Vulcan; no extra memory needed
SNOBOL	Char string manipulation language incl. compiler, interpreter, storage allocation; needs 48K words of memory under DMS, TOS, DOS; no extra under Vulcan
MACRO	Assembler; requires 3,100 + *n* locations (*n* = size of symbol table); available in MACRO form when more than 8K system; otherwise use Basic Assembler
UTILITIES	FORTRAN support library (incl. single- and double-precision floating-point routines; utility package provides system software support routines that are not resident in core (source update, etc.); Sort/Merge; indexed sequential; editor; cross-reference program; hardware diagnostics; object time trace; an interactive, program debugging aid

* Paper tape, magnetic tape, punched card

Note: All software is available at no charge. The appropriate operating system is provided to meet the system configuration. Source software is subject to extra charges.

RJE packages under Vulcan allow communications compatibility with a large number of computer systems. These emulate the CDC UT-200 for the 6000/7000 series, the IBM 2780 and HASP II M/L for the IBM System/360 and 370, and the Univac 1004 for the 1100 Series.

MAINTENANCE

Harris supplies contracts for prime-shift, 2-shift, or 3-shift maintenance. Preventive maintenance and emergency calls during the contracted shift(s) are performed for a monthly fee. Harris can also supply a dedicated on-site service engineer on a contractual basis. If the user does not want a contract, service is available on a per-hour basis (4 hours minimum) plus expenses; or user parts can be shipped to the Florida factory via the nearest service center.

PRICE DATA

MODEL NO.	DESCRIPTION	PURCHASE PRICE $	MONTHLY MAINT.*(1) $
	SYSTEMS		
System 110	Series 100 CPU (Slash/4; 96K bytes of core memory; 10.8M-byte cartridge disc with controller; 9-track, 800-bpi, 45-ips mag. tape unit with controller; CRT with keyboard, controller, & comm. multiplexor)	85,000	760
System 210	Series 200 CPU (Slash/7; 192K bytes of interleaved core memory; 860K-byte fixed-head disc with controller; 40M-byte storage module drive with controller; 9-track, 800-bpi, 45-ips mag. tape unit with controller; CRT with keyboard, controller, & comm. multiplexor; 600-cpm card reader with controller & stand; 200-lpm line printer with controller; SAU)	159,000	1,375
System 220	Series 200 CPU (Slash/7; 288K bytes of interleaved core memory; 1.7M-byte fixed-head disc with controller; 40M-byte storage module drive with controller; 9-track, 800-bpi, 45-ips mag. tape unit with controller; CRT with keyboard, controller, comm. multiplexor; 1,000-cpm card reader with controller & stand; 600-lpm line printer with controller; SAU)	189,000	1,910
System 240	Series 200 CPU (Slash/7; 576K bytes of interleaved core memory; 2.1M-byte fixed-head disc with controller; 80M-byte storage module drive with controller; additional 80M-byte storage module drive; 9-track, 800/1,600-bpi, 150-ips mag. tape unit with controller; additional 9-track, 800/1,600-bpi, 150-ips mag. tape unit; CRT with keyboard, controller, & 2 comm. multiplexors; 1,000-cpm card reader with controller & stand; 600-lpm line printer with controller; SAU)	400,000	3,045
	CENTRAL PROCESSORS & WORKING STORAGE		
Slash/4-1	CPU (24K bytes of 750-nsec core memory; memory parity, hardware multiply/divide/square root; priority interrupt control system; 4 external priority interrupts; 5 registers, 3 indexable; 8-bit I/O channel, IOC/IC; BP; basic software; in 19-in. cabinet)	24,000	165
Slash/4-2	CPU (same as Slash 4-1 except 48K bytes of core)	31,000	215
Slash/5-1	CPU (24K bytes of 950-nsec core memory; memory parity; hardware multiply/divide/square root; priority interrupt control system; 4 external priority interrupts; 5 registers, 3 indexable; 8-bit I/O channel, IOC/IC; basic software; mounted in 19-in. cabinet)	16,500	115
Slash/5-2	CPU (same as Slash 5-1 except 48K bytes of core)	21,500	150
Slash/7	CPU (96K bytes of 425-nsec core memory; memory parity; hardware multiply/divide/square root; priority interrupt control system; 4 external priority interrupts; 5 registers, 3 indexable; 8-bit I/O channel, IOC/IC; power fail shutdown & restart; 120-Hz clock; bootstrap timing & control; BP; basic software; mounted in 19-in. cabinet)	45,000	315
	PROCESSOR OPTIONS		
415/715	Scientific Arithmetic Unit (SAU)	9,900	70
416/716	Program Restrict & Instruction Trap	1,000	10
417/717	Stall Alarm	650	10
418/718	Interval Timer	750	10
419	Power Fail Shutdown & Restart	500	10
420	Address Trap	650	10
421	120-Hz Clock	150	10
422/722	100-kHz Real-Time Clock	1,500	10
424/724	Run Time Meter	150	10
516	Program Restrict & Instruction Trap	1,000	10
517	Stall Alarm	650	10

PRICE DATA (Contd.)

MODEL NO.	DESCRIPTION	PURCHASE PRICE $	MONTHLY MAINT.*(1) $
518	Interval Timer	750	10
519	Power Fail Shutdown & Restart	500	10
520	Address Trap	650	10
521	120-Hz Clock	150	10
522	100-kHz Real-Time Clock	1,500	10
425-429, 516-519	Hardware Bootstrap	750	10
435-439, 525-539	Additional Hardware Bootstrap	250	10
	MEMORY		
401	24K-Byte Memory Increment	7,000	40
402	48K-Byte Memory Increment	12,200	75
415	Scientific Arithmetic Unit (SAU)	9,900	70
703	96K-Byte Memory Increment	25,000	150
710	24K-Byte Semiconductor Memory	26,750	160
711	Additional 24K-Byte Semiconductor Memory	22,500	135
404	24K-Byte Core Memory System	12,000	70
405	Additional Increment (up to 3)	7,000	40
406	48K-Byte Core Memory System	17,200	105
407	Additional 48K-Byte Increment (up to 3)	12,200	75
410	24K-Byte Semiconductor Memory System	26,750	160
411	Additional 24K-Byte Increment	22,500	135
501	24K-Byte Memory Increment	5,000	30
706	48K-Byte Multiport Core Memory System	17,200	100
707	Additional 48K-Byte MP/CM Increment (up to 3)	12,200	75
447	Chain Block Controller (CBC)	2,200	15
448	External Block Controller (XBC)	2,000	15
451	Priority Interrupt Expander (above 24 levels)	1,250	10
455/755, 457/757	I/O Processor (IOP) for Multiport Memory	3,500	20
463/763	8-Bit IOC-IC with Multi-CPU Channel Adapter	950	10
464/764	24-Bit IOC with Multi-CPU Channel Adapter	1,450	10
466/766	CBC with Multi-CPU Channel Adapter	2,450	15
470/770	Memory Expansion Chassis (beyond 192K bytes)	7,500	45
484/486, 784/786	Port (IOP) MP/SCM	3,000	20
487 to 489	Port (IOP) MP/CM	1,500	10
560	1 Set of Link Cables (2 link each ABC; 2 each p.i. generator)	5,750	35
561	CPU Link Cable to Link Slash/5 to Slash/4, 5, or 7 (I/O channels not incl.)	1,250	10
570	Memory Expansion Chassis (beyond 96K bytes)	3,500	20
571	I/O Expansion Chassis (beyond 6 channels)	3,500	20
735-739	Hardware Bootstrap	350	10
743	24-Bit IOC	1,200	10
745	8-Bit IOC/Integrated Controller (IOC/IC)	750	10
747	Chain Block Controller (CBC)	2,200	15
748	External Block Controller (XBC)	2,000	15
750	Priority Interrupt (1 level)	150	10
751	Priority Interrupt Expander (above 24 levels)	1,250	10
752	Priority Interrupt Generator	300	10
	MASS STORAGE		
	Discs		
5120	Moving-Head Disc & Controller (28M bytes)	30,000	300
5130	Moving-Head Disc & Controller (56M bytes)	37,500	375
5230/A	Cartridge Disc with Controller (2.7M bytes; single platter)	10,900	110
5240/A	Cartridge Disc with Controller (5.4M bytes; double platter)	11,500	115
5260/A	Cartridge Disc with Controller (10.8M bytes; double platter)	12,900	130
5410	Fixed-Head Disc with Controller (268K bytes)	14,000	125
5420	Fixed-Head Disc with Controller (430K bytes)	15,500	140
5430	Fixed-Head Disc with Controller (537K bytes)	17,500	160
5440	Fixed-Head Disc with Controller (860K bytes)	20,000	180
5450	Fixed-Head Disc with Controller (1,075K bytes)	23,000	205
5460	Fixed-Head Disc with Controller (1,720K bytes)	26,500	240
5470	Fixed-Head Disc with Controller (2,150K bytes)	30,500	275
5510	Storage Module Drive with Controller (40M bytes)	28,500	255
5530	Storage Module Drive with Controller (80M bytes)	33,500	300
5515	Storage Module Pack (40M bytes)	1,000	NA
	INPUT/OUTPUT		
	Magnetic Tape		
6210	Controller & MTU (7-track; 556/800 bpi; 100 ips)	38,000	340
6220	Controller & MTU (7-track; 586/800 bpi, 150 ips)	42,000	380
6230	Controller & MTU (7-track; 556/800 bpi, 200 ips)	46,000	415
6240	Controller & MTU (9-track; 800/1,600 bpi; 100 ips)	40,000	360

PRICE DATA (Contd.)

MODEL NO.	DESCRIPTION	PURCHASE PRICE $	MONTHLY MAINT.*(1) $
6250	Controller & MTU (9-track; 800/1,600 bpi; 150 ips)	44,000	395
6260	Controller & MTU (9-track; 800/1,600 bpi; 200 ips)	48,000	430
6630	MTU & Controller for up to 4 Drives (7-track; 800/556 bpi; 45 ips; tension arm; incl. cabinet)	11,000	100
6640	MTU & Controller for up to 4 Drives (9-track; 800 bpi; 45 ips; tension arm; incl. cabinet)	12,000	110
6650	MTU & Controller for up to 4 Drives (9-track; 800/1,600 bpi (PE); 45 ips; tension arm; incl. cabinet)	16,000	145
	Printer/Plotters		
4710	11-in. Size, 500 LPM Printer	15,000	150
4730	20-in. Size, 300 LPM Printer	17,500	175
	Paper Tape		
2010	Paper Tape Reader (300 cps) with Controller	2,500	25
2020	Paper Tape Punch (75 cps) with Controller	3,500	30
2030	Paper Tape System (300 cps/75 cps) Reader/Punch with Controller	5,750	50
2130	ASR 33 TTY Unit Only	2,100	50
2140	KSR 33 Unit Only	1,900	35
2150	ASR 35 Unit Only	6,500	80
2160	KSR 35 Unit Only	4,000	50
2170	RO 35 Unit Only	3,900	45
2180	ASR 38 Unit Only	2,750	35
2190	KSR 38 Unit Only	2,400	30
	Console Devices*		
2210	ASR 733 (30 cps) with Controller	5,000	65
2220	KSR 733 (30 cps) with Controller	4,000	50
2320	TTY Replacement CRT (24 lines/80 char with keyboard, interface & controller)	3,200	45
2325	2320 with Hard-Copy Device	6,700	100
	Punched Cards		
	Card Equipment		
3010	Card Reader (300 cpm) with Controller	5,000	45
3030	Card Reader (1,000 cpm) with Controller	10,000	90
	Line Printers		
4040	Line Printer (200 lpm, 64 char) with Controller	12,200	135
4120	Line Printer (600 lpm, 64 char) with Controller	19,500	175
4125	Line Printer (436 lpm, 96 char) with Controller	21,500	195
4070	Line Printer (1,000 lpm) with Controller	60,000	660
	Remote Terminals		
8530	TTY ASR 33	2,100	50
8540	TTY KSR 33	1,900	35
8570	TTY RO 35	3,900	45
8590	TTY ASR 38	2,400	30
8610	Harris-Modified Interactive CRT for Model 8630	5,150	75
8620	Harris-Modified TTY Replacement CRT for Model 8630	2,850	45
8630	Interactive CRT for RS232 Interface	5,150	75
8640	TTY Replacement CRT for RS232 Interface	2,850	45
8720	KSR 733 Terminal	3,500	45
	Communications		
8140-1	Asynchronous Controller	3,000	30
8310	Communications Multiplexor	3,000	30

*Require Model 445, 545, 745, or 7310.

Notes:

(1) Includes on-call service, 7 A.M. to 5 P.M., 5 days per week with full parts replacement and preventive maintenance. Overtime is at rate of $32/hour.

HARRIS CORPORATION
S100 and S200 Series

HEADQUARTERS

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OVERVIEW

The new Harris computers are systems built around configurations of the 24-bit-word Slash 4 and Slash 7 processors. The Slash 4 was developed by Datacraft before it was purchased by Harris in 1974. The Slash 7 is currently under development and has not yet been delivered. The Slash 4 has been around since 1973. The new systems are the S110 and S120 based on the Slash 4 and the S210, S220, S230, and S240 based on the Slash 7. All the system software except remote job entry is tightly bundled to the hardware.

All systems run under VULCAN (Virtual Core Manager), a demand paging, multiprogramming system that supports timesharing, real time and batch processing. VULCAN supports an impressive array of language processors: FORTRAN IV, COBOL, RPG II, Macro Assembler, SNOBOL 4 (COBOL derivative), and FORGO (Compile and go FORTRAN). Support programs include Sort/Merge, Indexed Sequential File Handler, Interactive Text Editor, Cross Reference, DEBUG, and Trace. Automatic spooling from disc to slow-speed devices is a standard feature, as well as job accounting for billing purposes. On-line diagnostics are also standard. Remote job entry software is available to emulate the CDC UT-200 for the 6000/7000 Series, IBM 2780 and HASP II M/L for the System 360/370 Series, and Univac 1004 for the 1100 Series. These packages are unbundled and cost $5,000 each for installation.

MAINFRAME

The Slash 4 and 7 processors are powerful number crunchers with a rich instruction set of over 600 instructions, including fixed-point and floating-point arithmetic for add, subtract, multiply, divide and square root. Floating-point arithmetic is performed by a SAU (Scientific Arithmetic Unit) that uses double precision operands, 8-bit exponent and 39-bit fraction. Instructions also perform byte and bit manipulations.

Virtual memory is a hardware/software system that is transparent to the user but transfers pages, 1K words each, between main memory and a disc unit. It has two operating modes: user and monitor. In the user mode, a memory map translates memory references into an 18-bit address that selects a word within one of the 256 pages. Thus, a user program can reference up to 256K words of data; 64K words can be executable code. Pages can be non-contiguous in main memory or on the disc. When an addressed page is not in memory, a demand page instruction trap interrupt is generated to swap it into memory. In the monitor mode, mapping is disabled.

The same core memory modules (750 nanoseconds cycle time per word) and most of the same peripherals are used for both the S100 and S200. Because the S200 Series systems are larger and more powerful than the S100 systems, some large discs and high performance peripherals

are available for the S200 only. The S100 is a synchronous system and cannot support interleaved memory. For the asynchronous S200, pairs of 16K-word memory modules are interleaved for an effective cycle time of about 425 nanoseconds. Only single ported memory modules are offered for the S100. Two- or four-port memory modules are available for the S200 for up to 192K bytes. In addition, 96K bytes of semiconductor memory in modules of 24K bytes with two or four ports each, are available for the S200.

Input/output for both systems is via up to 12 I/O channels. IOCs, 8 or 24 bits wide, are available for up to 16 slow speed devices each, and CBC (Chained Block Controllers) units are available for up to 16 high speed devices operating under channel control. An IOP (input/output processor) is optional for the S200. Transfer rate via IOCs is a function of the program controlling the data transfer. Maximum transfer rate via CBC is 2.7M/2M bytes per second for input/output on the S100 and 3.8M/2.9M bytes per second for input/output on the S200. With interleaved memory and multiple channels, the maximum aggregate transfer rate is 5.7M bytes per second. Transfer rates via IOP are 5M bytes per second for input or output and 5.7M bytes per second for multiple channels and interleaved memory.

Disc capacity ranges from 10.8M bytes on disc cartridge to 80M bytes on moving head disc storage modules for the S100, and from 40M to 240M bytes on disc storage modules for the S200. Fixed-head and floppy discs are also available for the S200.

First shipments of both the S100 and S200 are scheduled for the fall 1975.

COMPETITIVE POSITION

Table 1 compares the S100 and S200 with recently announced midicomputers.

No matter how often one compares computer systems, one never ceases to wonder at the infinite variety in packaging: CPU features and options, memory types and sizes, peripherals with a variety of performance characteristics, and software. Bundled/unbundled? What price to pay? Where? It is difficult to define "like" systems to compare. Unlike the earlier Slash Computer Series, which were modular, general-purpose systems, the S100 and S200 systems are bundled according to some marketing alchemist's dream or research or something. Earlier Slash Series systems were marketed like minicomputers to sophisticated users from a modular, shopping list of constituent components. In fact, most customers are in government installations or on college or university campuses and, from our interviews, are satisfied customers. In this kind of market, the S100 and S200 will compete with Digital's PDP-11/70, Interdata's 8/32 Megamini and SYSTEMS SEL 32. For sheer processor power, the systems are quite competitive. What sets the S100 and S200 off from these midicomputers is primarily the software, but the packaging is also different. The midis don't support RPG II, and only Digital supplies COBOL as a standard item.

VULCAN for both the S100 and S200 is a sophisticated operating system which supports not only BASIC and FORTRAN IV, but also RPG II and COBOL. The software combined with the packaging make the S100 and S200 more directly competitive with the HP 3000CX Mini Data Centers: HP 50CX, 100CX, 200CX, and 300CX. Because of space, Table 2 compares them only with the 50CX and 300CX. The HP 3000CX software, which is extensive, is generally unbundled except for the operating system, utilities and SPL compiler. The S100 and S200 software is bundled. The software offerings are very similar, with one notable exception. Hewlett-Packard offers an extensive data base management system (DBMS), Image 3000, with the Query 3000 option. It is based on the Total DBMS. In a complex real-time environment, the S200 can be front-ended by an S100. In a similar environment, the HP 3000CX is front-ended by an HP 21MX system.

The S100 and S200 appear less expensive than the HP 3000CX for comparable configurations. This is even more apparent when a substantial amount of software is needed. Certainly the main memory and disc capacities are much larger for the S100 and S200. Both systems have a large variety of peripherals to choose from, so the performance can be matched to the application. The 24-bit word of the S100 and S200 is a distinct advantage over the 16-bit word of the HP 3000CX for certain applications. Like most new systems, the S100 and S200 appear to have the price/performance competitive edge, for the moment at least.

COMPATIBILITY

The S100 and S200 are upward compatible with the earlier Slash Series: Slash 1, 3, 4 and 5.

Table 1. Comparison of S100 and S200 with Competing Midicomputers

Characteristics	Digital PDP-11/70	Interdata 8/32	SEL 32	Harris S100	Harris S200
CENTRAL PROCESSOR					
Microprogrammed	Yes	Yes	Yes	No	No
Control Memory	ROM	ROM	ROM	–	–
No. of Registers	10 accs: 3 stack pointers; 1 PC; all 16-bit; all can be used as indexers	2 stacks of 16 32-bit gen regs std; 6 more sets opt	8:3 can be used as index regs	6:3 can be used as index regs	6:3 can be used as index regs
Word Length	16	32	32	24	24
Addressing					
Direct	To 64K bytes	To 1M bytes	To 512K bytes	To 192K/96K(2) bytes	To 768K/96K(2) bytes
Indirect	Single level	No	Multilevel to 16M bytes	Single level, all of memory	Single level, all of memory
Indexed	Yes	Yes	Pre- and post-indexing	Yes	Yes
Mapping	Yes, to 2M bytes	Yes, to 1M bytes	Yes, to 16M bytes	Yes, to 192K bytes	Yes, to 786K bytes
Instruction Set					
Implementation	Firmware	Firmware	Firmware	Hardware	Hardware
Types	Single word	Single and double word	Half and full word	Single word	Single word
Number	400 std; 46 opt	214	152	Over 600	Over 600
Floating Point	Hardware opt	Hardware opt	Firmware std	Hardware opt	Hardware std
Hardware Stack	Yes	No	No	No	No
Instruction Execution Times (μsec)					
Fixed Point					
Add	1.0	1.1	1.2	1.5	1.0
Multiply	3.8	5.6	4.5	6.0	2.1
Divide	8.3	5.7	5.1	11.3	6.4
Floating-Point(1)					
Add	7.9	2.0	3.0	0.8–2.3	0.8–1.8
Multiply	9.9	3.2	4.5	5.3	5.0
Divide	10.9	5.0	8.9	12.0	11.7
Writable Control Store	No	No	No	No	No
Interrupts					
Levels	4 lines, 8 levels	1,024	128	10-48	14-48
Type	Hardware	Hardware	Hardware	Hardware	Hardware
MAIN STORAGE					
Type	Bipolar (cache); core (main memory)	Core	Core	Core	Core/SC
Cycle Time* (μsec)	0.24 (bipolar); 1.0 (core; 32 bits)	0.750	0.600	0.750	0.750/200
Basic Addressable Unit	Word, byte	Word, half-word, byte	Double word, word, half-word, byte, bit	Word, byte, bit	Word, byte, bit
Bytes/Access	4	4	4	3	3
Cache Memory	Bipolar, 2,048 bytes	Bipolar, 16 bytes	–	–	–
Capacity (bytes)					
Min	64K	131,072	32,768	98,304	196,608
Max	2M	1,048,576	1,048,576	196,608	786,432
Increment Size (bytes)	64K	128K	32K	48K	48K
Ports/Module	1	1	1	1/2/4	1/2/4
Error Checks	Parity std	Parity opt	Parity: 1 bit/byte std	Parity: 2 bits/wd std	Parity: 2 bits/wd std
Memory Protection	Yes; memory management and 3 operating modes	Yes, with memory management	Yes, in pages of 512 words	Yes, in pages of 1K words	Yes, in pages of 1K words
Memory Management	Yes	Yes	Yes	Yes	Yes
Interleaving	Yes, 2-way	4-way	2 reads/4 writes	No	2-way
INPUT/OUTPUT					
Max Devices Addressable	No limit	1,024	Via IO Crs	16/channel	16/channel
Programmed I/O	Yes (UNIBUS)	Yes	Yes, IOC	Yes, IOC	Yes, IOC
DMA	Std (UNIBUS); plus 4 high-speed data channels	Std for 112 devices	IOC	CBC	CBC/IOP
DMA Transfer Rate	4M bytes/sec (UNIBUS); 5.8M bytes/sec (data channel)	6M bytes/sec	1.2M bytes/sec each; 26.7M bytes/sec aggregate	2.7M bytes/sec; 4M bytes/sec aggregate	3.8M bytes/sec (CBC); 5.M bytes/sec (IOP); 5.7M bytes/sec aggregate
Price for System with 128K-byte Memory	$54,600(4)	$49,900	$43,900	(3)	(3)

Notes:
*Effective memory cycle time varies with type of memory and number of memory modules interleaved.
– Not applicable.
(1) PDP-11/70 times include operand load times. Also floating-point processor operates in parallel with central processor.
(2) User mode/Monitor mode.
(3) Sold only as bundled systems, see Table 2.
(4) CPU bundled with console, line clock, and installation.

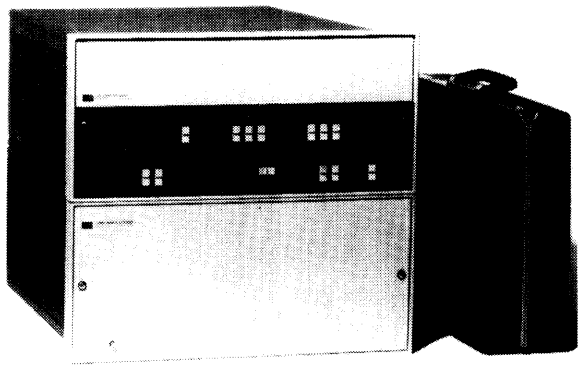
Table 2. Comparison of the S100 and S200 with the HP 50CX and HP 300CX

	HP 50CX	Harris S110	Harris S120	HP 300CX	Harris S210	Harris S220	Harris S230	Harris S240
Hardware[1]								
CPU	3000CX	Slash 4	Slash 4	3000CX	Slash 7	Slash 7	Slash 7	Slash 7
Word Length, bits	16	24	24	16	24	24	24	24
Memory	Core	Core	Core	Core	Core/SC	Core/SC	Core/SC	Core/SC
Min/Max, K bytes	96/128*	96/192*	144/192*	128	192/384*	288/384*	480/576*	576/768*
Hardware Floating Point	*	*	*	*	X	X	X	X
Decimal Arithmetic	*	—	—	*	—	—	—	—
System								
Operator Console	CRT	CRT	CRT	CRT	CRT	CRT	CRT	CRT
Virtual Memory	X	X	X	X	X	X	X	X
Communications								
Mplr/Controller, lines	16	16	16	16	16	16	16	32
Mag Tape, 9-tk 800 bpi, 45 ips; number of units	1	1	1	1	1; 2*	1; 2*	2[2]; 3*	2[3]; 3*
Card Reader, cpm	—	—	600; 1,000*	—	600/ 1,000*	1,000	1,000	1,000
Card Reader/Punch, cpm	—	—	—	200/75	—	*	*	*
Line Printer, lpm	—	—	200; 600*	1,250	200; 600*	600	600	600
Floppy Disc, KB	—	—	—	—	310	310	310	310
Cartridge Disc, MB	5	10.8	10.8	—	—	—	—	—
Moving-Head-Disc, MB	—	40*; 80*	40*; 80*	47	40; 80*; 120*; 160*	40; 80*; 120*; 160*	40; 80*; 120*; 160*	160; 240*
Fixed-Head Disc, MB	—	—	—	2	0.86	1.7	2.1	2.1
Software								
Operating System	MPE/C	VULCAN	VULCAN	MPE/C	VULCAN	VULCAN	VULCAN	VULCAN
Spooling	X	X	X	X	X	X	X	X
Accounting	X	X	X	X	X	X	X	X
FORTRAN, ANSI Std	*	X	X	*	X	X	X	X
BASIC								
Interactive/Compiler	*/*	X/—	X/—	*/*	X/—	X/—	X/—	X/—
COBOL, ANSI Std	*	X	X	*	X	X	X	X
RPG II	*	X	X	*	X	X	X	X
Macro Assembler	SPL[4]	X	X	SPL[4]	X	X	X	X
SNOBOL 4 (COBOL-like)	—	X	X	—	X	X	X	X
FORGO (Load & Go FORTRAN)	—	X	X	—	X	X	X	X
Support Programs								
Sort/Merge	X	X	X	X	X	X	X	X
Sequential File Handler	X	Index	Index	X	Index	Index	Index	Index
Interactive Text Editor	X	X	X	X	X	X	X	X
Debug	X	X	X	X	X	X	X	X
Trace	X	X	X	X	X	X	X	X
Statistical Analysis	*	—	—	*	—	—	—	—
Data Base Management								
Image/3000	*	—	—	*	—	—	—	—
Query/3000	*	—	—	*	—	—	—	—
Remote Job Entry								
CDC UT 200	—	*	*	—	*	*	*	*
IBM 2780	* +	*	*	* +	*	*	*	*
Univac 1004	—	*	*	—	*	*	*	*
IBM HASP II M/L	—	*	*	—	*	*	*	*
On-Line Diagnostics	X	X	X	X	X	X	X	X
Total Price, $ in 000	99.5	85.0	119.0	203.5	159	189	280	400

Notes:

*Option, priced separately.
X Standard item.
— Not available.

(1) All peripherals available for the HP 3000CX and for the Slash Series can interface to the respective systems.
(2) 75 ips; 800/1,600 bpi.
(3) 150 ips; 800/1,600 bpi.
(4) ALGOL-like.



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OVERVIEW

The HP21MX is Hewlett-Packard's latest implementation of its popular 2100 Series of computers. The 21MX is completely upward compatible with the 2100. Virtually all 2100 software can be used on the 21MX, and all 2100 peripherals can interface with the 21MX I/O channels. Features of the 21MX Series include microprogramming ability, semiconductor memories, and a potential address space of 1 million words. The system is intended for both OEM and end-user markets.

The 21MX series initially consists of two models: M/10 or HP 2105A and M/20 or HP 2108A. The M/10 is the smaller of the two models, differing from the M/20 primarily in memory capacity and in control store and I/O expandability.

The central processors provide 128 instructions in the standard set; 80 that emulate the HP 2100 Series, 42 that implement indexing, bit and byte manipulation, and byte and word moves, plus six that perform floating-point arithmetic. The instruction set implemented by microprogrammed firmware is supplied on four ROM modules of 256 locations each. Maximum control store capacity is 4,096 24-bit words. Additionally, writable control store RAMs are optionally available. Each module supplies 256 24-bit locations. The microprocessor instruction set includes 178 microinstructions.

Main memory consists of N-channel MOS semiconductor modules with a cycle time of 650 nanoseconds. Memory parity generation and checking are standard, and memory protect is optional.

Special power failure and brownout protection is standard, providing for memory integrity through a line loss of 10 Hz. Optional stand-by battery power is available to maintain 32K words of memory for two hours if a total power failure occurs. A direct memory access option for two channels is available for high-speed devices.

The system logically structures memory into 1K pages. Through a variety of addressing techniques (direct, indirect, indexing) any location in memory can be addressed.

The optional Dynamic Mapping System (DMS) provides techniques for expanding the system's physical address space to 1 million words. It supplies four sets of 32 registers each — two sets for mapping user and operating system and two sets for data control, permitting scatter/gather I/O operations. The DMS is available only on the M/20. A memory protect feature is included, which supplies both a programmable fence register and page oriented read/write protect.

The 21MX provides 60 levels of chained priority interrupt. The 2105A has four standard I/O channels, and the 2108A has nine standard channels. Both models can expand I/O capacity by 34 channels in increments of 17. The channels support a wide range of high- and low-speed peripherals, TTY and CRT terminals, plus special-purpose gear.

The systems are designed to withstand the same shocks and vibrations as HP's electronic instruments, and are protected against extremely high voltages. They will function in a temperature range of 0° to 55° Centigrade.

Software is provided to perform batch operations, multiprogramming, foreground/background processing, remote job entry, time sharing, and real-time processing. The system supports an assembly language system, FORTRAN, FORTRAN IV, BASIC, and ALGOL. Additionally, a terminal control system for data communications is available, plus a data base management system and over 1,000 canned programs and microcoded routines.

First customer deliveries were made in June 1974.

COMPETITIVE POSITION

The HP 21MX Series extends the processing capability of a popular line of minicomputers; over 9,000 HP 2100 systems have been installed. The series utilizes modern technology — all semiconductor memory, for example — to provide systems that are smaller, weigh less, consume less power, and cost less than the earlier 2100 systems. Almost all major minicomputer manufacturers are following this same route to modernize their computer lines.

In contrast to Interdata and MODCOMP, which use a 32-bit word for their top-of-the-line systems, Hewlett-Packard has kept the 16-bit word but has incorporated the ability to extend the power of its systems substantially by the simple expedient of adding larger memory capacity and a memory management unit, which generates 20-bit addresses. This allows addressing of 1,048,576 words of physical memory. The feature also provides significant hardware/software control over program and data page allocation with no impact on system cycle time.

The 21MX has a large 4K-word control memory which allows for a fairly broad set of microcoded user

application oriented routines. In the earlier 2100 series, a more limited control store provided throughput improvement over conventional programmed instructions of 10 to 50 times for some applications. Thus, increases of even greater magnitude can also be expected from the 21MX.

Major competition for the HP 21MX will be the Data General Nova/Supernova and ECLIPSE Varian V70 Series, Interdata 7/16 and 7/32, and the DEC PDP-11. Primarily due to its orientation to instrumentation, Hewlett-Packard has generally provided more application-oriented packages than other minicomputer manufacturers.

As processors continue to provide more and more power and performance for less and less money, and plug-compatible peripherals proliferate, minicomputer manufacturers must take the problem-solving system approach to marketing. Less sophisticated users want easy-to-use systems that do a job. This means manufacturers must provide application-oriented systems that can be easily customized for a specific job.

Hewlett-Packard has taken this approach previously with its time-sharing, test and measurement, and distributed processing systems, and is currently expanding it with its data base management and remote job entry systems. The same approach is being followed with the 21MX with its comprehensive range of software including seven operating systems, four languages, special-purpose processors such as data base management and query system and remote job entry, plus an extensive application program library.

The 21MX must be considered a major and serious entry into the minicomputer arena, and it should prove to be the prime contender in many competitive procurements.

MAINTENANCE AND SUPPORT

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world, including 60 service facilities in the United States and Canada backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for "parts only" warranty for 15 months; a second provides for full services, parts, and labor for 90 days. Follow-on agreements can provide for either guaranteed response times and full service or a per-call time and materials service.

CONFIGURATION GUIDE

A minimal 21MX configuration consists of a mainframe and 4,096 words of semiconductor memory. Peripherals can be added to the basic configuration, depending on the requirements of the user. Mainframe characteristics are given in Table 1. A complete list of available peripheral devices is supplied in Table 2.

Table 1. Hewlett-Packard 21MX: Mainframe Characteristics

Type	2105A Micro-programmed	2108A Micro-programmed
CENTRAL PROCESSOR		
Control Memory	Yes	Yes
Size	1,024 (24 bits)	1,024 (24 bits)
Use	Firmware	Firmware
No. of Internal Registers	9; additional 16 at micro level	9; additional 16 at micro level
Addressing		
Direct	2,048	2,048
Indirect	Multilevel; 32,768	Multilevel; 32,768
Indexed	Yes	Yes
Instruction Set		
Implementation	Firmware	Firmware
Number (std; opt)	128; 38; 178 micro-instr	128; 38; 178 micro-instr
Decimal Arithmetic	No	No
Floating-Point Arithmetic	Yes, firmware	Yes, firmware
User Micro-programming	Yes	Yes
Priority Interrupt System Levels	60	60
MAIN STORAGE		
Type	SC	SC
Cycle Time (μsec)	0.650	0.650
Basic Addressable Unit	Wd (16-bit)	Wd (16-bit)
Bytes/Access	2	2
Cache Memory		
Min Capacity (bytes)	8,192	8,192
Max Capacity (bytes)	65,563	393,216
Increment Size (bytes)	8K; 16K; 32K	8K; 16K; 32K
Ports/Module	1	1
Error Checks	Parity	Parity
Protection Method	No	Fence reg
Memory Management	No	Opt
ROM	Yes	Yes
Use	Control storage Firmware; loaders	Control storage Firmware; loaders
Capacity	1,024 (24-bit)	1,024 (24-bit)
RAM	Opt	Opt
Use	Writable control Store (WCS)	Writable control Store (WCS)
Capacity	256 (24-bit)	512 (24-bit)
I/O CHANNELS		
Programmed I/O	Yes	Yes
DMA Channels	2	2
Multiplexed I/O (no. subchannels)	4; 32	9; 32
Max Transfer Rate (wd/sec)		
Over DMA	616,666	616,666
Simultaneous Operation	Yes	Yes

Table 2. Hewlett-Packard 21MX: Peripherals

DEVICE MODEL NO.	DESCRIPTION
Discs	All Models Moving Head
12960A	Cartridge, 1 removable, 1 fixed; sectored 2.5M wds, 47.5 access time, xfer rate 126 kws
12961A	Same as 12960A except contain only 1 removable platter
12965A	Pack, 11.776M wds/pack, 32 msec access, xfer rate 155 kw/s
Magnetic Tape	
12971A	7-trk, 200/556/800 bpi, 25/37/45 ips
12970A	9-trk, 800 bpi, 25/37/45 ips
12972A	9-trk, 1,600 bpi, 25/37/45 ips
Console	
(listed under Terminals)	
Paper Tape	
12925A	Pchd PT reader, 500 cps
12926A	Tape punch, 75 cps
12927A	Tape punch, 120 cps
Punched Card	
12986A	Optical mark reader, 200 cpm
12985A	Card reader, 600 cpm
Line Printers	
12980A	200 lpm, 132 cols, 64-char set
12980A-001	150 lpm, 132 cols, 96-char set
12984A	300-1, 100 lpm, 80 cols, 64-char set
12982A	600 lpm, 132 cols, 64-char set
12982A-001	400 lpm, 132 cols, 96-char set
12987A	200 lpm, 132 cols, ROM customized char set
Displays	
7210A	Digital plotter, 20 vctrs/sec
7202A (also see under Terminals)	Graphic plotter, 2 vctrs/sec, 10/15/30 cps
A/D Subsystems	
12604A	Data source interface, 32 lines
D/A Subsystems	
12555B	D/A converter, 2 chan, 8 bits/chan
12597A	Duplex register, 8-bit, 48-pin
12566B	Micro-circuit duplex register, 16-bit, 48-pin
12930A	Universal interface, 16-bit
Digital I/O	
12539C	Clock, crystal bases (0.1ms to 1,000 sec Interval)
Data Communications	
12587B	Async data set interface (45-2, 400 bps)
12618B	T/R sync data set interface (9,600 bps)
12589A	Automatic calling unit interface
12531C/D	Async terminal interface (110-2, 400 bps)
12920A	Async multiplexor; 16 dev interfaces, 57-2, 400 baud
12880A	TTY or CRT channel, local or remote, buff/unbuff (110-2, 400 bps)
Terminals Supported	
2754A	TTY ASR 33 (10 cps)
2754B	Heavy-duty TTY ASR 35, (10 cps)
2762A	Term console printer KSR (35 cps, 75 cols)
2762A-006	Term printer KSR (30 cps, 118 cols)
2615A	Char mods CRT buffer 2,000 char
2616A	Pg mode CRT (stores/ 256 25 x 80 pgs)

Users operating under control of any of the operating systems described in Table 3 require (as a minimum) a paper tape reader, a console device such as a TTY, and the system device for the operating system, such as magnetic tape or disc. Beyond these limitations, the user is relatively free to expand the system up to the maximum memory capacity and maximum number of I/O channels — currently 196K words of memory with a potential for 1 million words, and up to 54 directly addressable devices.

The system's basic control memory provides for a maximum of 4,096 words of addressable ROM, the bulk of which is available to the user. In addition, a user can optionally add one (M/10) or two (M/20) modules of writable control store RAM (256 24-bit locations). Both the ROM and RAM facilities provide the user with extremely powerful implementation tools.

The 21MX Series is also available in several preconfigured versions at considerably reduced costs. The M/200 line is oriented towards a business environment;

Table 3. Hewlett-Packard 21MX: Software

PACKAGE NAME	DESCRIPTION
Basic Control System (BCS)	Executive monitor providing loac interrupt processing, and I/O drives; memory resident on min system; min config
Magnetic Tape System (MTS)	Batch processing; tape resident; can be used on single tape system; provides job control directives and executive functions
Disc Operating System-III (DOS-III)	Disc-resident batch processor; std executive function plus logical file mgmt and appl prog segmentation; 4,500 wds main mem; 400K bytes disc
Real-Time Executive (RTE)	Core or disc-resident; multi-programming, foreground/ background processing; prior prog sched; min config 16K
Time-Sharing System	Extended BASIC interpreter; up to 32 terminals
Language Processors	ASSEMBLY; FORTRAN; FORTRAN IV; BASIC; ALGOL
Special-Purpose IMAGE/2000	DBMS; allows structured data network; query and batch modes; uses min 5.5K memory, 300K bytes disc; will run under DOS-III
Remote Job Entry (RJE)	Remote job interface to OS360; will run under DOS-III
Terminal Control System (TCS)	Multitasking supervisor; up to 32 terminals; requires 6.5 memory
Applications Various	More than 1,000 applications-oriented macro and microcoded routines

the S/200 Series favors a scientific/engineering environment. Both packages provide highly sophisticated levels of data processing. The 21MX/55, a special disc-based configuration, is available for the OEM shop; it is based on M/20 with 32K words of high-density memory and includes 4.9 million bytes of disc cartridge storage.

The 21MX Series also provides facilities for data communication and time-sharing services. As noted in Tables 2 and 3, a wide variety of potential configurations are possible, operating under either the time-shared system or the terminal control system.

COMPATIBILITY

The 21MX Series is fully compatible with previous versions of the 2100 line of processors. Virtually all peripherals are interchangeable between the two lines, and all software written for the 2100 line should be convertible to the 21MX with few, if any problems.

HEADQUARTERS

Hewlett-Packard Company
1501 Page Mill Road
Palo Alto CA 94304
(415) 493-1501

TYPICAL PRICES

Model Number	Description	Purchase Price $	Monthly Maint. $
2124A	OEM Disc System (M/20 processor; 16K X/1 memory; dual channel port controller; 12960A disc subsystem; diagnostic software)	21,500	195
HP21-MX/55-008	8K X/1 Memory	19,400	191
HP21-MX/55-016	16K X/1 Memory	21,500	195
HP21-MX/55-024	24K X/1 Memory	24,000	199
HP21-MX/55-032	32K X/1 Memory	26,100	203
2124A-108	Add 8K X/1 Memory Module	2,500	
2124A-116	Add 16K X/1 Memory Module	4,600	
2124B	OEM Disc System	18,900	189
2124A-204	Add 4K X/2 Memory Module	900	
2124A-208	Add 8K X/2 Memory Module	1,500	
HP MX/65			
2125A	DISC computer with M/20 processor; 8K X/2 memory; dual channel port controller and 15 megabytes; 12962A disc subsystem	22,250	181
	Options		
2125A-012	Replace M/20 with M/30	900	NC
-016	Replace 8K module with 16K	1,200	NA
-204	Add 4K module	900	+ 2
-208	Add 8K module	1,500	+ 4
	Options for 2/24A/B		
2124A-003	Add Fast FORTRAN Processor	1,250	
2124A-004	Add Dynamic Mapping System	1,950	
2124A-005	Add Writable Control Store	1,000	
2124A-006	Add FFP and DMS	2,700	
2124A-008	Replace 16K with 8K	-2,100	
2124A-014	Add Disc Loader ROM	100	
2124A-015	230V/50 Hz	—	
	PROCESSORS AND WORKING STORAGE		
HP21-M/10			
2105A	Microprogrammable Processor, HP 21-M/10 (supports up to 32K semiconductor memory, provides 4 powered I/O channels and full user microprogramming)	4,150	66
HP21-M/20			
2108A	Microprogrammable Processor, HP 21-M/20 (supports up to 32K semiconductor memory; 9 powered I/O channels; opt memory protect and full user microprogramming)	5,300	66
HP M/30-			
2112A	Microprogrammable processor with 8 memory module slots for up to 128K of memory, fourteen powered I/O channels, and full user microprogramming capabilities	6,200	66
	Options for 2105A/2108A		
-003	Fast FORTRAN Processor	1,250	2
-004	Dynamic Mapping System (for 2108A only)	1,950	
-005	Writable Control Store	1,000	9
-006	Dynamic Mapping System and Fast FORTRAN Processor (for 2108A only)	2,700	
-014	Disc Loader ROM	100	—
	MEMORY		
2101A	Semiconductor Memory System, HP 21-X/1 (high density 8K- and 16K-word modules)	650	8
2102A	Semiconductor Memory System, HP 21-X/2 (medium density 4K- and 8K-word modules)	500	8
	Options for 2101A/2102A		
-001	Dual-Channel Port Controller	750	8
-003	Memory Protect (M/20 only)	500	9
-004	4K Memory Module (for 2102 only	900	2
-008	8K Memory Module	1,500	4
-016	16K Memory Module (for 2101A only)	4,600	8

Model Number	Description	Purchase Price $	Monthly Maint. $
-010	Additional Disc Drive for Subsystem	9,975	95
12961A	790A Cartridge Disc Subsystem (1 removable cartridge disc, moving head; 2.5 megabytes)	11,800	93
-010	Additional Disc Drive	6,775	79
12869A	Disc Cartridge	125	—
12965A	2883A Disc File w/Controller	29,900	157
-020	Additional Disc File as 2nd or 4th Drive	18,000	115
-030	Additional Disc File as 3rd Drive	27,900	152
12868A	Additional Disc Pack	620	—
12610C	Interface for 2766A Fixed-Head Disc Memory	4,535	6
	INPUT/OUTPUT		
2752A	Teleprinter, Modified Teletype ASR-33	2,000	54
2754A	Teleprinter, Modified Teletype ASR-35	6,950	54
2600A	Keyboard Display	3,965	50
2615A	CRT Keyboard Terminal (visual display of input/output 10 to 960 cps)	2,835	32
2616A	CRT/Keyboard Terminal (page mode operation)	4,500	41
2762A	Terminal Printer	4,920	29
-001 or -002	Same as 2762A, 220V/50 Hz, or 240/50V Hz	5,150	29
-006	2762A, Terminal Printer (with kybd, 118 cols)	6,055	29
-007 or -008	Same as 2762A, 220V/50 Hz or 240V/50 Hz	6,280	29
12925A	Tape Reader and Interface	2,295	31
12575C	Tape Winder	100	0
12989A	2894A Card Reader Punch Subsystem	12,450	123
-002	With off-line kybd Punch and Verify	14,250	123
12986A	7261A Optical Mark Reader and Interface	3,775	33
12985A	2892A Card Reader and Interface (600 cpm)	5,665	54
7260A	Optical Mark Card Reader	3,190	30
7261A	Optical Mark Card Reader (automatic feed)	2,760	30
12980A	2610A Line Printer and Interface (200 lpm; 132 cols/line, 64-char set)	14,935	86
-001	2610A-001 Line Printer and Interface (150 lpm, 96-char set, 132 cols/line)	17,035	86
12982A	2614A Line Printer and Interface (600 lpm, 132 cols/line, 64-char set)	30,385	142
-001	2614A-001 Line Printer and Interface (400 lpm, 132 cols/line, 96-char set)	32,960	142
12984A	2767A Line Printer and Interface (300 to 1,100 lpm, 80 cols/line, 64-char set)	13,900	52
12987A	2607A Line Printer and Interface (200 lpm, 132 cols/line)	7,950	2
12982A	2614A Line Printer and Interface (600 lpm, 132 cols/line, 64-char set)	30,385	142
-001	2614A-001 Line Printer and Interface (400 lpm, 132 cols/line, 96-char set)	32,960	142
12984A	2767A Line Printer and Interface (300 to 1,100 lpm, 80 cols/line, 64-char set)	13,900	69
12987A	2607A Line Printer and Interface (200 lpm, 132 cols/line, 64-char set)	7,950	72
-001	2607A-001 Line Printer and Interface (165 lpm, 128-char set)	8,450	72
12970A	Nine-Track NRZI Magnetic Tape Subsystem	8,900	72
-010, -011, -012	Additional Magnetic Tape Drive for Subsystem	6,850	61
12971A	Seven-Track NRZI Magnetic Tape Subsystem	12,400	105
-010, -011, -012	Additional Magnetic Tape Drive for Subsystem	6,900	62
12972A	Nine-Track Phase-Encoded Magnetic Tape Subsystem	10,900	109
-005, -006, -007	Additional Mag Tape Master Unit	9,375	89
-010, -011, -012	Additional Mag Tape Slave Unit	6,845	81
12935A	Digital Plotter Subsystem	4,235	43
7202A	Graphic Plotter ASCII Input	3,830	40

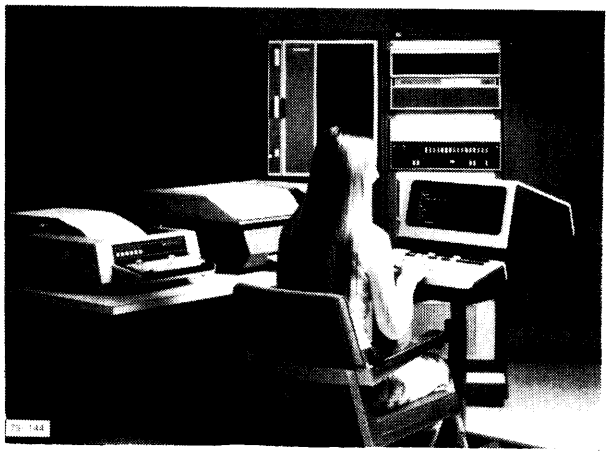
TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
	ACCESSORIES		
12892A	Memory Protect (M/20 only)	500	9
12897A	Dual-Channel Port Controller	750	8
12898A	Dual-Channel Port Controller for I/O Extender	500	10
12944A	Power Fail Recovery System	475	3
12945A	User Control Store Board	100	—
12976A	Dynamic Mapping System	1,950	
12976A-003	Add Fast FORTRAN Processor	750	
12977A	Fast FORTRAN Processor	1,350	10
12978A	Writable Control Store	1,250	9
12979A	I/O Extender	2,700	9
-010	Used as Second Extender	2,700	9
HP21-X/1	Field Memory Expansions		
12990A	Memory Extender	3,500	
12991A	Power Fail recovery for M/30 or 129900A	600	3
12999A	8K Memory Module	2,600	4
12997A	16K Memory Module	4,700	8
HP21-X/2	Field Memory Expansions		
12994A	4K Memory Module	1,000	2
12998A	8K Memory Module	1,600	4
	MASS STORAGE		
	DISCS		
12960A	7900A Cartridge Disc Subsystem (1 fixed disc and 1 removable disc served by the same moving head; 5 megabytes)	15,000	103
7203A	Graphic Plotter (binary input)	3,830	40
7210A	Digital Plotter	3,400	40
	DATA COMMUNICATIONS		
12587B	Async Data Set Interface	550	6
12589A	Automatic Calling Unit Interface	400	3
12618A	Transmit-Receive Sync Data Set Interface	700	5
12880A	Interface for 2600 CRT	350	4
12889A	Hardwired Serial Interface	750	4
12920A	Async 16-Channel Multiplexor for 103A-Type Modems or Terminals	2,200	15
12920A-001	Async 16-Channel Multiplexor for 202-Type Modems	3,000	19
	SOFTWARE		
24307B	DOS-III Software	2,500	—
24342A	Terminal Control System (TCS) Software	2,250	35
24376A	IMAGE/2100 Software	4,250	40
24380A	HP Remote Job Entry Software Package for BCS	1,250	40
-001	DOS-III Compatible HP RJE	1,250	40
20854A	Timeshare BASIC "F" Software	5,000	—
20855A	Basic Control System Software	500	—
20856A	Timeshare BASIC "E" Software	2,500	—
24383A	Course Writing Facility for Use with 20854A Software	2,500	45
24383B	Course Writing Curriculum Conversion	255	—
24387A	Basic Analysis and Mapping Program Software (requires 2000F system)	3,000	25

— Not Applicable NC No Charge NA Not Available

HEWLETT-PACKARD CO.

HP 21MX Report Update



ACCESS 2000 Hewlett-Packard 600-lpm Printer

Medium-Speed Printer

A new medium-speed printer, designated Model 13053A when used with the 21MX or 2100 minicomputer, has been announced by Hewlett-Packard.

The new printer operates at 600 lines per minute and prints 136 columns with a 64-character set. A 96-character ASCII drum is optional and the print rate is 436 lines per minute.

Business forms of up to six parts can be handled by the printer with spacing controlled by a 12-channel vertical format control tape, which can slew as many as 15 lines. Either six or eight lines per inch are switch-selectable. DOS, RTE, and 2000/Access operatng systems support the printer.

Purchase price for the printer with controller is approximately $16,350, depending on the options selected. First delivery was in September 1975.

ACCESS 2000

This dual-processor system is designed to perform three primary functions:

- Source data entry from 16 or 32 HP 2640 terminals.
- A HASP RJE station to an IBM System/360 or 370 host or a U200 terminal to a CDC host.
- Concurrent local processing for applications programming.

Access 2000 centers around a 21MX Model M/20,which operates as the systems processor, and a 21MX Model M/30, which operates as a communications processor, performing asynchronous interactive communications with the terminals and synchronous communications with the host processor. The communications processor functions are implemented in firmware to optimize efficiency. This is the first firmware system HP has marketed as a standard product.

The systems and communications processors are closely coupled, physically located in adjoining racks. The terminals can be connected locally, hardwired, or they can be located remotely and connected via telephone lines.

The HP ACCESS 2000 is available in two models: the Model 30 is a minimum configuration that can support 16 terminals. It consists of the following components:

- HP 21MX M/20 with 64K bytes of 4K MOS RAM.
- HP 21MX M/30 with 48K bytes of 4K MOS RAM.
- One 16-line multiplexor.
- Model 7900 Disc Drive with five megabytes of storage capacity.

The basic Model 30 price is $59,900.

The Model 40 is a larger configuration that can support 32 terminals. It consists of the following components:

- HP 21MX M/20 with 64K bytes of 4K MO RAM.
- HP 21MX M/30 with 64K bytes of 4K MOS RAM.
- Two 16-line multiplexors.
- HP 7905 Disc Subsystem with 15 megabytes of storage capacity.

Card readers and line printers at the local site, as well as the 2640 terminals, can perform RJE input/output functions for the host processor. At the same time users can be running interactive BASIC programs from the terminals.

The systems will be marketed initially to users of IBM System/360 and 370 and CDC 3300 or larger systems, and to Hewlett-Packard's current customer base of distributed processing systems.

The HP Access 2000 will compete with systems from Data 100, Entrex, Four Phase, and Datapoint.

HP 21MX, M/30

In March 1975, Hewlett-Packard announced a third model in the 21 MX line, the M/30, which extends system size upward from the M/10 and M/20. The M/30 sup-

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ports 32K words of memory in the processor chassis as a standard feature and 128K words with the Dynamic Mapping System option. If the Memory Extender is also added, memory capacity is 256K words. The M/30 uses the X/2 memory modules (650-nanosecond cycle time), which are available in 4K-, 8K-, and 16K-word modules. The M/30 also extends the number of addressable devices to 14 as a standard feature and to 46 with I/O extenders.

The M/30 chassis is 12.25 inches high and weighs 65 pounds. It has space for eight memory modules, 16 I/O channels, and two I/O extenders (16 channels each) in the main chassis.

Like the M/10 and M/20, the M/30 has all the 21MX Series features:

- 16-bit word plus one parity bit.
- Two accumulators.
- Two index registers.
- 12 scratchpad registers.
- Extended Arithmetic Unit (EAU).
- Floating-point arithmetic.
- Fast FORTRAN processor (scientific instuction set) optional.
- Single-ported memory.
- Priority interrupt system with 56 levels.
- Minimum interrupt latency: 4 μsec without floating-point and 75 μsec with floating-point arithmetic.
- Microprogrammed processor with optional Writable Control Store.
- ROM bootstrap loader.
- Data communications instructions.
- Power supply with "brown out" safety features.
- Memory built around 4K-bit MOS memory.
- Memory operating asynchronously with respect to processor.
- Multiple bus structure: one data bus, one address bus, one I/O bus.
- Line voltage: 88-132V or 176-264V (allows wide swing in line voltage).
- Line frequency: 47.5 to 16 Hz.
- Operating temperature: 0°C to 55°C.
- Operating humidity: 95 percent at 40°C.

The cost of the M/30 as compared to the M/10 and M/2 is as follows:

	M/10 $	M/20 $	M/30 $
Processor with 16K words of X/2 memory, EAU, and floating-point arithmetic	7,350	8,500	9,400
Maintenance	78	78	78
With Dynamic Mapping	NA	10,450	11,350
Fast FORTRAN Processor	1,250	1,250	1,250

Quantity discounts range from 15 percent to 34 percent for orders of 50 or more units.

Management/280

Management/280 is Hewlett-Packard's new data management system, which is based on the 21MX minicomputer and designed to handle on-line order processing functions. All the necessary applications software is included with the system.

With the new system, users can enter, update, and question customer orders; update their customer files; request information on products; print invoices; generate pick lists; and initiate sales and credit checks. Batch operations can also be performed: invoices can be printed, a daily list of the status of orders can be generated, or an up-to-date list of customers can be printed out each day.

Software supplied with the system includes ON-TOP (On-line Terminal Order Processing), IMAGE/2000 with QUERY/2000, and TCS (Terminal Control Software). The ON-TOP sales order processing software operates on-line; it can be used with IMAGE/2000 data base management software, to enter, change, and access data, and to create multiple indexes for commonly used information. With the QUERY/2000 module, the user can change information or generate reports without any additional programming. TCS simplifies adding or changing terminals and implementing user-written applications software.

Hardware includes the HP 21MX central processor with 32K words of semiconductor memory, a 1,600-bit-per-inch magnetic tape unit, a 4.9M-byte disc storage subsystem, a 200 line-per-minute printer, paper tape reader, terminal printer, and system console. The system can handle up to 10 additional workstation terminals.

Optional features, such as additional disc storage and A/N display stations, are available. A communications package allows M/280 to interconnect with systems using bisynchronous communications (IBM 360/370, for example).

PRICE DATA

Model Number	Description	Purchase Price $
19655B	HP 2108A M/20 24K-word micro-programmable processor, paper tape reader, 2762-A pick-list terminal printer, 4.9M-byte disc, 1,600-bpi mag tape, system table, double bay cabinet, disc operating system software, IMAGE/2000 software, memory expansion to 32K, multiple port I/O extender, ON-TOP software, TCS software, line printer, system console display, console interface	70,235
	OPTIONS	
015	230-V/50-Hz operation	NC
001	Replaces 4.9M-byte disc with 23.5M-byte disc	18,600
003	Replaces 1,600-bpi mag tape subsystem with 800-bpi subsystem	—2,000
213	Adds 14.7M-byte disc storage and cabinets	17,000
406	Deletes 1,600-bpi mag tape	—10,900
401	Deletes pick-list terminal and interface	—6,225
2640A	Order entry display terminals (1-5)	3,000
12880A	Terminal interface	350

OVERVIEW

The HP 3000CX Series contains a group of preconfigured systems intended to satisfy the batch and on-line data processing requirements of the general user. Each system is based on the HP 3000 16-bit minicomputer configured with 32K to 128K bytes of memory, peripherals, and software. Although the series has a strong orientation towards the terminal user and Hewlett-Packard's traditional market — scientific/engineering, time-sharing, and real-time processing, typical business-oriented components — COBOL, RPG II, and a data base management system — give the system an appeal to an extremely wide market.

Four models or hardware configurations are marketed within the series: 50CX, 100CX, 200CX, and 300CX. The four models use a common operating system (MPE/C) that operates in both terminal and multiprogramming batch mode with full spooling capabilities. Software is build around full hardware implementation in the stack architecture of the HP 3000 CPU. Each model is upward compatible and can be field expanded with a minimum of dislocation.

The CPU stack architecture gives the user reentrant, recursive programming without the excessive overhead of non-stack systems. The code and data segments of a program are segregated so that each functions in its own domain and each is addressable through its own register set. (No instruction in the HP 3000 permits a program operating in task mode to modify the program.)

The system has 176 microcoded instructions that perform fixed- and floating-point arithmetic, relational operations, boolean functions, word and bit tests, byte and word move operations, scan and test functions, plus various shift and program and loop control instructions. In addition, optional decimal and extended floating-point instruction sets are available. Provisions are also made for both indirect and indexed address modification.

In addition to the stack processing mode, the HP 3000CX provides for maximum usage of available memory space through a virtual memory addressing technique that is largely transparent to the user. Virtual memory address space is 64K words.

The system allows up to 253 separate priority interrupt levels and handles a variety of peripheral equipments. Three modes of I/O operation are available: direct, multiplexed, and selector channel. The organization of the interrupt and I/O systems allows independent ordering of device service priority, device access priority, and device interrupt priority.

The entire system is organized around a Central Data Bus; the CPU, main memory, IOP and selector channels use the central data bus to communicate with each other. Although this path serves as a limiting factor on access time and aggregate transfer rate, its speed of 5.7M bytes per second is sufficient to handle virtually all situations.

Table 1 lists the mainframe characteristics.

In addition to the MPE/C operating system for the HP 3000CX, Hewlett-Packard provides both a BASIC interpreter and compiler, FORTRAN, COBOL, RPG II, SPL (Hewlett-Packard's Algol-like System Programming Language) IMAGE/3000, various utility packages, such as Sort and Trace, and a host of applications programs.

The system can be integrated into a network of HP 3000CX data centers or interfaced to a large computing facility. Additionally, BASIC programs from the smaller HP 2100 and 21MX Timesharing Series can be moved up to the HP 3000CX processors.

Table 2 lists the basic and optional configurations of the four models.

Competitive Position

The HP 3000CX is in an excellent competitive position for the medium-scale, general-purpose processing environments in which it will be marketed. Its commercial processing features, notably COBOL, IMAGE/3000 (a data base management system), RPG II, and a spooling capability, should appeal to users with a variety of jobs — scientific, engineering, and commercial processing — and a limited budget.

Prime competition for the 50CX and 100CX will be Digital's 11/40 and 11/45 under RSTS-11/E or RSX-11D or M at the lower end, and small Digital System 10s as well as XEROX 550 and 560 with the 200CX and 300CX at the top end. Systems such as the Data General ECLIPSE Series, Burroughs 1700 Series, IBM 370/115, 125, and 135, Modular Computer MODCOMP IV, PRIME 300, Varian V74, General Automation SPC-16/80, and Interdata Models 7/32 and 8/32 compete for some applications.

The prime thrust of Hewlett-Packard's marketing activities will be towards new installations and upgrades of obsolete or obsolescent installations, BASIC timesharing

installations, and small commercial and various engineering applications. Because of its comprehensive software, the 3000CX should be a prime contender for customers with a wide variety of data processing tasks and a small budget. Although minicomputer manufacturers are providing more support for commercial processing, none offer the wide variety available with the HP 3000CX, especially comparable to IMAGE/3000 for data base management. This variety has been the domain of Xerox with its Sigma line (now replaced by 550 and 560) and Digital with its PDP-10. The sophisticated operating systems required to perform this variety of tasks on general-purpose systems are available only for large configurations. Minicomputers such as the PDP-11/45 are moving in this marketing direction. Thus, Hewlett-Packard should "make hay while the sun shines" because the hay fields will soon be full of competing reapers.

Configuration Guide

Table 1 lists the configurations for the four models of the 3000CX Series. The range of configurations addresses a broad spectrum of applications from the 50CX, which is geared to both the small user and the OEM market, to the 300CX, which is adaptable to most medium-scale environments. It should be noted that all models are based on a common processor and a common operating system. This single feature provides the user with the capability to upgrade his computing, terminal, and I/O power without the usual trauma associated with such changes.

Table 3 lists the peripherals available. Table 4 provides a summary of the available software.

Compatibility

The four models of the HP 3000CX Series are fully compatible with each other at the CPU and program level.

Table 1. HP 3000CX Series: Mainframe Characteristics

Central Processor	
Type	Microprogrammed
Control Memory	
Size	2,048 (32 bit)
Use	Firmware
No. of Internal Registers	11
Addressing	
Direct	Variable for instructions + data
Indirect	1 level, 64K
Indexed	Yes
Instruction Set	
Implementation	Microprogrammed
Number	172
Decimal Arithmetic	Opt firmware
Floating-Point Arithmetic	Yes (opt extended F-P firmware)
User Microprogramming	No
Priority Interrupt System Operation Modes	
Levels	253
Main Storage	
Type	Core
Cycle Time (msec)	0.980
Basic Addressable Unit	Word (16-bit)
Bytes per Access	2
Cache Memory	No
Min Capacity (bytes)	96K
Max Capacity (bytes)	28K
Increment Size (bytes)	32K
Ports per Module	1
Error Checks	Parity
Protection Method	Bounds/stack
Memory Management	Yes, stack
ROM	No
Use	
Capacity	
RAM	No
Use	
Capacity	
I/O Channels	
Programmed I/O	Yes
DMA Channels	4
Multiplexed I/O (no. of subchannels)	2 (32)
Max Transfer Rate	
Within Memory (Central Data Bus)	5.7M bytes
Over DMA	3.8M bytes
Simultaneous Operations	Yes

DATA COMMUNICATIONS

The HP 3000CX provides a wide variety of data communications facilities from a multi-terminal time-shared mode of operation to a multi-processing distributed network configuration and from a remote job entry or front-end facility to a large 370 type system.

When operating with a second processor, the interprocessor communications operations are multiprogrammed with both other terminal and batch jobs.

Maintenance and Support

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world including 60 service facilities in the United States and Canada, backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for "parts only" warranty for 15 months; a second provides full services, parts, and labor for 90 days. Follow-on agreements can provide for guaranteed response times and full service or operate on a per-call time-and-materials basis.

Hewlett-Packard also provides a set of diagnostics that function as a task of the operating system. A stand-alone set runs directly on the CPU without operating system aid. In addition, a set of microprogrammed micro-diagnostics can be executed and transmitted directly to Hewlett-Packard through a modem and common carrier line for immediate assistance on difficult problems.

Table 2. HP 3000CX Series: Basic Configurations and Options

Basic Configurations	50CX	100CX	200CX	300CX
Memory (bytes)	96K	96K	128K	128K
Disc (bytes)	5M (moving hd cartridge)	10M (moving hd cartridge)	2M (fixed hd) 47M (mov. hd pack)	2M (fixed hd) 47M (mov. hd pack)
Tape	800 bpi	800 bpi	800 bpi	800 bpi
Peripherals	— —	200-lpm printer 600-cpm reader	200-lpm printer 600-cpm reader	1,250-lpm printer reader/punch 200 cpm (30-75 cpm)
Terminal	16-port Async term controller	16-port Async term controller	16-port Async term controller	16-port Async term controller
Software	MPE/C Utilities SPL Comp. lib Trace Editor Sort	MPE/C Utilities SPL Comp. lib Trace Editor Sort	MPE/C Utilities SPL Comp. lib Trace Editor Sort	MPE/C Utilities SPL Comp. lib Trace Editor Sort
Options				
Memory (bytes)	128K	128K	—	—
Disc	Expandable	Expandable	Expandable	Expandable
Tape	1,600 bpi	1,600 bpi	1,600 bpi	1,600 bpi
Peripheral	—	Delete	Delete	Delete
Terminal	Add 202 capability	Add 202 capability	Add 202 capability	Add 202 capability
Software/Firmware*	MPET	MPET BASIC FORTRAN IV RPG Decimal Firmware, expanded floating-pt firmware	MPET Same as 100CX Plus:- COBOL IMAGE	MPET Same as 200CX
Additional Hardware			Real-time data acquisition programmable controller	

**Available in packaged combinations at various prices*

Table 3. HP 3000CX Series: Peripherals

Device Model	Description
Discs	
30103A	Fixed head; 2M bytes; 236KW/sec
30102A	Moving head; 4.9M bytes; 156KW/sec
30110A	Moving head; 47M bytes; 246KW/sec
Magnetic Tapes	
30115A	9 trk; 800 bpi; 36KB/sec
30115A-100	9 trk; 1,600 bpi; 72KB/sec
Card	
30106	600-cpm reader
30119A	Reader/punch; 200 cpm/30-75 cpm
30119A-001	Keyboard + verify
Printer	
30118A	600 lpm; 64 char set; 132 col
30118A-002	128 char set option
30128	1,250 lpm; 64 char set; 132 col
30128-001	96 char option
30127	300 lpm; 64 char; 132 col
30127-001	96 char set
Paper Tape	
30104A	Reader: 500 cps
30105A	Punch: 75 cps
Data Communications	
30032	16-port async channel
30120A	Terminal/console, 30 cps/75 col, 300 baud
30120A-001	Opt 118 col
30124A	ASR-33, 10 CPS
30123A	CRT, 72 char x 25 line, switchable data rates HP2640 Terminal
30300A	Programmable controller, based on HP 2100 mini

Table 4. HP 3000CX Series: Software

MPE/C	Multiprogramming execution, multiprogrammed batch and on-line terminal; full logical level I/O and data communications handle.
MPET	A limited subset of MPE/C oriented to environments using primarily BASIC.
Language Processors	FORTRAN, COBOL, Systems Programming Language (SPL), RPG II, BASIC (both a compiler + interpreter version)
Special Purpose	Image/3000, a data base management system; Query/3000 terminal-based query facility for Image/3000 data base
Scientific Library	A collection of various functions and transforms
Other	Diagnostics, utilities, user library

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TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	PROCESSORS AND WORKING STORAGE		
30000C	Model 50CX (includes CPU with 96K bytes of core memory; multiplexor channel (15 device capacity); async terminal controller (16 ports); system console and cabinets; mag tape unit; 5M-byte cartridge disc unit; std power with 120/208V and 3 phase/60Hz)	99,500	687
32400C	Model 100CX (same as 30000C except multiplexor channel (16 device capacity); 10M bytes of disc storage; 5M byte cartridge disc unit plus additional 5M-byte drive; 600-cpm card reader subsystem; 200-lpm dot matrix printer)	129,500	953
32401C	Model 200CX (same as 32400C except CPU with 128K bytes of core memory; 2M-byte fixed-head disc; 47M-byte moving-head disc; 600-cpm card reader subsystem; 200-lpm dot matrix line printer)	171,000	1,134
32402C	Model 300CX (same as 32401C except with 1,250-lpm printer; reader/punch subsystem)	203,500	1,263
	Processor Options		
	All Processors		
001	MPET operating system in place of MPE	NC	NC
015	System AC power option with 230V	NC	NC
100	1,600-bpi tape unit replaces 800-bpi unit	1,500	30
202	Adds 202 type data set control to async terminal controller	1,240	8
	Processor Options 50CX		
181	Increases memory to 128K bytes	10,000	34
403	Delete disc cartridge system	8,000	136
	Processor Options 100CX, 200CX		
401	Deletes 600-cpm card reader	-6,000	-66
402	Deletes dot matrix printer	-9,000	-83
600	Timeshare package	NC	40
601	Scientific package	5,000	49
602	Commercial package	5,000	44
603	Commercial and scientific package	9,000	74
	100CX and 200CX Option		
102	128-char option for line printer	500	NC
	200CX and 300CX Options		
104	Expands fixed-head disc to 4M bytes	6,600	18
	300CX Options		
102	96 character option for line printer	2,000	18
106	Keyboard and verify capability added to reader/punch	2,000	NC
404	Delete card reader/punch subsystem	-12,000	-127
405	Delete high-speed printer	-28,000	-151
604	Commercial package without data base management capability	6,000	64
605	Commercial and scientific package without data base management capability	10,000	94
	MEMORY AND CPU ENHANCEMENTS		
30011A	Expanded instruction set	3,250	19
30011A-001	Replaces extended-precision floating-point instruction set with decimal firmware instruction set	1,000	NC
30011A-002	Adds the decimal firmware instruction set to the extended-precision floating-point instruction set	2,000	NC
30414A	Field-installed memory upgrade kit (increases memory to 96K-bytes)	11,000	46
30429A	Field-installed memory upgrade kit (increases memory from 64K-bytes to 128K-bytes)	21,500	80
30431A	Field-installed memory upgrade kit (increases memory from 96K-bytes to 128K-bytes)	11,000	34
	MASS STORAGE		
30102A/015*	47M-byte disc file subsystem	32,000	216
30102A/010*	Adds drive on same controller	-12,000	-40
30103A	Fixed-head disc subsystem with 1.0M bytes of storage	20,000	148
30103A-001*	Adds 1.0M bytes of storage	3,300	36
30103A-002*	Adds 3.0M bytes of storage	9,900	54
30110A/015*	Cartridge disc subsystem	15,000	136
30110A-010*	Adds additional 7900 drive (5M bytes)	-5,025	-19
	INPUT/OUTPUT		
	LINE PRINTERS		
30118A/015*	200-lpm subsystem (132 col; 64 char)	9,750	83
30118A-001*	128 char set	500	NC
30127A/015	300-lpm subsystem with 136 col and 64 char	13,500	135
30127A-001*	96 char set	2,000	NC
30128A/015*	1,250-lpm subsystem with 132 col and 64 char	36,000	151
30128A-001*	96 char set	2,000	NC
	PUNCHED CARD		
30106A/015*	Card reader subsystem: 600 cpm	7,160	66
30107A/015*	Card reader subsystem: 1,200 cpm	18,540	126
30107A/001*	Adds double read station	2,575	2
30119A/015*	Card reader/punch subsystem: reads 200 cpm, punches 75 cpm	13,500	127
30119A-002*	Adds off-line keyboard punch and verify capability	2,000	NC
	MAGNETIC TAPE		
30115A	Includes 2,400 ft of tape and cabinets; 9 channel, 800 cpi, 45 ips; includes controller interface. Handles up to four 9-channel mag tape units - one 30115A and mixture of up to three additional units (i.e. either 30115A-200's, 30115A-300's, or 30115A-400's)	12,000	93
30115A-100*	9 channel, 1,600 cpi, 45 ips. Includes controller interface, handles up to four 9-channel mag tape units	1,500	30
30115A-200*	Adds an additional 800 cpi, 45 ips, 9-channel drive	-2,450	-22
30115A-300*	Adds a 9-channel, 1,600 cpi, 45 ips, master drive	-975	8
30115A-400*	Adds a 9-channel, 1,600 cpi, 45 ips, *slave* drive	2,500	NC
	PAPER TAPE		
30104A	Cabinets + controller interface included; paper tape reader subsystem (500 cps)	3,350	32
30105A	Paper tape punch subsystem (75 cps)	4,225	52
	TERMINALS		
30120A/015*	Printer Terminal (30-cps, 75-col keyboard, and pin feed with paper guide; w/o pedestal)	4,920	38
30120A-001*	Adds 118 col facility and replaces pin feed with tractor mechanism; vertical tab/form feed, horizontal tab, and pedestal included	1,135	NC
30120A-003*	Friction feed replaces pin feed; with pedestal	NC	NC
30120A-015*	230V/30Hz ac power option	220	NC
30122A/015*	Character-mode CRT (2615A)	2,835	36
30124A	Teletype terminal (10 cps ASR-33)	2,650	68
30124A-015*	230V/50Hz ac power option	200	NC
	EXPANDED I/O CAPABILITY		
30030A	High-speed selector channel	6,080	13
30032B	Async terminal controller (Note: Option 001 or 002 must be ordered)	3,000	18
30032B-001*	For 103 type modems only	1,240	8
30032B-002*	For 103 and 202 type modems	2,480	16
	ADDITIONAL DEVICE INTERFACES		
30126A	CalComp plotter interface for 500 Series plotters	1,030	5
30300A/015*	Programmable controller with 8K of memory	18,000	207
30361A	Programmable controller interface kit	5,000	8
	REAL-TIME CAPABILITY		
30301A/015*	Real-time programmable controller (includes HP 2100S computer with 8K-words of memory, DMA, programmable time-base generator, hardware extended arithmetic and floating-point instructions; paper tape reader; teleprinter; interconnection interfaces; signal cable, cabinets; software	23,000	NA
30361A-001*	Option to the programmable controller interface kit replaces BCS/3000 software with the RTE C/3000 software	+2,000	NA
	DATA COMMUNICATION		
30130A	2780/3780 Emulation Subsystem	3,500	30
30441A	Adds 202 modem support to async term controller	1,500	8

*indicates option number
NA-information not available

HEWLETT-PACKARD CO.
HP 3000 Report Update

SAS/3000

Hewlett-Packard's Student Assignment System (SAS/3000) software package for the HP 3000 minicomputer allows school administrators to build master schedules, assign students to classes and interactively maintain school and student files.

As part of the TOADS (Terminal Oriented Administrative Data System) software system, SAS/3000 compares a manually developed master schedule to student course requests and then produces class schedules based on school-defined priorities. Individual student course requests can be entered on-line and scheduled without rescheduling all the other students. The system is designed for use in junior, senior and vocational high schools.

The HP Mini Data Center equipped with SAS/3000 is also available to students, teachers and school personnel for general problem solving and administrative tasks. The one-time software license charge is $9,500 and a HP 3000 minicomputer with SAS/3000 ranges in price from about $100,000 to $200,000.

MEDIUM SPEED PRINTER

Hewlett-Packard has announced a new medium-speed printer, designated Model 30133A when used with the HP 3000CX minicomputer.

Print speed is 600 lines per minute with a 136-column line and a 64-character set. A 96-character ASCII drum is optional; print speed is reduced to 436 lines per minute.

Business forms of up to six parts can be handled by the printer, with vertical spacing controlled by a 12-channel tape. Control tapes allow slewing up to 15 lines. Either six or eight lines per inch are switch-selectable.

Purchase price for the printer is approximately $19,000 including controller, depending on the options selected. Deliveries began in September 1975.

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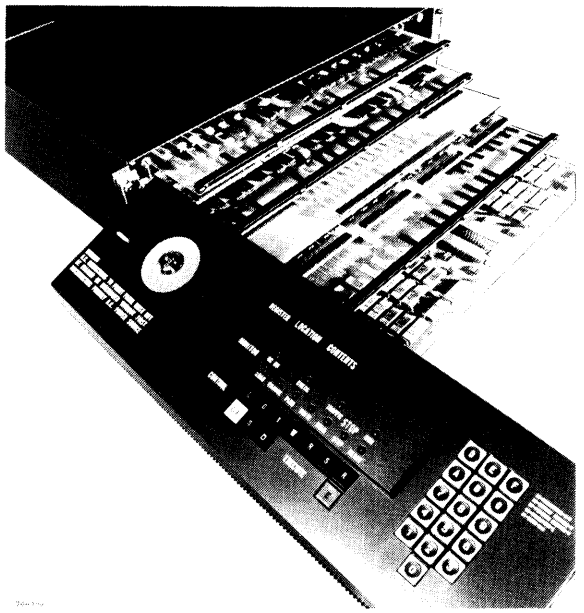
HONEYWELL INFORMATION SYSTEMS

Level 6 System Report



Honeywell Level 6/36, 65K Words of Memory, 4-Peripheral Controller, and 8-Line Communications Controller

OVERVIEW

The Honeywell Level 6 currently consists of three models: the 6/06, 6/34, and 6/36. All models are based on the same 16-bit-word microprogrammed processor and are specifically aimed at the OEM market. The Model 6/06 includes firmware to emulate Honeywell's System 700 and a bus adapter to convert the system bus to the same System 700 I/O interface. Thus, Model 6/06 can run all the System 700 software and use all the System 700 peripherals. Models 6/34 and 6/36 implement an entirely different instruction set than the 6/06 implements. Table 1 summarizes the mainframe characteristics of the 6/06 and 6/30 Models.

The Level 6 processor utilizes a central bus architecture implemented in T^2L bipolar logic. The central processor, memory modules, and peripheral device controllers all communicate with each other in a master-slave relationship over the system bus, which is called the "Megabus." Cycle time of the Megabus is 300 nanoseconds for each word transferred.

Memory for Level 6 interfaces to the Megabus via memory controllers. Each controller can support up to four 8K-word memory modules and each requires one Megabus slot. Memory is designed using n-channel MOS 4K-bit dynamic RAMs. Cycle time is 650 nanoseconds per word. A byte parity memory with 16 data bits and two parity bits is standard; memory with Error Detection And Correction (EDAC) — 16 data bits and six detection bits — is optional. The Memory Save and Auto Restart option can retain memory contents for 2 hours when main power is down.

Maximum memory capacity is currently 32K words for Model 6/34 and 65K words for Model 6/36. The Megabus, however, can carry 24 address bits; thus, future Level 6 models could address up to 8M words (16M bytes) of memory.

All peripheral devices connect to a Megabus slot via controllers. All controllers except the DMA interface for user-designed devices include a microprocessor and memory. Four types of I/O interfaces are available:

- Multiple Device Controller supports four slow-speed devices (card reader, line printer, serial printer, Teletypewriter, diskette, TTY-compatible display).
- Mass Storage Controller supports up to four cartridge disc units (2.5-million to 40-million-byte capacity); maximum throughput is 312K bytes per second.
- Multiline Communications Controller interfaces to multiple asynchronous or synchronous lines — eight full-duplex low-speed lines (300 bits per second or less) or medium-speed lines (600-10,800 bits per second) or four broadband lines (up to 72,000 bits per second) — with an aggregate throughput up to 160,000 bits per second.
- General-Purpose DMA Interface supports one user-designed device; maximum transfer rate between memory and device is 500,000 words per second.

Peripheral devices interface to the standard controllers via Device-Pacs, each one designed for a specific device. Each controller requires only one slot on the Megabus, and each controller provides DMA block transfer facilities for the interfaced devices.

HEADQUARTERS

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Table 1. Honeywell Level 6: Mainframe Characteristics

Characteristic	Level 6/06	Level 6/30
CENTRAL PROCESSOR		
Microprogrammed	Yes	Yes
No. of Registers	7	18
Addressing Word Length	16 bits (1)	16 bits (1)
Direct	1K words (2)	64K words
Indirect	Multilevel (2)	Single level
Indexed	Yes, pre and past (2)	Yes
Mapping	No	No
Instruction Set		
Implementation	Firmware	Firmware
Types	Single-word/double-word	Single-word/double-word
Fixed-Point		
Add/Subtract	4.1	4.1
Multiply	11.2	11.2
Divide	13.2-14.5	13.2-14.5
Floating-Point	NA	NA
Writable Control Store	NA	NA
Interrupt Levels	63	64
Stack Operations	Limited	Yes
MAIN MEMORY		
Type	nMOS RAM	nMOS RAM
Word Length	16 + 2 parity/16 + 6 EDAC	16 + 2 parity/16 + 6 EDAC
Cycle Time (nsec)	650	650
Basic Addressable Unit	Word	Word or byte
Bytes/Access	2	2
Cache Memory	No	No
Capacity (bytes)		
Min	16K	16K
Max	65K	128K
Increment Size (bytes)	16K	16K
Ports/Module	1	1
Error Checks	Parity, std; EDAC, opt	Parity, std; EDAC, opt
Memory Protection	Memory lockout opt	NA
Memory Save	Opt	Opt
Memory Management	No	No
Interleaving	No	No
INPUT/OUTPUT	6/06	6/30
Maximum Addressable Devices	64	1,024
Programmed I/O	Software dependent	Control words only
Megabus Transfer Rate (bytes/sec)	6M	6M
Max DMA Transfer Rate (bytes/sec)	1M (3)	.8M-1M
Multiplexed I/O	Sys 700 DMC (3) and DMA	Via device controllers

Notes:

(1) By instruction. Megabus has 24 address bits; thus it can address 16M words of memory.
(2) The Level 6/06 has all the System 700 addressing modes, which are upward compatible with the older Series 16 addressing.
(3) The Level 6/06 is designed as an OEM version of the System 700; thus it supports only the System 700 peripheral devices.

The Megabus has up to 23 slots to connect memory, DMA, multi-device, or multiline communications controllers.

The central processor implements a standard set of 107 instructions. Although fixed-point arithmetic uses single-precision (one-word) operands, bit, byte and double-word instructions are also available. A bit can be set, reset, or swapped. Bytes can be loaded and stored and logical operations can be performed on them. Double words can be loaded into registers or stored in memory. Multiply and divide are included in the instruction set. Hardware floating-point arithmetic is not available.

The CPU uses 18 internal addressable registers that are used to implement eight modes of addressing, multiple accumulators, and indexing. The processor also implements 64 interrupt levels.

The Model 6/34 includes the processor, in a four-slot Megabus chassis, memory controller with parity, an 8K-word MOS Memory-Pac, multiply/divide, real-time clock, and ROM bootstrap loader. The processor requires one Megabus slot. The memory controller, which also requires one Megabus slot, can support three additional Memory-Pacs. Two slots are left in the four-slot chassis to attach peripheral devices and communications lines. Options include the controllers, Level 6 peripherals, full control panel, Memory Save and Auto Restart, watchdog timer, peripheral power supply, cabinetry, and accessories.

The Model 6/36 includes the processor, in a five- or 10-slot Megabus chassis that can be expanded to 23 slots, a full control panel, multiply/divide hardware, real-time clock, ROM bootstrap, and power supply. Options include the peripheral controllers, Level 6 peripherals, memory controllers and Memory-Pacs with parity or EDAC for up to 64K words, Memory Save and Auto Restart, watchdog timer, and basic control panel (for the five-slot chassis only).

Peripherals

The following peripherals are available for the Level 6/30 models:

- Card readers — 300 to 500 cards per minute, 80-column punched cards and 40- or 80-column marked cards.
- Keyboard typewriter console — 30 characters per second, 64-character ASCII set, 132 columns, 10 characters per inch.
- Teleprinter consoles — ASR/KSR-33 models.
- CRT keyboard console — display of 12 lines, 80 characters per line, 64-character set; keyboard can generate 128 ASCII codes, 60 encoded keys, and N-key rollover.
- Serial printers — 165 characters per second, 64- or 96-character ASCII code, 132 columns per line, original plus four copies.
- Printers — 240, 300, 480, or 600 lines per minute, 136 columns per line, 64- or 96-character set, ASCII code, 6 or 8 lines per inch.
- Diskettes — one to four diskettes, single or dual diskette units, 256,256 bytes per diskette, 26 sectors per track, 128 bytes per sector, 77 tracks, compatible with IBM 3740.
- Cartridge disc units — one to four units of 2.5M to 10M bytes each for a total capacity of 40M bytes; units with removable cartridge only or one fixed and one removable cartridge, 100 or 200 tracks per inch; average random access time is 50 milliseconds; transfer rate is 156K words per second.

SOFTWARE

Two software packages are available: GCOS/BES 1 and GCOS/BES 2. Both provide executive modules for control of on-line, interrupt-driven system operation with task scheduling, input/output control featuring device-independence, timing of tasks, and trap handling. The executive modules require no peripherals other than an input unit, such as diskette, cartridge disc or paper tape, from which modules are loaded. Both GCOS/BES 1 and BES 2 provide program development modules that support an assembler, FORTRAN compiler, editor, command processor, linker, and utilities.

The GCOS/BES 2 package is a superset of BES 1. The BES 2 package includes a communications module that supports the Multiline Communications Processor for synchronous line control including IBM BSC/2780 communications support and asynchronous line control. The module is designed to allow users to insert communications software for user-developed terminals and protocol handlers.

Competitive Position

In 1970, Honeywell occupied the number three position in the minicomputer market; only Digital Equipment Corporation and Hewlett-Packard had more minicomputer systems installed. At that time, however, only 22,000 minicomputers had been installed; about 2,000 of them were Honeywell systems. In 1972, when Honeywell introduced the System 700, based on a new 716 CPU, the company announced the integration of its minicomputer line into its data processing division. Minicomputers would be sold as part of computer installations that included medium- or large-scale Honeywell computers.

Although logical on the surface, this approach ignored the nature of the minicomputer market, which has been separate from the commercial data processing market. Only now are minicomputers beginning to compete with general-purpose systems. In the period since 1972, Honeywell missed out on the steady growth in the minicomputer field even though a company spokesman claimed the company sold $80 million worth of minicomputers in one form or another in 1975. When Honeywell essentially pulled out of the minicomputer market in 1972, Prime Computers built and marketed its Prime Series, which are peripheral- and software-compatible with Honeywell's Series 16 (Honeywell's System 700 is the remaining member of that line). Prime Computers not only filled the Series 16 vacuum, but the company has continued to produce upward-compatible, high performance, real-time and timesharing systems. Level 6/06 is apparently designed to make the System 700 cheaper as an OEM product. It should appeal only to current Honeywell customers. Other OEMs would have no reason to choose it over a Prime Computer, which has substantive systems to upgrade into.

The Level 6/30 Models are the systems Honeywell has designed for reentry into the minicomputer market. They use a totally new architecture (for Honeywell) based on the central Megabus, which is similar to the Unibus of Digital Equipment's PDP-11. So Honeywell stands in the same position as any other newcomer in the minicomputer market; the traditional way companies have entered that market is via OEM. The end-user market requires a customer base to sell to and the quickest way to get that base is via OEMs, who will sell systems incorporated in a product.

The OEM market is very competitive. Furthermore, Data General, Digital Equipment, General Automation, Digital Computer Controls, Computer Automation, and other manufacturers are quite well established in that market. Table 2 shows that the Level 6/30 is performance competitive with the Nova 3, PDP-11/35, and GA-16/330. It is very well priced in comparison to the PDP-11/35, but it is more expensive for small configurations than both the Nova 3 and GA-16/330. It is less expensive than the Nova 3 for larger systems. All three systems offer much more software than is available with the Level 6.

Honeywell has been building a special sales staff to sell the Level 6 minicomputers. It consists mainly of experienced minicomputer salesmen who have sold for other companies. They will need to be good to compete against a Data General salesman and the Nova 3, for example. Reentering the OEM minicomputer market with a system that is not substantially better and lower in cost than those of major competitors will be difficult. Honeywell will probably need to squeeze the price more, up the performance, and add more software before the Level 6 is serious competition.

Table 2. Honeywell Level 6/30 Compared with OEM Competitors

	Honeywell 6/30	Data General Nova 3	Digital Equipment PDP-11/35	General Automation GA-16/330
Word Length (bits)	16 + 2 Parity/ 16 + 6 EDAC	16/16 + 2 Parity	16/16 + 2 Parity	16/16 + 2 Parity
Instruction Times (μsec)				
Add	4.1	1.8	2.7	4.6
Multiply	11.2	6.9 (1)	9.7	21.2
Divide	13.2 to 14.5	7.5 (1)	11.3	20.3
Floating-Point Add	Subroutine	7.7*	18.8*	*
Floating-Point Multiply	Subroutine	11.3*	29.0*	*
Floating-Point Divide	Subroutine	13.7*	46.7*	*
Max Memory (bytes)	64K/128K	64K/256K	124K	128K
No. of GP Registers	7118	4	9	16
Max DMA Rate (bytes/sec)	6M	2M	2M	2M
Price, $				
CPU + Memory				
32K bytes	5,570	4,400	11,495	5,250
64K bytes	8,790	7,100	20,495	8,250
128K bytes	17,000	22,700	32,245	NA
256K bytes	NA	37,500	44,220 (2)	—

*Opt, at extra cost

Notes: (1) Operands are unsigned integers on std.
(2) Maximum memory consists of 248K bytes.

PRICE DATA

Model Number	Description	Purchase $	Monthly Maint. $	6/06	6/34	6/36
	CENTRAL PROCESSOR SYSTEMS (CPS)					
	Each 6/30 is rack mountable or freestanding and includes: • Megabus Chassis with Power Supply • Multiply/Divide Hardware • Real Timer Clock • ROM Bootstrap Loader for keyboard console, diskette, & card reader					
CPS9450	6/34 Processor in 4-Slot Megabus Chassis including basic control panel, memory controller with parity, and an 8K-word Memory-Pac. Can add up to 3 more 8K-word Memory-Pacs (CMM9001) for 32K-word max.	3,990	60		X	
CPS9460	6/36 Processor in 5-Slot Megabus Chassis including full control panel. Memory controller and 8K-word Memory-Pacs must be ordered separately, up to 64K-word max.	3,200	40			X
CPS9461	Same as CPS9460 except in 10-Slot Megabus Chassis	4,100	42			X
	GENERAL OPTIONS					
CPF9401	Watchdog Timer	400	3		X	X
CAB9401	4-Slot Megabus Expansion Chassis with Power Supply	1,900	8			X
CAB9402	9-Slot Megabus Expansion Chassis with Power Supply	3,000	10			X
GIS9001	General-Purpose Interface	900	4		X	X
	MOS RAM Memory					
CMC9001	Memory Controller with Parity including 8K-word Memory-Pac (CMM9001); can add up to 3 more 8K-word Memory-Pacs	2,400	24	X		X
CMM9001	8K-Word Memory-Pac with Parity	1,600	10	X	X	X
CMC9002	Same as CMC9001 except with EDAC instead of parity	2,800	28	X		X
CMM9002	8K-Word Memory-Pac with EDAC	1,800	12	X		X
PSS9001	Memory Save for up to 64K words with Auto Restart (tabletop model)	700	6		X	X
	PERIPHERALS					
MDC9101	Multiple Device Controller	1,200	10		X	X
KCM9101	Device-Pac for Keyboard Console	200	5			
DIM9101	Device-Pac for Diskette	500	5			
CRM9101	Device-Pac for Card Reader	400	7			
PRM9101	Device-Pac for Printer	400	6			
TTU9101	ASR-33 Teletypewriter Console	1,600	48			
DKU9101	CRT/Keyboard Console, 64-char set	1,400	21			
TWU9101	30 CPS Keyboard Typewriter Console (KSR)	2,300	26			
DIU9101	Single Diskette, rack mountable	1,700	17			
DIU9102	Dual Diskette, rack mountable	2,800	28			
CRU9101	300 CPM Punched Card Reader	3,500	41			
CRF9101	51-Col Card Option	600	7			
PRU9101	60 LPM Serial Printer, 64-char set	5,100	40			
PRU9104	300-LPM Printer, 64-char set	8,700	60			
PRU9106	600-LPM Printer, 64-char set	16,000	140			
	MASS STORAGE DEVICES					
MSC9101	Mass Storage Controller	2,800	16	X	X	
CDM9101	Device-Pac for Cartridge Disc	1,200	12			
CDU9101	Cartridge Disc Drive, Low Density, for 1 removable disc (1.25M words)	5,700	50			
CDU9102	Cartridge Disc Drive, Low Density, for 1 removable and 1 fixed disc (2.5M words)	7,800	60			
CDU9103	Cartridge Disc Drive, High Density, for 1 removable disc (2.5M words)	7,400	60			
CDU9104	Cartridge Disc Drive, High Density, for 1 removable and 1 fixed disc (5M words)	8,500	80			
	COMMUNICATIONS					
MLC9101	Multiline Communications Processor with Communication-Pacs for 8 async lines up to 9.6KB each, with cables	3,400	26	X		X
	Each 6/06 CPS includes: • 6/06 Processor with high-speed arithmetic/base sector relocation and real-time clock • Megabus Chassis with Power Supply • S700 Bus Interface					
CPS9220	6/06 CPS in 5-Slot Megabus Chassis mounted in 60-in cabinet with all panels and doors (includes Memory Save for up to 64K words, with Auto Restart, power distribution unit, and any required S700 expansion drawers and add-on cabinets); memory controller and 8K-word Memory-Pacs must be ordered separately.	5,500	60	X		
CAB9010	Extension Table Wing	250	NC			
GIS9002	Additional S700 Bus Interface	850	13	X		

OVERVIEW

System 700 is a line of general-purpose minicomputers, which are marketed primarily as components of a large data processing network. The 700 offers good I/O and interrupt facilities, a broad range of peripherals, and well-integrated software. Both hardware and software place emphasis on the real-time processing required for process control, data collection, and data communications environments.

The three models currently being offered for the 700 Series are all based on the 716 processor first announced in 1972. The 716 uses a 16-bit word, and memory cycle time is 775 nanoseconds per word. The models have letter suffixes indicating function: G for "general-purpose," S for "sensor-based," and "M" for rack-mounted version targeted at system builders who want to use their own cabinets. The 725-G/735-G General-Purpose System, the 725-S/735-S Sensor-Based System, and the 725-M Rack-Mounted System comprise the newest system offerings.

Standard features for the G and S systems are high-speed arithmetic, real-time clock, and 8K-word memory boards that allow memory to be extended to 64K words within the main processor chassis. Table 1 lists mainframe characteristics.

Peripherals available for the 700 Series include a wide variety of low-speed, mass storage, and special subsystems. Table 2 lists peripherals.

One strong point of the 700 Series is its data communications capability. There are several special-purpose "Datanet" 700 communications systems based on the 716 processor. These Datanet systems are designed to provide minicomputer-controlled remote batch processors, concentrators, and distributed processors that can be configured into a large network controlled by Honeywell or IBM computers. The equivalent of Datanet systems can be configured with 725-G/735-G systems, using RJE (HASP II) or the RCP 707 systems software packages.

Operating system support is provided by OS/700, a modular real-time, multiprogramming system that provides computer-to-computer communication, priority-oriented task scheduling, and centralized control of all system resources. OS/700 is available in both core-based (COS) and disc-based (DOS) versions. The FORTRAN IV compiler, BASIC interpreter, and Assembler can run under OS/700 or can operate in a free-standing environment. Host-resident software systems allow program development on other Honeywell or IBM computers. In addition, OS/700 can support extensive communications facilities and a file management package. Since the RJE (HASP II) and RCP 707 system software packages are also available, a user could implement a Datanet system from a 725 or 735, given the proper configuration. Table 3 lists software configuration requirements.

Table 1. Honeywell System 700: Mainframe Characteristics

Central Processor	
Type (microprogrammed)	No
Control Memory (RAM, ROM)	—
Size	
Use	
No. of Internal Registers	2 general-purpose, 1 index register; alternate index register
Addressing	
Direct (no. of words)	1,024(1)
Indirect	Multilevel
Indexed	Yes
Instruction Set	
Implementation (hardware, firmware)	Hardware
Number (std, opt)	78 std, 4 opt
Decimal Arithmetic	No
Floating-Point Arithmetic	By subroutine
User Microprogramming	—
Priority Interrupt System Operation Modes Levels	3-48
Main Storage	
Type	Core
Cycle Time (μsec)	0.775
Basic Addressable Unit	16-bit word
Bytes per Access	2
Cache Memory	No
Min Capacity (bytes)	16K(2)
Max Capacity (bytes)	128K
Increment Size (bytes)	16K
Ports per Module	1
Error Checks	Parity (opt)
Protection Method	Memory lockout (opt)
Memory Management	—
ROM	
Use	Loaders
Capacity (bytes)	256-2,048 words
I/O Channels	
Programmed I/O	Yes
DMA Channels	Yes (no limit)
Multiplexed I/O (no. of subchannels)	DMC optional (8)
Max Transfer Rate	
Within Memory (wds/sec)	321,500
Over DMA (wds/sec)	1,290,000
Simultaneous Operations	None, except multiple peripherals with processing

Notes:
(1) Base sector and current sector; base sector is optionally relocatable.
(2) OS/700 requires 32K bytes of memory for a program development system. Execute-only systems can be configured with as little as 16K bytes of memory.

Relationship to Other Honeywell Products

The 700 line has undergone a number of evolutionary changes and reorganizations; most of these represent changes in pricing (getting more for less) and marketing (model numbering, definition of "BASIC" systems) coupled with some engineering developments (8K-word memory boards). The current 725-6/735-G General-Purpose System, for instance, directly replaces the 720/01 Terminal System and the 720/02 Peripheral System as well as retiring the 720/03 Multipurpose System and the

Table 2. Honeywell System 700: Peripherals

Fixed-Head Disc—64K, 128K, 256K, and 512K wds on 16, 32, 64, and 128 trks, respectively; avg access time, 12.5 msec; transfer rate, 82K wds/sec.
Removable-Head Disc—6 drives with capacities of 0.9M to 7.2M wds; 7.5M wds; 1.1M wds; 1.8M wds; 3.7M wds; and 7.5M wds.
Magnetic Tape—tape cassette system; 6 subsystems including 7-trk and 9-trk units, with 200-, 556-, 800-, and 1,600-bpi densities.
Printers—9 printers at 200, 300, 450, 650, 950, and 1,100 lpm; 96, 120, and 136 cols; 64 and 96 char sets.
Punched Card—readers at 300, 600, 800, and 1,050 cpm; punches at 400-1,000 cpm; reader/punches at 400 cpm read, 100-400 cpm punch.
Paper Tape—reader at 300-cps max transfer rate, 8-level tape; punch at 110-cps max transfer rate, 8-level tape.
Teletype—ASR 33, KSR 33, ASR 35; ASR includes paper tape reader/punch.

Table 3. Honeywell System 700: Software Configuration Requirements

Operating System	Configuration Required
OS/700	
DOS (disc-based)	716 processor, 16K-wd main memory, 1 disc with 128K wds/min, 1 programmed I/O device
COS (core-based)	716 processor, 24K-wd main memory, 1 programmed I/O device
BOS (Batch Operating System)	716 or 316 processor; 12K-wd core memory, 0.9M-wd disc storage, ASR 33 Teletype
OP-16 Real-Time Operating System	716 or 316 processor, 4K-wd main memory, real-time clock, ASR 33 or 35 Teletype

720/05 Batch Processing System, both of which were based on the H316 processor. The current 725-S/735-S directly replaces the 720/20 Sensor-Based System and the 720/21 Extended Sensor-Based System. Both the new G and S systems include as standard features several 720/xx options such as high-speed arithmetic and real-time clock; also both use only 8K-word memory boards, allowing 64K words of memory to be stored within the main processor chassis.

The 716 processor that serves as the foundation for the 700 Series is architecturally similar to the earlier 316 and 516 models. The 716 instruction set includes the 316 and 516 instructions as subsets. Since all 16 Series peripherals can attach to a 716 with the aid of the DMC adapter option, program compatibility is completely maintained given the same environments. In addition, all 316 and 516 programs can run on the 716. The OP-16 and BOS operating systems developed for the 316 are also available in 716 versions for users who want to run 316 programs on a 716.

The 716 processor has stack-register and register-addressing features unavailable on the Series 16 processors. These features include standard DMA channel, a complete line of data communications hardware, a new real-time operating system (OS/700), and host-resident software. In addition, the 716 is 20 percent faster than the DDP-516 and over twice as fast as the H316.

System 700 models can duplicate all of the major Series 16 systems except the 1640 Timesharing Systems. Honeywell currently has no plans to upgrade the time-sharing systems to use the 716 processor.

COMPETITIVE POSITION

Honeywell is not marketing the 716 processor chiefly as a minicomputer or as an upgrade to the Series 16 processors. The system is marketed by the commercial data processing sales force, which is concerned with the total computer network, so System 700 configurations are sold as component parts of that network.

The Series 16, forerunners of the 700 Series, were strong competitors in the minicomputer field. Unlike Digital with its PDP-11 line, Honeywell did not change the architecture of the 716 processor from that of the older Series 16 line. This evolutionary path to computer development protects the Series 16 users' software and peripherals, and provides the 716 system for upgrading.

The System 700 models span the breadth of the major part of the minicomputer market, including most of the OEM segment. System 700 is offered unbundled for the OEM market; contracts for the system are negotiated with the home office. There is no equivalent to the smaller, slower board-level "microcomputers" that manufacturers like General Automation and Digital are adding at the bottom end of their lines, mostly for OEM applications. Moreover, Honeywell has not added a memory mapping option to extend the line into the larger 128K- and 256K-word systems available from manufacturers like Hewlett-Packard and again Digital and General Automation, plus Interdata and Modular Computers.

The sensor-based systems compete directly with the IBM System/7, 1130 and 1800, CDC 1700, Xerox Sigma 3, and Digital PDP-11 for data acquisition, manufacturing, and process control applications. General-purpose models compete both as business minis and as terminal control systems. As such, they are directly competitive with such intelligent terminal systems as MODCOMP I and III; Four-Phase System IV/70; and, in some cases, IBM System/3. These systems are designed for data collection and limited processing from terminals in banks, factories, and laboratories.

Honeywell's advantage in this market is that customers can obtain a total distributed processing network from a single supplier. Univac offers this capability, but IBM has refrained from embracing this type of distributed systems concept, stressing instead large centralized systems. As a result, independents have developed the distributed processing idea — and Honeywell's 716-based HASP II RTE package directly competes in the general intelligent terminal market geared toward IBM computers.

The System 700's most direct competitor is PRIME Computer's PRIME 100, 200, and 300, which are program and peripheral compatible with the Honeywell Series 16

line. The PRIME computers utilize MSI and LSI technology plus all MOS memories. They offer many enhancements over the Series 16, including a substantial upgrade capability to the midi-range PRIME 300. Honeywell's shift of emphasis away from the minicomputer market to the network market has the advantage of consolidating its computer lines, but it has also left a vacuum in the minicomputer market that PRIME has moved to fill.

Configuration Guide

All 700 Series systems are based on the 716 processor. The 725 configurations have software and support separately priced, while the 735s have these items bundled. Basic configurations are as follows:

- 725-G/735-G General-Purpose System — includes 716 processor in a 60-inch cabinet with control panel, real-time clock, multiline priority interrupt system with 3 levels implemented, power fail/auto restart, hardware multiply/divide, base-sector relocation, and 8K words of core; a teleprinter is also part of the basic configuration.
- 725-M Rack-Mounted System — for system builders who want to use their own cabinets; identical to 725-G, but no cabinet and power distribution unit.
- 725-S/735-S Sensor-Based System — includes 716 processor with control panel, real-time clock, watchdog timer, multiline priority interrupt system with 3 levels implemented, power fail/auto restart, hardware multiply/divide, base sector relocation, analog/digital subsystem controller capable of holding 8 digital and 8 analog pages (1 digital page is implemented), 8K words of core, and 2 cabinets; a teleprinter is also part of the basic configuration.

Processor options include parity, an additional crystal-controlled clock, watchdog timer (for the 725-G/735-G), 512 to 2,048 words of ROM, the communications controller, and a wide variety of peripherals. Memory can be expanded to 64K words, but expansion over 32K requires an extended memory controller that slows memory cycle time to 855 nanoseconds for the first 32K words and to 1,030 nanoseconds for memory above 32K. Memory is added in 8K-word increments with all eight modules housed in the system cabinet.

DMA and programmed I/O channels are standard to all systems. An optional Direct Multiplex Control (DMC) adapter can be added in order to attach a maximum of eight controllers from the Series 16 line of peripherals.

A Binary Synchronous Down-Line Load Option (2,048-word ROM) and other communications devices can be attached to either processor. Only the 725-S/735-S, however, can handle the real-time interface for sensor-based applications.

Compatibility

The 716 instruction set includes the H316 and DDP-516 instruction set as a subset. An optional DMC adapter for the 716 allows connection of the H316 and DDP-516 peripherals that transfer data via a DMC unit.

Honeywell has introduced new peripherals that encompass all the other peripherals used with the H316 and DDP-516. As a result, virtually all software developed for the H316 and DDP-516 can run on the 716. The 716 processor has features that are unavailable for the H316 and DDP-516, so any 716 software using the new features cannot run on the other two processors.

MAINTENANCE AND SUPPORT

Honeywell provides world-wide marketing support, including several hundred local offices for its Field Engineering Division. An emergency network provides service 24 hours a day, 7 days a week.

For the System 700, Honeywell has trained its commercial data processing field support staff to furnish the applications-oriented service required by minicomputer users. Recently, this support has been further enhanced by the opening of nine more new service centers. The total solution approach and the level of support should appeal to a wide range of customers.

HEADQUARTERS

Honeywell Information Systems
Computer Controls Division
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TYPICAL PRICES

Model Number	Description	Monthly Rental $ Short Term	Monthly Rental $ 3 yr.	Purchase $	Monthly Maint. $
	CENTRAL PROCESSOR AND WORKING STORAGE				
	(includes a 716 CPU, real-time clock, auto restart, high-speed arithmetic/base sector relocation, cabinets, and drawers; memory must be ordered separately)				
725-G	General-Purpose Minisystem (with separately priced support)	260	240	7,600	40
725-S	Sensor Based Minisystem (with separately priced support)	625	570	16,700	85
725-M	Modular General-Purpose Minisystem (with separately priced support)	NA	NA	6,000	40
735-G	General-Purpose Minisystem (with bundled support)	393	362	11,800	40
735-S	Sensor Based Minisystem (with bundled support)	758	692	20,900	85
	Memory and CPU Options for Models 725 and 735				
700-1209	8,192 Words of Main Memory (excludes parity)	115	105	3,200	30
700-1210	8,192 Words of Main Memory (with parity)	120	110	3,400	30
700-1220	256-Word ROM (for customer-supplied programs)	—	—	840	18
700-1222	1,024-Word ROM (for customer-supplied programs)	—	—	1,260	18
700-2022	Extended Memory System (for over 32K words of main memory; Model 735 only)	110	100	2,520	20
700-3000	Real-Time Clock/Watchdog Timer	26	23	720	5
700-3010	Direct Multiplex Control Adapter (for max of 8 controllers)	94	85	2,650	18
700-3030	Binary Sync Down-Line Load Option (2,048-word ROM)	53	47	1,480	10
	MASS STORAGE				
700-4510	Fixed-Head Disc Subsystem (64K words; includes control)	347	313	9,825	40
700-4511	Fixed-Head Disc Subsystem (128K words; includes control)	490	442	13,860	55
700-4512	Fixed-Head Disc Subsystem (256K words; includes control)	620	560	17,385	75
700-4513	Fixed-Head Disc Subsystem (512K words)	925	835	25,960	110
700-4710	Removable Disc Storage Subsystem (1.1 million words; Model 735 only)	655	590	18,000	95
700-4720	Removable Disc Storage Subsystem (7.5M words)	1,830	1,220	35,800	180
700-4721	Additional Disc Pack Drive (7.5M words)	1,505	1,005	29,500	125
700-4740	Removable Disc Storage Subsystem (1.1M words)	480	434	12,515	101
700-4741	Removable Disc Storage Subsystem (1.8M words)	575	525	15,000	120
700-4742	Removable Disc Storage Subsystem (3.7M words)	765	695	20,000	160
700-4743	Removable Disc Storage Subsystem (7.5M words)	1,115	1,010	29,000	200
	INPUT/OUTPUT				
	Magnetic Tape				
700-4041/51	Mag Tape Subsystem (7/9-track, 26 ips); includes control and 1 tape unit (add up to three 700-4042 units)	355	325	10,000	95
700-4042/52	Additional Mag Tape Unit for 700-4041	245	225	7,000	70

TYPICAL PRICES (Contd.)

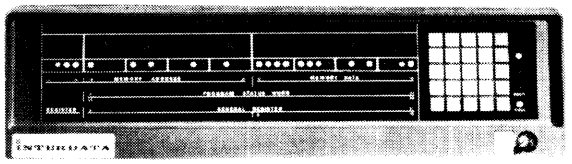
Model Number	Description	Monthly Rental $ Short Term	Monthly Rental $ 3 yr.	Purchase $	Monthly Maint. $
700-4150	Mag Tape Subsystem (9-track, 36 ips)	640	426	12,500	145
700-4180	Mag Tape Subsystem (35 ips, 1,600 bpi)	565	515	15,300	150
700-4190	Mag Tape Subsystem (70 ips, 1,600 bpi)	590	540	17,000	160
	Cassettes				
700-5400	Cassette Tape Subsystem	146	133	3,575	35
700-5401	Additional Cassette Drive for 700-5400	38	35	925	10
	Paper Tape				
700-5010	Reader with Control (300 cps)	114	104	3,200	22
700-5210	Punch with Control (110 cps)	118	107	3,300	20
	Punched Card				
700-5100*	Reader Subsystem (300 cpm)	184	164	6,000	40
700-5123	Reader Subsystem (600 cpm)	327	296	6,000	85
700-5121	Reader Subsystem (800 cpm)	378	342	9,000	86
700-5122	Reader Subsystem (1,050 cpm)	429	388	10,000	113
700-5140	Reader/Punch Subsystem (400-/100-400 cpm)	675	615	20,800	120
700-5141	Punch Subsystem (100-400 cpm)	496	496	17,000	105
700-5151	Reader Subsystem (punched cards, 300 cpm)	170	155	4,350	50
700-5152	Reader Subsystem (punched and marked cards, 300 cpm)	225	205	5,800	55
	Printers				
700-5515	200-lpm Printer Subsystem (96 cols; requires 700-3010)	475	429	12,000	100
700-5516	200-lpm Printer Subsystem (132 cols; requires 700-3010)	605	550	12,000	115
700-5520	300-lpm Printer Subsystem (120 cols; requires 700-3010)	665	605	12,000	165
	Teleprinters				
Note: ASR 33 or ASR 35 is mandatory on all systems for maintenance and warranty purposes. A KSR 33 can be substituted for the ASR on those systems that include a paper tape reader, Type 700-5010, or any card reader.					
700-5300	Teleprinter Interface Only	22	20	840	10
700-5307	ASR 33 Teleprinter with Control	92	87	2,150	40
700-5310	KSR 33 Teleprinter with Control	66	60	1,850	35
700-5507	ASR 35 Teleprinter with Control	184	166	5,200	35
	DATA COMMUNICATIONS				
	Synchronous/Asynchronous Equipment				
700-6312	Sync Single-Line Controller	55	50	1,400	15
700-6316	MIL STD 188C Interface	34	31	570	13
700-6321	Low-Speed Multiline Controller	268	241	6,885	40
700-6322	Universal Multiline Controller	277	250	7,140	40
700-6333	Medium-Speed Multiline Controller	58	53	1,615	10

NA Not Available

Notes: NA Not available
— Not applicable
* Not available on new orders

INTERDATA

7/32 System Report



75-17

OVERVIEW

Interdata's Model 7/32 computer is a microprogrammed 32-bit minicomputer that is at the bottom of Interdata's new 32-bit line; at the same time, it can operate in a 16-bit mode to use application programs developed for Interdata's 16-bit systems. Because it uses a 32-bit word, the 7/32 can directly address 1 million bytes of memory and can handle higher-precision arithmetic operations than the 16-bit line. The 7/32 is a processor designed for the top end of the minicomputer market, designated by Interdata as the "mega-mini" market.

The 7/32 uses memory modules that can store up to 32 kilobytes of core memory on a single circuit board. Memory cycle time is either 750 or 1,000 nanoseconds for 2 bytes. Maximum memory capacity is 1,048,576 bytes for the 7/32.

The 7/32 falls between Interdata's 7/16 and 8/32 minicomputers. The 7/16 is a 16-bit machine that can be expanded in the field to a 7/32. The 7/32 can operate in either the 16-bit mode of the 7/16 or the 32-bit mode used exclusively in the faster 8/32.

Interdata's 7/16 is a 16-bit machine with the same basic architecture as the earlier "New Series," but with a larger instruction set and 32K-byte memory boards. The New Series consisted of Models 50, 55, 60, MS-5, 70, 74, 80, and 85; the first four models use special communications instruction sets and the latter four use general-purpose instruction sets. The 7/16 can be field upgraded to a 7/32 by means of a special "stretch 32" option.

The 7/32 uses the same basic architecture as Interdata's earlier computers but with some notable extensions: 32 hardware accumulators, 30 index registers, both multiplexor and selector I/O channels, large multilevel priority interrupt system, I/O Auto Drive Channels, and large instruction set. The 7/32 uses 136 instructions, a superset of the 16-bit New Series and 7/16 instruction set. Like the 7/16, the 7/32 is well suited for communications by virtue of its sophisticated interrupt handling system (up to 1,023 levels). The 7/32 also has a specialized set of standard instructions for data communications applications including code translation, CRC-16, and special character recognition. Table 1 lists the 7/32 mainframe characteristics.

The 8/32 is a 32-bit machine with a full 32-bit bus structure, four-way interleaved memory, 214 instruction set, up to 1 million bytes of directly addressed memory, dual 64-bit lookahead stacks and eight dual stacks of 16 32-bit general registers for user, I/O, and OS programming as well as rapid context switching. The 8/32 uses the same 750-nanosecond core modules (16-bit words) as the 7/16 and 7/32, achieving greater processing speed by virtue of the four-way core interleaving, the lookahead stacks, and 32-bit wide memory bus.

Table 1. Interdata Model 7/32: Processor Characteristics

Central Processor	
Type	Microprogrammed
No. of Internal Registers	32 (2 stacks of 16)
Use	general purpose; 30 indexable
No. of Instructions	
Standard	136
Optional	17
Fixed-Point Arithmetic	
Add/Subtract	Std
Multiply	Std
Divide	Std
Add time (μsec)	3.25 to 3.75
Floating-Point Arithmetic	Opt
Addressing	
Direct (16-bit half-words)	524,288 (1M bytes)
Indirect	No
Indexed	Yes (2 levels)
Max I/O devices	1,023
Priority Interrupt System	
Lines	8
Levels	1,023
Memory	
Type	Core
Word length (bits)	32 (two 16-bit fetches)
Cycle time/word (μsec)	0.75; 1.0
Capacity (16-bit half-words)	
Max	524,288
Min	8,167
Increment	2K, 4K, 8K
Parity	Opt
Protect	Opt
ROM	Std
Use	Microinstructions (control store)
I/O Channels	
Programmed I/O	Std (Auto Drive Channels)
Direct Memory Access	Std
No. of channels	7
Multiplexed I/O	Std
Selector Channel	Opt
Over DMA	2.6M
Over selector channel	2.0M

Software for the 7/32 includes two new operating systems, OS/32ST, a serial (batch) processing system, and OS/32MT, a multiprogramming real-time system. Language processors for the 7/32 include FORTRAN V, the CAL assembler common to both 32-bit and 16-bit lines, and BASIC. The 7/32 was first delivered in August 1974.

PERFORMANCE AND COMPETITIVE POSITION

The 7/32 is at the bottom of Interdata's 32-bit line, a line extending from minicomputer power at the level of the Digital PDP-11/40 and Data General ECLIPSE all the way up to the middle of the IBM System/370 line with the 8/32. The system will not impact the small-to-medium computer market that used to be the exclusive property

of the large mainframe manufacturers however, because the larger computer manufacturers offer software support and custom programming that puts them in another league. With the 7/32 competing against 16-bit systems in the minicomputer market, Interdata stresses not only cost but inherent software advantages over its competitors due to use of the 32-bit word. The 7/32 can address all large memories directly. Unlike 16-bit word computers, it does not require a memory management hardware unit to convert virtual memory addresses to physical addresses for memories beyond 64K addresses. The advantage is programming simplicity and easy-to-implement operating systems.

In addition, the 32-bit word restricts program size only to that of physical memory and not to the size of the largest virtual memory segment. Virtual addresses need not be converted to physical addresses via a memory management unit. This process slows down program execution time by lengthening memory access time and by increasing the operating system overhead for loading and maintaining memory mapping registers. Also, a real-time operating system is easier to develop when the system does not require a management unit, and it needs less memory for its implementation. Other minicomputer manufacturers, MODCOMP, for instance, have 32-bit machines, but so far, Digital and Data General are still using 16-bit lines. Part of the reason for staying with the 16-bit word is the cost of developing new software. Nevertheless, many industry observers feel that it will not be long before most mini makers will produce 32-bit systems (and cut into the market for big computers).

Interdata has produced both of the 7/32's operating systems on schedule, and this factor has considerably strengthened the system's original position vis-a-vis the minicomputer giants. Although addressing a large market with the 7/32, this market will be expensive to compete in, because of the strong systems already available. Interdata must develop considerable software to compete successfully. Having a larger system to offer users who are moving up strengthens the company's position. The 7/16 is now the entry-level system; users can then advance to the 7/32 for medium-range processing power, or go all the way to the powerful 8/32. The market range for Interdata computers is quite broad; not only have the 7/32 and 8/32 increased the size of the market for which these computers are applicable but they protect the firm's customer base from wandering as their processing needs increase.

Configuration Guide

The basic Model 7/32 system consists of a central processor with 136 instructions that include hardware multiply/divide, 32K bytes of core memory with cycle time of 0.75 microsecond, power supply, and chassis with 16 slots. The central processor uses three circuit boards, and each 32K bytes of memory uses one board. The 7/32 can be expanded by 32K-byte core memory modules to a maximum of 1,048,576 bytes. Other optional features include floating-point arithmetic, memory protect, power fail/auto restart and display console with hexadecimal display and hexadecimal character keys. The 7/32 uses a 16-bit wide I/O bus and can use the same peripherals as the 7/16. Table 2 lists the available peripheral devices.

Configuration requirements for the operating systems and language processors are described in Table 3.

Compatibility

Although not 100 percent compatible, the Model 7/32 can run application programs developed for the New Series processors and for the 7/16. The 7/32 uses a 32-bit word, but it can run programs in a 16-bit word mode under control of a mode bit in the program status doubleword. It uses the same chassis, power supplies, peripheral controllers, and memory modules used by all the New Series processors.

Table 2. Interdata Model 7/32: Peripherals

Model Number	Description
Punched Tape	
M46-240	300-cps reader
M46-242/250	300-cps reader, 75-cps punch
Punched Card	
M46-230/236	400-/1,000-cps reader
Printers	
M46-204	60 to 200- lpm, 132-col, 64-char set
M46-207/209	200/600- lpm, 132-col, 64-char set
Terminals	
M46-000/001	ASR 33/35 TTY
M46-100-103	A/N display, 4,920 char, to 9,600 baud
M46-108	Graphic display, to 9,600 baud, 1,024 x 1,024 point matrix
Magnetic Tape	
M46-400	Dual-drive cassette, 500K bytes/cassette, 1,000-cps xfer rate
M46-460	9-trk, 800-bpi magnetic tape, 45 ips
M46-465-467	9-trk, 1,600-bpi magnetic tape, 45 ips, 4 drives/controller
M46-476	7-trk, 556- or 800-bpi (not both) magnetic tape subsystem, 4 drives/controller
Discs	
M46-410	2.5M bytes, 5440-type removable cartridge disc, 4 drives/controller
M46-516	10.0M bytes, fixed/removable 5440-type cartridge disc, 4 drives/controller
M46-429	40.0M bytes, 2316-type disc pack, 4 drives/controller
Process I/O	
M48 series	Wide-range analog input, up to 512 channels
M48 series	High-speed low-level analog input, up to 64 channels
M48 series	High-level analog I/O, up to 8 differential or 16 single-ended inputs
M48 series	Real-time analog controller, two 32-word solid-state buffer memories
M07/M48	Digital multiplexor subsystem, 2,048 input & 2,048 output lines
Communications	
M10-022	Auto dial units, 4-lines
M11-200	IBM 360/370 interface multiplexor (burst or block modes) channel
M47-000/001	Bell-type adapters, 201/301, to 9,600/40,800 baud
M47-100	Async line module controller, up to 92 lines, to 1,800 baud
M47-101/102	Programmable single-line module/adapter for Bell 103 & 202

Table 3. Interdata Model 7/32: Software

Package	Description
OS/32 MT	Real-time multiprogramming, multitask operating system, up to 255 priority levels; requires 32-bit Interdata computer, 65K bytes of memory, operator console, TTY, memory protect, clock
OS/32ST	Serial task operating system, upward compatible with OS/32MT; requires 32-bit processor, 65K bytes of memory, operator console, TTY
FORTRAN V	ANSI x 3.9 - 1966 FORTRAN IV with extensions including ISA calls, requires 32-bit CPU, 8K bytes of memory above operating system requirements, operator console, TTY
CAL	Common Assembly Language for both 16-bit and 32-bit systems; requires 8K bytes of memory above operating system requirements on 32-bit CPU, console, TTY
BASIC	Extended Dartmouth BASIC, for single user; requires 32-bit CPU (in 16-bit mode), 10.5K bytes of memory above operating system requirements, console, TTY

The 7/32 programs are upward compatible with those of the 8/32.

MAINTENANCE AND SUPPORT

Interdata supplies systems on a purchase-only basis. Users can negotiate separate maintenance contracts for on-site engineers (1, 2, or 3 shifts) or they can take damaged boards to a repair depot. Maintenance service can also be obtained on a per-call basis.

Interdata has offices in more than 34 locations in the United States and Canada as well as in Japan, Australia, Great Britain, and Germany.

HEADQUARTERS

Interdata
2 Crescent Place
Oceanport NJ 07757
(201) 229-4040

TYPICAL PRICES

Model Number	Description	Purchase $*	Monthly Maint. $
	MODEL 7/32 GENERAL PURPOSE PROCESSOR		
	32-bit processor capable of directly addressing 1,000,000 bytes of main memory; includes 32 GP Reg, each 32 bits wide, high-speed multiply/divide, DMA connection, privilege instruction detect, 1,024 hardware vectored interrupt levels, up to 1,024 automatic driver channels and autoload bootstrap instruction for initial loading		
M73-023	Model 7/32 Processor with 32,768 Bytes of Core Memory (750 nsec, 16-slot chassis, and power supply)	9,950	110
	MODEL 7/32 PROCESSOR OPTIONS		
M73-100	Power Fail Detection/Auto Restart	400	2
M73-101	Floating-Point Hardware	3,900	30
M73-103	DMA Buffer	350	5
M73-104	Memory Access and Protect Controller	3,500	25
M73-105	Extended Memory Selector Channel	1,000	10
M73-106	Local Memory Bank Interface	5,900	50
M73-107	Processor Parity Control	1,000	–
M71-101	Binary Display Panel	300	2
M71-102	Hexidecimal Display Panel	600	5
M70-104	Loader Storage Unit controller	500	10
M70-105	128-Byte Storage Module	100	–
M48-005	Multiplexor Bus Buffer	900	5
	MODEL 7/32 MEMORIES		
M71-300	8,192-Byte Memory Expansion Module (1-μsec core cycle time)	2,000	20
M71-302	16,384-Byte Memory Expansion Module (1-μsec core cycle time)	2,650	30
M71-304	32,768-Byte Memory Expansion Module (1-μsec core cycle time)	3,950	40
M73-306	M71-304 with 750-nsec core cycle time	4,500	45
M71-301	M71-300 with parity	2,500	20
M71-303	M71-302 with parity	3,150	30
M71-305	M71-304 with parity	4,450	40
M73-307	M73-306 with parity	5,000	45
	SYSTEM MODULES		
M48-012	Line Frequency Derived Clock	250	5
M48-000	Universal Clock Module	600	5
M48-001	8-Line Interrupt Module	900	5
M48-002	General Purpose Interface Board (15 inches)	550	NA
M48-013	Universal Logic Interface	650	NA
M48-014	Input/Output Bus Switch	1,500	10
M48-107	Extension Cable Kit, 25 feet	175	–
M48-018/9	Manual Control Panel for I/O Bus Switch	200	–
	DISC		
M46-410	2.5M-Byte Removable Cartridge Disc System	10,000	80
M46-414	2.5M-Byte Removable Cartridge Disc System	10,100	80
M46-411	2.5M-Byte Removable Cartridge Disc Expansion Drive	5,500	50
M46-420	Removable Cartridge Disc Interface (for use with up to four 2.5M-byte disc drives)	4,000	30
M49-023	Expansion Power Supply for Single Drive Disc	500	–
M49-027	Expansion Power Supply for Single Drive Disc	600	–
27-039	2.5M-Byte Removable Cartridge Disc Pack	200	–
M46-416	10M-Byte Removable Cartridge Disc System	12,000	120
M46-417	10M-Byte Removable Cartridge Disc System	12,100	120
M46-418	10M-Byte Removable Cartridge Disc Expansion Drive and Power Supply	8,000	90
M46-419	50-Hz Version of M46-418	8,100	90
M46-421	Removable Cartridge Disc Interface (for use with up to four 10M-byte dual disc drives)	4,000	30
27-056	10M-Byte Removable Cartridge Disc Pack	270	–
M46-429	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	24,950	200
M46-430	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	25,100	200
M46-431	40M-Byte Removable Cartridge Disc Expansion Drive	17,950	200
M46-432	40M-Byte Removable Cartridge Disc Expansion Drive	18,100	200
M46-433	Removable Cartridge Disc Controller (for use with up to four 40M-byte disc drives)	7,000	50
M46-434	40M-Byte Removable Cartridge Disc Pack	500	–
	TELETYPE CONSOLES		
M48-010	ASR Model 33/35 TTY Interface (with internal cable)	350	5
M46-000	ASR Model 33 Teletypewriter (with external cable)	1,450	40
M46-002	50-Hz Version of M46-000	1,550	40
M46-001	ASR Model 35 Teletypewriter (with external cable)	4,200	40
M46-003	50-Hz Version of M46-001	4,300	40
	PAPER TAPE EQUIPMENT		
M46-250	Combination Paper Tape Reader/Punch Interface	900	10
M46-240	Paper Tape Reader, Uni-directional (300 cps)	1,300	20
M46-241	50-Hz Version of M46-240	1,400	20
M46-242	Combination Paper Tape Reader/Punch (300/75 cps)	3,300	40
M46-243	50-Hz Version of M46-242	3,400	40
	PUNCHED CARD		
M46-235	Card Reader Interface (with internal cable)	900	10
M46-234	Hardware Hollerith to ASCII Conversion Option	350	–
M46-230	Card Reader (400 cpm; includes external cable)	3,000	40
M46-231	50-Hz Version of M46-230	3,100	40
M46-236	Card Reader (1,000-cpm; includes external cable)	5,900	80
M46-237	50-Hz Version of M46-236	6,000	80
	PRINTERS		
M46-202	Line Printer Interface (and internal cable for 60 to 200 lpm line printer)	500	10
M46-204	Fully Buffered Line Printer (60 to 200 lpm, 132 cols, 64 char set; includes external cable)	5,000	50
M46-205	50-Hz Version of M46-204	5,200	50
M46-206	Line Printer Interface (and internal cable for 200 or 600 lpm line printer)	750	10
M46-207	Full Buffered Line Printer (200 lpm, 132 cols, 64 char set; includes external cable)	12,350	90
M46-208	50-Hz Version of M46-207	12,650	90
M46-209	Fully Buffered Line Printer (600 lpm, 132 cols, 64 char set; includes external cable)	17,150	110
M46-210	50-Hz Version of M46-209	17,450	110
	MAGNETIC TAPE		
M46-400	INTERTAPE (cassette system with dual transports, 1,000 char per sec read/write speed, hardware read-after-write check, longitudinal redundancy check, 500,000-byte capacity per cassette; includes interface)	4,200	30

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $*	Monthly Maint $
M46-470	9-Track, 800 bpi, Magnetic Tape Transport Interface (interface controls up to 4 IBM compatible continuous read-after-write 45 ips drives; includes cyclic redundancy check hardware and read-after-write check)	2,900	20
M46-460	9-Track, 800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-461	50-Hz Version of M46-460	6,100	90
M46-473	7-Track, 556 bpi Magnetic Tape Transport Interface	2,900	20
M46-474	7-Track, 800 bpi Magnetic Tape Transport Interface	2,900	20
M46-476	7-Track, 556/800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-477	50-Hz Version of M46-476	6,100	90
M46-471/2	Magnetic Tape Transport Direct Connect Cable	100	–
M46-475	9-Track, 1,600 bpi, Magnetic Tape Transport Interface (controls up to 4 IBM compatible, continuous read-after-write 45 ips drives via a phase-encoded formatter supplied with M46-465 or M46-466)	1,500	10
M46-465	9-Track, 1,600 bpi, 45 ips Magnetic Tape Transport and 1 x 4 Phase-Encoded Formatter (continuous transfer rate is 72,000 char/sec)	12,000	120
M46-466	50-Hz Version of M46-465	12,100	120
M46-467	9-Track, 1,600 bpi, 45 ips, Magnetic Tape Expansion Transport (for use with M46-475 and M46-465)	6,800	80
M46-468	50-Hz Version of M46-467	6,900	80
	VIDEO DISPLAY		
M46-107	1,200 Baud Local Current Loop Interface (with internal cable)	400	5
M46-100	Alphanumeric Video Display Unit (1,920-char (24 lines x 80 char); std 64-char ASCII subset; 110 or 1,200 baud via current loop interface; up to 9,600 baud with RS-232C)	2,250	30
M46-101	Std 50-Hz Version of M46-100	2,350	30
M46-102	M46-100 with complete processor and operator cursor control, a full range of editing features, and message and character modes	3,350	40
M46-103	50-Hz Version of M46-102	3,450	40
M46-108/9	Graphic Display Terminal	6,500	60
M46-104/5/6	External Cable Assembly	–	–
	DATA COMMUNICATIONS SYSTEMS MODULES		
M47-000	Bell 201 Type Data Set Adapter or Equivalent	1,200	10
M47-001	Bell 301 Type Data Set Adapter or Equivalent	1,400	10
M47-102	Programmable Async Single Line Adapter (for 103/202 data set or local RS-232 terminal)	400	5
M47-100	Async Line Module Controller	500	10
M47-101	Programmable Async Line Module	1,200	10
M49-021	Programmable Async Line System Chassis	550	–
M10-022	Automatic Dial Unit Controller	1,600	10
M10-054	Data Set Cable (for RS232 compatible data sets)	60	–
M10-056	Data Set Cable (for Bell 301 type data sets)	350	–
M47-200	IBM 360/370 Parallel Interface (single address interface)	3,500	50
M47-201	IBM 360/370 Parallel Interface (multiple address (up to 256) interface)	5,000	60
	CABINETS, CHASSIS, AND POWER SUPPLIES		
M49-020	System Chassis	700	–
M49-024	Power Supply	800	5
M49-026	Bulk Power Supply	1,000	5
M49-003	Adapter Card (10 to 15 inches)	150	–
M49-004	System Cabinet	650	–
	SOFTWARE**		
S90-000-16	BOSS-PLUS Source Paper Tape and Documentation Package	175	–
S90-001-16	DOS-PLUS Source Paper Tape and Documentation Package	500	–
S90-002-46	RTEX Source Card and Documentation Package	1,500	–
S90-003-26	RTOS Source Cassette and Documentation Package	2,000	–
S90-004-26	OS/16 MT Source Paper Tape and Documentation Package	950	–
S90-005-11	OS/32 ST Source and Object Paper Tape and Documentation Package	750	–
S90-007-11	OS/32 ST Object Paper Tape and Documentation Package	300	–
S90-006-41	OS/32 MT Source Card and Object Paper Tape and Documentation Package	3,000	–
S90-009-21	OS/32 MT Object Cassette and Documentation Package	2,500	–

* Quantity discounts are available on most items. NA Not Available — Not Applicable

**Additional Software Documentation Packages available.

ITAM (Interdata Telecommunication Access Method) has been introduced by Interdata for use with the Model 7/32. The package runs under OS/32-MT, Interdata's 32-bit multitasking operating system. A minimum ITAM system includes the Model 7/32 with 65 bytes of memory, OS/32-MT, memory access controller, a real-time clock, control console, and appropriate data set adapters. The 7/32 offers as standard features data communications instructions, auto driver channels, and DMA transfer rates of two megabytes per second.

ITAM provides two levels of communications: device independent and device dependent.

On the device independent level, remote devices are accessed as though they are directly attached peripherals. Asynchronous terminals such as A/N displays and teleprinters can be supported. A remote job entry (RJE) package for the 7/32 can also be included to allow it to emulate an IBM 2780 or 3780 remote batch terminal. Processor-to-processor communication using binary synchronous (BSY) protocol is also supported.

On the device dependent level, users can develop special systems with minimum operating system overhead. Interdata offers asynchronous and binary synchronous modules that can accommodate a variety of facilities, protocol, and networks so the sophisticated user can provide his own terminal protocols. ITAM simplifies the user's software interface. Users, for example, can initiate, via one request, a single message followed by a series of message receptions.

The purchase price for ITAM is $2,500; it became available in May 1975.

Interdata has also introduced two new language processors to help users increase their programming capabilities: MACRO CAL and BASIC/32.

MACRO CAL provides alternate macro libraries and keyword macro prototypes. It can be used with all Interdata minicomputers, both 16- and 32-bit. MACRO CAL requires 24K bytes of main memory; it includes a macroprocessor, utility program, and reference manual in addition to the system macro library. Each programmer can develop his own library of macros that refer to his programs and applications.

Keyword macro prototypes allow programmers to use symbolic references in the macro routine to the arguments or variables in the macro's parameter list. Operands or data quantities can be written in any order or omitted with default values or standard conditions provided.

The BASIC/32 interpreter requires 10K bytes of main memory. It includes the BASIC Interpreter, Language/Operating procedure, as well as matrix handling, string data manipulation and pattern matching. BASIC/32 is reentrant for multiuser operations in a terminal-oriented environment.

Some Interdata BASIC/32 standard features include run time trace facilities, set trace, end trace, matrix operations, extended interface statement, and INPUT and PRINT via logical unit.

MACRO CAL costs $300 and BASIC/32 $150; both are immediately available.

OVERVIEW

The Interdata 8/32 Megamini is the first all 32-bit system in Interdata's line of minicomputers. It is at once the top of the Interdata line and a front runner in the upward push of the minicomputer market into the small- and medium-scale ranges. The 32-bit word allows it to address up to 16 megabytes of main memory, although, at present, memory capacity is limited to 1 megabyte. The speed of the system, throughput efficiency, input/output transfer rate and software have all been designed to make it competitive in the midicomputer range. The system is upward compatible with Interdata's 16-bit-line, giving Interdata users a roomy upward growth path. The I/O bus is 16 bits wide to maintain compatibility with standard peripherals. The memory modules are the same ones used with the 7/32 and 7/16 systems, but two 16-bit-word modules operate in tandem over two 16-bit-wide buses to make up the 32-bit word. In other respects, cache memory registers, memory interleaving, I/O organization and a number of other features enhance throughput. Table 1 lists specifications.

Interdata sees a sizeable new market for 32-bit real-time "midicomputers" because of their low cost, high speed and reliability. One area, of course, is data communications, which has long been one of Interdata's strong fields. Other markets identified are power grid analysis, nuclear power plant control and refinery monitoring, all of which could use the Megamini for economic problem solving. Air traffic control and banking applications also show promise.

With these applications in mind, Interdata recently has added more software capability. The Model 8/32 Megamini can run under the OS/32 ST for batch program development and under OS/32 MT, a multitasking operating system which was delivered in December 1974 for the 7/32. FORTRAN V, Level II is available for program development, as well as Macro CAL, the assembler language common to all Interdata computers. BASIC is available as a compiler and as an interpreter. In addition to these, Interdata has added ITAM, Interdata's Telecommunications Access Method, employing both device-independent and device-dependent modes to meet users' needs.

Table 1. Interdata 8/32 Megamini: Mainframe Specifications

Central Processor	
Microprogrammed	Yes
No. of Internal Registers	32-128
Addressing	
Direct	To 1M bytes
Indirect	No
Indexed	Yes, 2 levels
Instruction Set	
Number	214
Decimal Arithmetic	No
Floating Point Arithmetic	Yes (opt)
User-microprogramming	Not software supported
Interrupt System	
Lines	4
Levels	1,024 std
Main Storage	
Type	Core
Cycle Time (nsec)	750
Basic Addressable Unit	32-bit word
Cache memory	Lookahead Stack
Min Capacity (bytes)	128K
MaxCapacity (bytes)	1M
Increment Size (bytes)	32K
Ports per module	1
Memory Interleaving	4-way
Error Checks	Parity
Protection	Opt
Memory Management	Yes (opt)
ROM	
Use	Control Store
I/O Channels	
Programmed I/O	Yes
DMA channels	1 (up to 7 selectors)
Multiplexed I/O	1,024 subchannels
Max Transfer Rate	
Over DMA, bytes/sec	6M
MUX I/O, bytes/sec	62.5K

In addition to standard peripherals available for the 16-bit systems and the 7/32, Interdata has added new 360/370 interfaces that allow the 8/32 to interface directly to a block multiplexor, multiplexor, or selector channel of the IBM systems. These interfaces facilitate the development of front-end systems that look like 270X/370X to the host computer and strengthen Interdata's position in the communications marketplace. The dual I/O system, with a multiplexor bus for up to 1,024 low- or medium-speed devices and a DMA bus with selector channels for mass storage (up to 112 controllers) provide powerful I/O facilities which will be particularly useful for multiprocessor configurations for shared data bases that are undoubtedly in Interdata's future.

The first 8/32 Megamini was delivered in June 1975.

Interdata is a small but rapidly growing company, organized in 1966. As of June 1975, it had delivered more than 3,000 systems; the company employs around 1,000 persons world wide, with offices in 25 U.S. cities, and four

other countries — England, Germany, Canada and Australia. Interdata became a subsidiary of the Perkin-Elmer Corporation in 1974, a move designed to enhance the financial position of the company by providing access to more development funds.

COMPETITIVE POSITION

The Model 8/32 Megamini is a fine addition to Interdata's line of computers, expanding the power and thus the market of its system upward. This upward thrust has been exhibited by all the minicomputer manufacturers, even Computer Automation, and has interesting ramifications for the whole computer industry. The low end of the minicomputer market has been usurped by microcomputers and, with the dispersal of computer power and real-time interactive processing in vogue, all manufacturers have seen that their real-time systems can be expanded and speeded up to compete against medium scale, general purpose systems at much lower prices than, for instance, IBM. There is a trade-off of course. The minicomputer manufacturer does not supply the kind of software support that the large mainframe manufacturer does. On the other hand, the cost of a large mini can be as low as one tenth the cost of the smallest real-time IBM 370, the 158. Because the minis are oriented toward real-time and the 370 series is oriented toward batch processing, many applications are suited to "megaminis" or "midis", which are about the size of a 370/135, a batch system. Thus the midis don't really have competition from IBM because IBM enters at the high end of the real-time market.

The two minicomputer leaders, Digital and Data General, have approached this market with memory management systems that expand their 16-bit systems, instead of producing a 32-bit system. The only other 32-bit minicomputer system now on the market is the SEL32, made by Systems Engineering Laboratories, a small company that has had inconsistent management but good equipment. Thus, the strongest competition from minicomputer makers are from systems that already are using devices that increase throughput or memory size. These companies will have to devise more and more techniques to expand their systems further. The Interdata 32-bit line is just beginning to explore and exploit its capabilities, and it can easily move upwards, particularly in memory capacity.

The Xerox 550 is also a strong competitor in performance but, unlike other manufacturers like SYSTEMS with its SEL32, Xerox has not managed to bring hardware costs down.

Interdata's chief advantage over medium-scale, general purpose systems like the IBM 370/158 is price. But what a difference. Table 2 presents a comparison of the specifications of five chief competitors in the midicomputer field.

Users of Interdata's smaller computers have a system to move up to as the need for power expands. The name of the game today is to capture the first-time computer user when he enters the market; to maintain the customer base with a diversified compatible supply of computer products reaching up into the medium scale range; and to keep products, price and performance competitive by redesigning products around new technologies. Many computer users are loyal to a product line because of their investment in applications software. A manufacturer cannot expect to capture very many new customers at the high end of the computer line.

Interdata already has a substantial number of orders for the 8/32, primarily for aerospace simulation and data communication applications. Because the 8/32 is powerful but low-cost, Interdata believes new operations will be computerized for the first time, and this will open markets in the midi range. It remains to be seen how big that market is.

Table 2. Interdata 8/32 Megamini: Comparison With Other Computer Systems

	Interdata 8/32	Digital PDP-11/70	SEL 32	XEROX 550	IBM 370/158
Word Length	32 bits	16 bits*	32 bits	32 bits	32 bits
Instruction Times, μsec (Memory to Register)					
Integer Add	1.2	1.8	1.2	1.8	.9
Integer Multiply	3.5	3.9	4.5	6.2	2.0
Integer Divide	5.8	8.3	5.1	14.4	9.9
Floating Point Add	2.3	8.2	3.0	6.1	2.4
Floating Point Multiply	3.0	11.2	4.5	9.1	2.3
Floating Point Divide	5.3	12.2	8.9	23.3	8.9
Hardware I/O	Yes	No	No	Yes	Yes
Max. DMA Rate/Second	6MB	4MB (UNIBUS); 5.8MB (data-channel)	6MB	4MB	6.7MB
Max. Address	1MB	64KB	512KB	1MB	16MB
GP Registers	8 Stacks of 16 each	2 Stacks of 8 each	1 Stack of 4	4 Stacks of 16 each	1 Stack of 16
Pricing ($)					
CPU + 128KB Memory	51,900	54,600(1)	43,900	128,700	NA
+ 256KB Memory	70,900	68,800	71,700	178,700	NA
+ 512KB Memory	107,400	101,800	128,000	278,700	1,779,200
+ 1048KB Memory	179,400	163,800	238,400	478,700	1,905,700

Notes:
*Uses 16-bit operands but data paths between cache and memory and high speed device controllers are 32 bits wide.
(1) Console, installation, and parity are bundled with the PDP-11/70.

Interdata, like other minicomputer manufacturers, has traditionally been a tool maker, not a problem solver. As long as customers were sophisticated, they could develop the software techniques to convert the tools into solutions. This market has been largely saturated, at least enough to prevent continued growth of the minicomputer market from that source.

Recognizing this, Interdata has begun to focus its marketing effort toward specific types of applications — not just vertical markets but types of applications that cut across vertical markets. These include such things as industrial continuous and batch process control, test and measurement, seismic data processing, and simulations.

So far, Interdata has steered clear of commercial data processing, although others have developed commercial systems using Interdata computers. Most noteworthy is the COBOL-oriented commercial system developed by Diversified Data Systems, Inc., of Tucson, Arizona. Since it was first delivered for the 16-bit computers during the second quarter of 1974, over 50 systems have been delivered. A version for the 32-bit Interdata systems is scheduled for delivery in September 1975. It is called IBOLS-32 (Integrated Business Oriented Language Support) and provides batch services similar to that of the IBM 360 OS/MFT. It includes the COBOL compiler, sort/merge, ISAM initialize and run-time ISAM support. The one-time system license fee is $12,500.

It is not surprising that the Interdata hardware is being used for commercial data processing, because the instruction set is very similar to the IBM 360 instruction set.

Interdata is working on a new optimizing FORTRAN compiler for its 32-bit computers. Most of the 8/32 Megamini users will be programming in FORTRAN, and this will enhance system throughput for most customers.

The next year will be crucial to Interdata as a company. So far, Perkin-Elmer has left Interdata alone while financing its expansion. This will undoubtedly continue only if Interdata's revenue continues to increase. In today's transitional market, minicomputer manufacturers are finding they cannot market in the same old way. Customers are more interested in problem solutions than in tools. Thus, companies must spend more creative energy on planning and marketing strategy. Interdata appears to understand today's market; it will be interesting to watch the company's response to it.

CONFIGURATION GUIDE

The basic 8/32 system consists of a 32-bit processor with two sets of 16 32-bit registers, 1,024 interrupt levels, up to 1,024 multiplexed autodriver channels, DMA channel, 128K bytes of core memory, two power supplies, and a 16-slot chassis. The following processor options are standard:

- Memory expansion up to 1M bytes.
- Register expansion to eight sets of 16 registers each.
- Floating point processor with one or two associated sets of registers (single precision only; or both single and double precision).
- Memory parity generation and checking.
- Field upgrade kit for converting 7/32s into 8/32s.

Memory is added in 32K-byte modules. Although core and semiconductor memories can be mixed on a system, Interdata offers only core at the present time.

Up to 1,024 devices can be addressed. The interrupt subsystem allows up to 1,024 device interrupts, and the multiplexor channel can attach 1,024 slow to medium speed devices. In addition to the multiplexor channel, a DMA channel is also standard. Up to seven selector channels can be implemented on the DMA, with up to 16 high speed and mass storage subsystems per channel.

The disc, magnetic tape, paper tape, card, printer, process I/O and communications peripherals used on the 7/32 can also be used on the 8/32. Table 3 outlines specifications of these.

Table 3. Interdata 8/32 Megamini: Peripherals

Model Number	Description
Punched Tape	
M46-240	300 cps Readers
M46-242/250	300 cps Reader, 75 cps Punch
Punched Card	
M46-230/236	400 1,100 cps readers
Printers	
M46-204	60-200 lpm, 132 col, 64-char set
M46-207/209	200/600 lpm, 132 col, 64-char set
Terminals	
M46-000/001	ASR 33/35 TTY
M46-100-103	A/N Display, 4,920 char, to 9,600 baud
M46-108	Graphic Display, to 9,600 baud, 1,024 x 1,024 point matrix
Magnetic Tape	
M46-400	Dual drive cassette, 500K bytes/cassette 1,000 cps xfer
M46-460	9-trk 800 bpi mag tape, 45 ips
M46-465-467	9-trk 1,600 bpi mag tape, 45 ips, 4 drives/controller
M46-476	7-trk, 556 or 800 bpi (not both) mag tape subsystem, 4 drives/controller
Discs	
M46-410	2.5Mb 5440-type removable cartridge disc, 4 drives/controller
M46-516	10.0Mb fixed/removable 5440-type cartridge disc, 4 drives/controller
M46-429	40.0Mb 2316 type disc pack, 4 drives/controller
Process I/O	
M48 series	Wide Range Analog Input, up to 512 chans
M48 series	High Speed Low Level Analog Input, up to 64 chans
M48 series	High Level Analog I/O, up to 8 differential or 16 single-ended inputs

Table 3. (Contd.)

Model Number	Description
M48 series	Real Time Analog Controller, two 32-word solid state buffer memories
M07/M48	Digital Multiplexor Subsystem, 2048 Input & 2048 output lines
Communications	
M10-022	Auto Dial Units, 4-lines
M11-200	IBM 360/370 Interface Multiplexor (Burst or Block modes) channel
M47-000/001	Bell-type Adapters, 201/301, to 9,600/40,800 baud
M47-100	Async Line Module Controller up to 92 lines to 1,800 baud
M47-101/102	Programmable Single Line Module/ Adapter for Bell 103 & 202

Table 4. Interdata 8/32 Megamini: Software

Package	Description
OS/32 MT	Real-time multiprogramming, multitask operating system, up to 255 priority levels, requires 32-bit Interdata computer, 32KB memory, Operator Console, TTY.
OS/32ST	Serial Task Operating system, upward compatible with OS/32MT, requires 32-bit processor, 32KB memory, Operator Console, TTY.
Fortran V	ANSI 3.9 - 1966 Fortran IV with extensions including ISA calls, requires 32-bit CPU, 8KB above operating system requirements, operator console, TTY.
CAL	Common Assembly language for both 16-bit and 32-bit systems, requires 8KB memory above operating system requirements on 32-bit CPU, console, TTY.
Basic 32	Extended Dartmouth Basic, for single user, requires 32-bit CPU (in 16-bit mode), 10.5KB memory above operating system requirements, Console, TTY.
ITAM	Interdata Telecommunications Access Method requires 65K bytes of memory, DMA, clock, control console, and data set adapter.

The major software packages with configuration requirements are listed in Table 4.

COMPATIBILITY

The 8/32 is generally upward compatible with Interdata's 16-bit linc at the application program level, given similar configurations. System software cannot be interchanged. Peripheral devices are completely interchangeable; the 8/32 uses a 16-bit I/O bus to maintain compatibility. A 7/32 system can be upgraded in the field to an 8/32.

MAINTENANCE AND SUPPORT

Interdata supplies systems on a purchase only basis. Separate maintenance contracts can be negotiated for either on-site engineers (1, 2, or 3 shifts), or for taking replacing damaged boards to a repair depot. Maintenance service can also be obtained on a per-call basis.

Interdata has offices in more than 25 locations in the United States and Canada as well as in Japan, Australia, Great Britain and Germany.

TYPICAL PRICES

Model Number	Description	Purchase Price $	Monthly Maint. $
	Model 8/32 General Purpose Processor 32-bit fully parallel processor; includes 2 sets of 16 general purpose registers; 1,024 hardware interrupt levels; 16-slot chassis; system cabinet; 2 power supplies; binary display panel; power fail detection/automatic restart; privilege instruction detect, and to 1,024 automatic driver channels; memory access and protect controller; provides for program protection, segmentation registers and current loop interface		
M83-023	Model 8/32 Processor with 131,072 bytes of 750 nsec core memory	51,900	500
	Processor Options		
M83-101	Single precision 32-bit Floating Point Hardware	2,500	20
M83-102	Hexidecimal Display Panel	300	
M83-107	Processor/Memory Parity Generation and Checking Hardware	1,000	
M83-110	Extended Register Sets for 8/32 Processor	5,000	20
	MEMORIES		
M84-300	Memory Expansion from 131,072 to 262,149 bytes	19,000	180
M83-301	M84-300 with parity	20,000	180
M83-302	Memory Expansion from 262,144 to 393,216 bytes	18,500	180
M83-303	M83-302 with parity	19,500	180
M83-304	Memory Expansion from 393,216 to 524,288 bytes	18,000	180
M83-305	M83-304 with parity	19,000	180
M83-306	Memory Expansion from 524,288 to 655,360 bytes	18,500	180
M83-307	M83-306 with parity	19,500	180
M83-308	Additional 131,072 byte memory increments	18,000	180
M83-309	M83-308 with parity	19,000	180
	SYSTEM MODULES		
M48-012	Line Frequency Derived Clock	250	5
M48-000	Universal Clock Module	750	5
M48-001	8-line Interrupt Module	900	5
M48-002	General Purpose Interface Board (15")	550	NA
M48-013	Universal Logic Interface	650	NA
M48-014	Input/Output Bus Switch	1,700	10
M48-107	Extension Cable Kit, 25 feet	175	—
M48-018/019	Manual Control Panel for I/O Bus Switch	200	—
M70-104	Loader Storage Unit Controller	600	10
M70-105	128-byte Storage Module (for use with M70-104)	100	—
M48-005	Multiplexor Bus Buffer	900	5
	DISC		
M46-410	2.5M-byte Removable Cartridge Disc System	10,000	100
M46-414	2.5M-byte Removable Cartridge Disc System	10,100	100
M46-411	2.5M-byte Removable Cartridge Disc Expansion Drive for use with M46-410 or M46-414	5,500	60
M46-420	Removable Cartridge Disc Interface for use up to four 2.5M-byte disc drives	4,000	30
M49-023	Expansion Power Supply for Single Drive Disc	500	—
M49-027	Expansion Power Supply for Single Drive Disc	600	—
27-039	2.5M-byte Removable Cartridge Disc Pack	200	—
M46-416/17	10M-byte Removable Cartridge Disc System	13,100	120
M46-418	10M-byte Removable Cartridge Disc Expansion Drive and Power Supply	8,500	90
M46-419	10M-byte Removable Cartridge Disc Expansion Drive and 50 Hz Power Supply	8,600	90
M46-421	Removable Cartridge Disc Interface	4,500	30
27-056	10M-byte Removable Cartridge Disc Pack	270	—
M46-422	2,500,000 byte Movable Head Fixed Disc System	7,200	100

PRICE DATA (Contd.)

Model Number	Description	Purchase Price $	Monthly Maint. $
M46-423	One Drive, 50 Hz version of M46-422	7,300	100
M46-429	40M-byte Removable Cartridge Disc Drive and 1 x 4 Controller	24,950	250
M46-430	40M-byte Removable Cartridge Disc Drive and 1 x 4 Controller	25,100	250
M46-431	40M-byte Removable Cartridge Disc Expansion Drive	17,950	150
M46-432	40M-byte Removable Cartridge Disc Expansion Drive	18,100	150
M46-433	Removable Cartridge Disc Controller	7,000	50
M46-434	40M-byte Removable Cartridge Disc Pack	500	—
	TELETYPE CONSOLES		
M48-010	ASR Model 33/35 TTY Interface with cable	350	5
M46-000	ASR Model 33 Teletypewriter with cable	1,750	40
M46-002	50 Hz version of M46-000	1,850	40
M46-001	ASR Model 35 Teletypewriter with external cable	4,850	40
M46-003	50 Hz version of M46-001	4,950	40
	PAPER TAPE EQUIPMENT		
M46-250	Combination Paper Tape Reader/Punch Interface with direct connect cable	900	10
M46-240	Paper Tape Reader, uni-directional, 300 cps	1,300	20
M46-241	50 Hz version of M46-240	1,400	20
M46-242	Combination Paper Tape Reader/Punch, 300/75 cps, rack mountable for use with fanfold tape	3,300	40
M46-243	50 Hz version of M46-242	3,400	40
	PUNCHED CARD		
M46-235	Card Reader Interface with internal cable for 400 cpm or 1000 cpm Card Reader	990	10
M46-234	Hardware Hollerith to ASCII Conversion Option	350	—
M46-230	Card Reader, 400 cpm includes external cable	3,060	40
M46-231	50 Hz version of M46-230	3,160	40
M46-236	Card Reader, 1000-cpm includes external cable	6,500	80
M46-237	50 Hz version of M46-236	6,600	80
	PRINTERS		
M46-202/206	Line Printer Interface and internal cable	990	10
M46-204	Fully Buffered Line Printer, 60 to 200 lpm, 132 cols, 64 char set, includes external cable	5,000	50
M46-205	50 Hz version, of M46-204	5,200	50
M46-207	Full Buffered Line Printer, 200 lpm, 132 cols, 64 char set, includes external cable	11,950	90
M46-208	50 Hz version, of M46-207	12,250	90
M46-209	Fully Buffered Line Printer, 600 lpm, 132 cols, 64 char set, includes external cable	17,150	110
M46-210	50 Hz version, of M46-209	17,450	110
M46-008	Carousel 15 Keyboard Printer Terminal	1,690	35
M48-023	Carousel 15 Current Loop Interface with internal cable	350	5
M46-845/483	Pedestal mount	175	—
M46-820	Paper Tape Reader for Carousel 15 Printer	375	5
M46-010	Carousel 30 Keyboard Printer Terminal	1,950	35
M48-024	Carousel 30 Current Loop interface with internal cable	400	5
M46-880	132 char Print Line Option for Carousel 30 Terminal	300	—
M46-860	Pin Feed adjustable width forms tractor	150	—
M46-803	Carousel 300 Keyboard Printer Terminal	2,450	35
M46-881	96 Char ASCII Character Set	300	—
M46-887	Electronic Format Control for Carousel 300 Terminal	150	—
	MAGNETIC TAPE		
M46-400	INTERTAPE; Cassette system includes dual transports, 1,000 char per sec read/write speed, hardware read-after-write check, longitudinal redundancy check, 500,000-byte capacity per cassette; includes interface	4,200	30
M46-470	9-Track, 800 bpi, Magnetic Tape Transport Interface	2,900	20
M46-460	9-Track, 800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-461	50 Hz version of M46/960	6,100	90
M46-473/4/8	Magnetic Tape Transport Interface	2,900	20
M46-476	7-Track, 556/800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-477	50 Hz version of M46-476	6,100	90
M46-479/80	7-Track 200/800 cpi, 45 lps Mag Tape Transport	6,000	90
M46-471/2	Magnetic Tape Transport Direct Connect Cable	100	—
M46-475	9-Track, 1600 bpi, Magnetic Tape Transport Interface	1,500	10
M46-465	9-Track, 1600 bpi, 45 ips Magnetic Tape Transport and 1 x 4 Phase Encoded Formatter	12,000	120
M46-466	50 Hz version of M46-465	12,100	120
M46-467	9-Track, 1600 bpi, 45 ips, Magnetic Tape Expansion Transport	6,800	80
M46-468	50 Hz version of M46-467	6,900	80
	VIDEO DISPLAY		
M46-107	1200 Baud Local Current Loop Interface with internal cable	400	5
M46-100	Alphanumeric Video Display Unit, 1920-char	2,250	30
M46-101	Std 50 Hz version of M46-100	2,350	30
M46-102	Alphanumeric Video Display Unit, 1920-char complete processor and operator cursor control, editing features, and message and character modes	3,350	40
M46-103	50 Hz version of M46-102	3,450	40
M46-108/109	Graphic Display Terminal, local interface	6,500	60
M46-104/1 105/106	External cable assembly for connection of local current loop interfaces to Video Display, 25 feet	60	—
	DATA COMMUNICATIONS SYSTEMS MODULES		
M47-000	Bell 201 Type Data Set Adapter or Equivalent	1,200	10
M47-001	Bell 301 Type Data Set Adapter or Equivalent	1,400	10
M47-102	Programmable Async Single Line Adapter for 103/202 Data Set or local RS-232 terminal; 75 to 9,600 Baud; full or half duplex; RS232C/CCITT interface; switched or private line	450	10
M47-100	Async Line Module Controller	500	10
M47-101	Programmable Async Line Module	1,200	10
M49-021	Programmable Async Line System Chassis	500	—
M10-022	Automatic Dial Unit Controller	1,600	10
M10-054	Data Set Cable, for RS232 compatible data sets	70	—
M10-056	Data Set Cable, for Bell 301 type data sets	350	—
M47-200	IBM 360/370 Parallel Interface	3,500	50
M47-201	IBM 360/370 Parallel Interface; capable of operation in multiplex burst or block multiplex modes	5,000	60
	CABINETS, CHASSIS, AND POWER SUPPLIES		
M49-020	System Chassis	700	—
M49-024	Power Supply	800	5
M49-026	Bulk Power Supply	1,000	5
M49-003	Adapter Card (10 to 15 in.)	150	—
M49-004	System Cabinet	850	—

* Quantity discounts are available on most items.
— Not Applicable

HEADQUARTERS

Interdata
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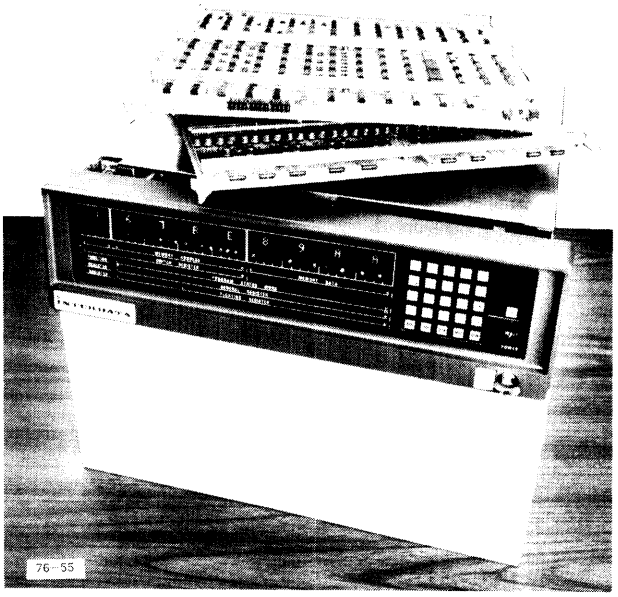
INTERDATA
Model 6/16 System Report



OVERVIEW

The new Model 6/16 offers more for less. It extends Interdata's 16-bit line of compatible computers downward in price, but not performance, making them more competitive to entry-level users as well as to OEM customers. This low end of the minicomputer market is important to manufacturers because users of small computer systems generally add on or upgrade in-line to the next larger system. OEMers also like to use compatible computers. Minicomputer manufacturers have found their best customers are their own customers. Thus, getting customers at the low end of a computer line means more customers at the top end.

Interdata tests indicate the Model 6/16 core version, executing a mix of instructions for general computation, is 30 percent faster than the Model 7/16. The increased speed can be partially explained by the multiply/divide times, which are one-fourth the Model 7/16 times. The Model 6/16 MOS version will be even faster because it uses a faster memory.

First deliveries of the Model 6/16 are scheduled for the first quarter of 1976.

Mainframe

The Model 6/16 processor is totally I/O and program compatible with the Model 7/16. It can be upgraded to a Model 7/32 via the Stretch/32 option. Both the 6/16 and 7/16 implement the basic 104 instructions, which include only arithmetic add and subtract in fixed-point, single-precision format. The optional hardware multiply and divide adds six instructions. A bipolar ROM with 60-nanosecond access time stores the CPU firmware. CPU logic is implemented using T^2L (transistor-to-transistor) MSI (Medium Scale Integration) technology.

The 6/16 uses the same four instruction formats of the rest of the 16-bit line: Register-to-Register (RR), Short Format (SF for single-register operations), register-to-indexed memory (RX), and register immediate (RS). The RR and SF formats use one-word instructions. The RX and RS formats use two-word instructions. All instructions that pull an operand from memory can address up to 64K bytes directly. Addresses can be indexed by the contents of one index register.

The central processor has 16 general purpose registers. All 16 can be used as accumulators and 15 can be used as index registers. Up to 255 interrupt levels can be implemented. Interrupt response time is 7.75 microseconds. Memory for the Model 6/16 is on one board. It can be a core memory with a 1-microsecond cycle time or n-channel MOS memory with a 500-nanosecond cycle time. Core memory boards with 8K, 16K, 32K, and 64K bytes of storage are available. The MOS memory boards are available in 8K-byte increments beginning with 8K bytes up to the maximum capacity of 64K bytes. All memory modules have a single port of entry. Memory parity is optional.

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Input/Output

The Model 6/16 has the same I/O structure as the rest of the Interdata 16-bit line. DMA is standard, but devices interface to DMA via a standard multiplexor channel or optional selector channels. Up to four DMA channels can be implemented. The multiplexor and selector channels use one DMA channel. The other three DMA channels are available for user-designed interfaces to high-speed devices. Up to 255 devices can be connected to one 6/16 system. Maximum transfer rate over DMA is 2M bytes/second.

Packaging

The Model 6/16 is available in three combinations of chassis and power supply.

- Chassis with eight slots and 25 amp power supply: CPU and memory use one slot each; thus six slots are available for peripheral controllers and options.
- Chassis with eight slots and 50 amp power supply: CPU and memory use one slot each; thus six slots are available for peripheral controllers and options.
- Chassis with 16 slots and 50 amp power supply: CPU and memory use one slot each; thus 14 slots are available for peripheral controllers and options.

Peripherals

All the input/output devices available for the rest of the Interdata 16-bit line of computers are available for the Model 6/16. They include a broad range of printers, discs, magnetic tape units, and terminals.

Optional Features

Optional features include power fail/auto restart, binary or hexadecimal display panel, turnkey console, automatic loader, multiply/divide, selector channel, and Stretch/32.

Software

Software for the Model 6/16 is the same as that available for the 7/16. Software is unbundled and is available for a one-time license fee.

The major operating system is the OS16MT2, a real-time-based multitasking, multiprogramming operating system. It offers a subset of the features available in the OS32MT for the 32-bit processors.

Two FORTRAN compilers are available: one is extended FORTRAN IV and the other is FORTRAN V, an optimising compiler.

The assembler language is Common Assembly Language (CAL) for all Interdata processors.

A BASIC Interpreter, which implements a superset of Dartmouth BASIC, is also available.

Interactive debug and operating system edit routines are available for program preparation.

Competitive Position

The Model 6/16 is a must system for Interdata, a major contender in the minicomputer field. All major minicomputer manufacturers must offer a competitively priced system for entry-level users and OEMs. The system must be an entry into a compatible line that has substantial software and flexible configuration possibilities. Peripherals must include small-, medium-, and large-capacity discs, a variety of printers, and data communications interfaces as well as other conventional peripherals. A small entry-level system nested in this surrounding gives the customer something unavailable with all microcomputer systems except perhaps Digital's LSI-11. Interdata carries its supporting environment farther than most other minicomputer manufacturers. Interdata's small 16-bit computers can even be upgraded to its 32-bit Megaminis without too much trauma via a Stretch/32 option.

Table 1 compares the characteristics of the Model 6/16 with Interdata's former entry-level system, the Model 7/16. Model 6/16 is considerably faster and costs about 40 percent less than the Model 7/16.

Table 1. Interdata 6/16: Mainframe Characteristics Compared to Model 7/16

Processor Characteristics	Model 6/16	Model 7/16
CENTRAL PROCESSOR		
Type	Micropgm	Micropgm
No. of Internal Registers	16	16
Use	Accumulators: 15 index regs	Accumulators: 15 index regs
Addressing		
Direct (no. of words)	32K	32K
Indirect	No	No
Indexed	Yes	Yes
Max. I/O devices	255	255
Instructions		
Implementation	Firmware	Firmware
Number	104	104-125
Execution Times, μsec		
Fixed-Point Arithmetic		
Add/Subtract	3.00	3.25
Multiply	10.8*	42.00*
Divide	14.5*	56.00*
Floating-Point Arithmetic**		*
Add/Subtract	—	31
Multiply	—	44
Divide	—	69
User Microprogramming	No	No
Priority Interrupt System		
Lines		
Internal	1 std	1 std
External Levels	255	255

Table 1. (Contd.)

Processor Characteristics	Model 6/16	Model 7/16
Memory		
Type	Core/MOS	Core
Word Length (bits)	16	16
Cycle Time/Wd (μsec)	1.0/0.5	0.75/1.0
Capacity (words)		
Max	32K	32,768
Min	4K	4,096
Increment	8K/16K/32K core; 4K (MOS)	4K, 8K, 16K
Parity	Opt: 1bit/wd	Opt
Protect	Opt	Opt
ROM use	Implement processor logic	Implement processor logic
Writable Control Store	No	No
I/O Channels		
Programmed I/O	Std	Std
Direct Memory Access	Std	Std
No. of Channels	4	4
Selector Channel	Opt	Opt
No. of Devices Handled	16	16
Multiplexed Channel	Std, 255 devices	Std
Maximum Transfer Rate (words/sec)		
DMA via Selector Channel	1M	1M
PRICE of CPU & 32K-byte memory, $	$4,800 /4,000	6,800 /6,300

* Using RX format and optional hardware.
** To be announced later.

Table 2 compares the Model 6/16 with comparable systems from other manufacturers: Data General's Nova 3, Digital's PDP-11/04, and the General Automation GA-16/330. The Nova 3 is faster than the Model 6/16 and less expensive for the comparable configurations shown in the Table. The Nova 3 price is for a four-slot chassis, which has space for the processor, up to 32K words of memory, and one peripheral.

Prices for the 32K-byte and 56K-byte PDP-11/04 have not yet been announced. The Model 6/16 is faster than the General Automation GA-16/330 and also less expensive.

So far, Interdata has not announced a floating-point processor for the Model 6/16, although one is promised.

Interdata continues to add to its software as well as to its hardware offerings. The Model 6/16 is another indication that Interdata's 16-bit line is not being neglected for the more glamorous Megamini line.

Table 2. Interdata Model 6/16 Compared with Major Competitors

	Interdata Model 6/16	Data General Nova 3	Digital PDP-11/04	General Automation GA-16/330
Word Length, bits	16/16 + 1 parity	16/16 + 2 parity	16	16/16 + 2 parity
Inst. Times, μsec				
Add	3.00	1.8	3.2	4.6
Multiply	10.8*	6.9[1]	NA	21.2
Divide	14.5*	7.5[1]	NA	20.3
Fl.P. Add	(2)	7.7*	—	*
Fl.P. Multiply	(2)	11.3*	—	*
Fl.P. Divide	(2)	13.7*	—	*
Max Memory, bytes	64K	64K/256K	56K	128K
No. of GP Registers	16	4	8	16
Max DMA Rate, bytes/sec	2M	2M	2.8M	2M
Price, $				
CPU + Memory				
32K bytes	4,800/4,000	4,400[3]	(4)	5,250
64K bytes	8,200/7,700	7,100[3]	(4)	8,250
256K bytes	—	34,200	—	—

* Optional, at extra cost.
NA Not available.
— Not applicable.

Notes:
(1) Operands are unsigned integers on std.
(2) To be announced.
(3) Nova 3/4 in 4-slot chassis.
(4) Digital has not announced price of unbundled memory although the 11/04 can support 56K bytes. Price for 16K-byte system with 9-slot chassis is $3545.

PRICE DATA

Central Processor and Working Storage	Purchase Price $
Equipment	
Model 6/16 CPU in 8-slot chassis, 20 amp power supply, and memory	
With Core	
8K Bytes	2,800
16K Bytes	3,300
32K Bytes	4,800
64K Bytes	8,200
With MOS	
8K Bytes	2,200
16K Bytes	2,800
24K Bytes	3,700
32K Bytes	4,000
40K Bytes	4,600
48K Bytes	5,500
56K Bytes	6,600
64K Bytes	7,700
Substituting 50 amp for 20 amp power supply	500 - 900 (depending on configuration)
Substituting 50 amp for 20 amp power supply and 16-slot for 8-slot chassis	1,000 - 1,300 (depending on configuration)
Optional Features	
Memory Parity Logic	500
Power Fail/Auto Restart	400
Binary Display Panel with Hexadecimal Input Keyboard	300
Hexadecimal Display Panel and Keyboard	600
Display Interface for Binary Display, Hexadecimal Display, or Turnkey Console	100
Turnkey Console for power initialize, and execute	100
Automatic Loader for OS/16 MT2 Loader or Custom-designed Loader	300
Signed Multiply/Divide for 16-bit operands	950
Selector Channel	1,000
Stretch/32 Field Upgrade to software and I/O-Compatible 7/32	5,000
Software	
OS/16 MT2	1,400
MACRO CAL	300
BASIC/16	300
FORTRAN IV	250
FORTRAN V	500
ITAM/16	1,200

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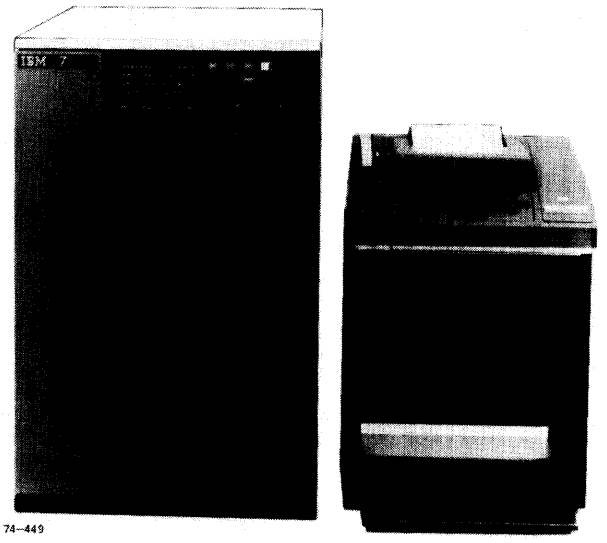
System/7 System Report



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OVERVIEW

IBM's System/7 is a small processor designed to excel in real-time data acquisition, laboratory automation, process control, and data communications applications. It is designed to operate as a small, stand-alone system for sensor-based applications or as a front-end to a host computer.

IBM offers A, B, and E Series of System/7 processor models. The A and B Series are identical in almost all respects; their memory capacity is the same, but they differ in their ability to function as front-end processors with other IBM computers. Model Bxx (xx is memory size) interfaces directly with the IBM 1130 computer; Model Axx communicates with the IBM 1800, System/360, or System/370 computers via an asynchronous or bisynchronous communications interface. Model Axx can also operate as a stand-alone system. Model Exx is most like Model Axx, but its memory capacity is much larger. Model Exx supports both synchronous and asynchronous data communications. It also has seven additional instructions in its instruction set and has memory protection facilities. Memory protection, however, is not supported by system software.

Main storage is monolithic; capacity ranges from 2K to 16K 18-bit words (one parity bit for each eight-bit byte) for Axx and Bxx models and from 16K to 64K words for Exx models. Memory cycle time is 400 nanoseconds per word. Standard peripheral equipment support for the System/7 includes an operator station with keyboard, printers, and paper tape input/output; communication interfaces; a wide variety of analog/digital and digital/analog equipment; sensing devices; and disc storage. Disc storage can consist of up to eight 5022 cartridge discs (fixed or removable versions) with a 1.2M or 2.4M-byte capacity and/or the 3340/3348 disc subsystem, an extremely fast high-capacity system that can store up to 34.2M bytes per drive and 273.6M bytes per eight-spindle subsystem. Thus, a maximum of 292.8M bytes of disc storage can be attached to a System/7. Moreover, the 3340/3348 can operate in a 5022 emulation mode for program compatibility or greater flexibility in access methods. A fixed-head option (0.480M bytes per spindle) is available, but the rotational position option sensing is not software supported.

Software for the System/7 allows it to function as a memory-based or disc-based stand-alone process control or DDC system, a front end for the 360/370, 1130, or 1800, a message-switching system, or a member of a distributed processing network. The MSP/7 software has to be expanded to provide a multiprogramming foreground/background system. The software combined with the addition of 3340 disc subsystems increases the flexibility of the System/7 and strengthens its competitive stance. The Executive Feature MSP/7 provides for up to 16 partitions for real-time multiprogramming. One partition can be used for on-line batch processing program preparation, various service routines, or user batch programs.

A number of custom products and features are also available for specific applications, such as for inquiry/response or data communications systems.

The System/7 central processor features two interval timers, four processing levels with 16 sublevels each, an adapter for the 5028 Operator Station, seven index registers, one program counter, and one accumulator. Each processing level has power-failure detection with automatic Initial Program Load (IPL). Internal air isolation allows use of the system in hostile environments. Switching time from one level to another is 800 nanoseconds.

The air isolation feature protects System/7 from atmospheric contaminants that may be present in industrial

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or laboratory environments. Internal air is recirculated through activated charcoal filters to absorb contaminants, and internal heat is dissipated via an air-to-air heat exchange that is part of the feature.

System/7 is designed to operate under severe physical conditions: temperature ranges from 40 to 120 degrees Fahrenheit and relative humidity ranges from eight to 85 percent are tolerable during operation. Thermal warning sensors sound an alarm when the temperature exceeds normal operating limits; and thermal shutdown occurs if component damage is imminent.

This rather impressive set of features and selected peripherals allows System/7 to compete in many application areas: data acquisition, process control, plant automation, and data communications. Table 1 lists the System/7 mainframe characteristics.

IBM announced System/7 A and B Series on October 28, 1970. First deliveries were made in the last quarter of 1971. The E Series was announced in July 1973 and first delivered in December 1973. The 3340/3348 disc subsystems, which are standard RPQ items, are scheduled for delivery in May 1976.

COMPETITIVE POSITION

IBM is naturally in a strong competitive position with respect to other vendors of front-end processors for its 1130, 1800, System/360, and System/370. Many corporations prefer one major supplier because equipment-related problems become the supplier's responsibility. IBM caters to this preference by offering user training and technical expertise in application areas.

Many corporations in the industrial community also understand the advantages of multiple suppliers and the need to practice economy in data processing operations. Most minicomputers can communicate with large IBM systems via binary synchronous communications facilities. Under these constraints, System/7 must prove its worth.

Initially, the System/7 had extremely limited expansion capability in comparison to other minicomputers, not only in peripherals but in main memory capacity, which was only 16K words. The E Series quadrupled maximum memory capacity from 16K to 64K words and offered memory protection. IBM has also expanded the standard

Table 1. IBM System/7: Mainframe Characteristics

Characteristic	5010 Model A	5010 Model B	5010 Model E
Announced	October 1970	October 1970	July 1973
Memory			
Type	Monolithic SS	Monolithic SS	Monolithic SS
Word Length (bits)	16	16	16
Cycle Time/wd (nsec)	400	400	400
Capacity (wds)			
Min	2048	2048	16,384
Max	16,384	16,384	65,536
Increment Size	2048	2048	4096
Parity	1 bit/byte	1 bit/byte	1 bit/byte
Protect	None	None	Yes(1)
Central Processor			
No. of Internal Registers	4 sets of 9	4 sets of 9	4 sets of 9
No. of Instructions			
Std	39	39	46
Opt	–	–	–
Addressing			
Direct (no. of wds)	Short: 255 Long: 16,384	Short: 255 Long: 16,384	Short: 255 Long: 16,384
Indirect	None	None	None
Indexed	Yes	Yes	Yes
Priority Interrupt System			
Lines	4	4	4
Levels	16/line	16/line	16/line
I/O Channels			
Programmed I/O	Yes	Yes	Yes
Direct Memory Access (DMA)			
No. of Channels	1	1(2)	1
Multiplexed I/O			
No. of Subchannels	–	–	–
Max Transfer Rate (wds/sec)			
Within Memory	625,000	625,000	625,000
Over DMA	250,000	250,000	250,000

Notes:
(1) Memory protect supported by Executive/7 System software only.
(2) The 1130 attachment provides direct memory access but does not provide block transfer of data.

peripherals to include interactive consoles, card equipment, greatly increased disc storage, and serial as well as line printers, all software-supported.

The System/7 is a well-designed system and features an advanced logical and technological architecture. It uses all semiconductor solid state memory with a 400-nanosecond cycle time. The processor always operates in one of four priority interrupt levels, and it can switch from one interrupt level to another in 800 nanoseconds. Each level has its own set of internal registers, and processing at the new level can begin immediately, once the context is switched. Its architecture lends itself to real-time, sensor-based, and data communications applications.

IBM originally had chosen to market System/7 as a sensor-based front end for its 1130, 1800, System/360, and System/370 systems. Initially, the software for a stand-alone System/7 was rudimentary, and program preparation facilities resided in Modular System Program support (MSP/7) incorporated in the software of a host computer: 1130, 1800, System/360, and System/370. This is still offered, but IBM now also offers the MSP/7 program preparation facilities for the System/7. MSP/7 support includes a macro assembler, FORTRAN IV compiler, linking editor, formater, and disc support.

System/7 started out as a powerful, small system surrounded by configuration and software constraints that made it almost inextricable from larger IBM systems. Stand-alone systems were practical only for dedicated applications. IBM is gradually loosening the constraints on the System/7, and configurations for general-purpose processing are now feasible. System/7's expanded standard peripheral offerings, expanded disc storage, multiprogramming software, and greater stand-alone capabilities enable it to be used for a wide variety of new applications.

System/7 is extremely fast and can compete with top-of-the-line minicomputers in sheer processing power. Its 64K-word memory capacity and program preparation facilities make it competitive with other minicomputers on the market. Even though many minicomputer manufacturers (Digital Equipment and Data General, for example) have more developed foreground/background multiprogramming systems — some designed to mix real-time, time sharing with a batch stream — the addition of the present version of MSP/7 will make the system attractive to users because of the overall system speed and IBM's reputation.

Despite its speed and performance characteristics and its IBM label, System/7 has not been a booming best-seller. IBM has not marketed it aggressively or packaged it to compete very well with other minicomputer systems. The software constraints and the RPQ status of many peripherals make it appear to be a reluctant contender. Large discs are now available, but they too are RPQ items. System/7 still seems to be a caged animal that is allowed out only under controlled conditions with the trainer retaining strict surveillance on keys to the cage.

USER REACTIONS

All System/7 users we contacted were pleased with the performance of the System/7.

One user selected it because it was reliable and fast and was backed up by IBM. Also, IBM first presented the possibility of sensor-based computing for his application. This company uses the System/7 as a front end to a System/360 Model 30 to monitor film processing. The company is expanding the system to control all laboratory functions, including process control and personnel record keeping. System downtime has been minimal and maintenance has been complete and comprehensive. This user finds the software good, the programming language easy to use, the hardware reliable, and the interfacing sensor-based devices simple.

A second user has installed a factory data collection system built around the System/7 and the System 370 Model 125. The System/7 was selected because it was cheaper than its major competitor for the data collection application at the time it was installed. Although the company had some problems with the 2790 system initially, these were ironed out and the whole system now runs smoothly. The System/7 itself ran well from the start. The company has a great deal of time left over on the System/7 but does not have any use for it because the 370 system manipulates and processes the data from the shop floor.

A third user has a stand-alone System/7 with 55 card readers to control the various gates and doors of an airport. The system is installed and operating. Downtime was less than five percent during startup.

Software houses and service bureaus often have very good overall views of a system's strengths and weaknesses. We interviewed two who were engaged in creating different types of data collection and process control systems based on System/7s. They successfully compete with IBM's software development groups because of expertise in particular process control areas. One user remarked that his company takes full responsibility for its installations: hardware interfacing, software development, and system maintenance. These companies also sell packaged systems, based on other minicomputers.

Frequently, control or collection systems are developed utilizing existing System/7s used part time for other purposes. Both of the users characterized the System/7 as an excellent piece of equipment, reliable and well-supported by IBM. One user pointed out that other minicomputer manufacturers survive because they price their systems lower. The other user had one criticism, which he labeled "very minor": IBM makes more software changes than necessary when adding enhancements, making the reprogramming to incorporate enhancements more extensive. tensive.

CONFIGURATION GUIDE

System/7 operates either as a stand-alone computing system or a satellite processor linked to a host processor that is on-site or at a remote location. The system is structured independently of a host processor and is configured according to its application. A system consists of a central processor module and from one to 11 I/O modules housed in the appropriate 5026 enclosure. An I/O module is equivalent to a device controller. The 5026 enclosure provides the cabinetry, power supply, and physical interface connections. Memory and the Direct Control Channel (DCC) are part of the central processor module. The DCC includes the host-processor interface, the operator-station interface, and the two interval timers. Peripherals are listed in Table 2.

Basic Configuration

The most basic stand-alone configuration includes an A02 processor with 2048 words of memory and one I/O module housed in a nonexpandable 5026 enclosure (Model A2). This configuration also includes an operator's console with paper tape facilities. An operator station is required with each configuration, but multisystem configurations can share a single station. Program preparation via an assembler requires a minimum of 4096 words of memory.

The basic configuration of a System/7-1130 installation includes a B02 processor with 2048 words of memory and one I/O module housed in a nonexpandable 5026 enclosure (Model A2).

Model B includes the 1130 attachment, which interfaces with the 1130 Storage Access Channel (SAC).

Expanded Configuration

The 5026 enclosure contains power and internal interface connections for the processor, memory, and input/output modules. There are five enclosures that can be used in various combinations for configuring a system. A system, however, can include a maximum of 11 I/O modules.

5026 Model	Accommodates
A2	1 CPU and 1 I/O module
C3	1 CPU and 2 I/O modules
C6	1 CPU and 5 I/O modules
D3	3 I/O modules
D6	6 I/O modules

Model A2 is not expandable; Models C and D contain multiplexors that allow I/O expansion, and they also accept the air isolation feature. Model D can be 200 feet from Model C so that contaminants, humidity, or temperature that affect it do not affect the central processor.

A/D Equipment Configuration

The input/output model is the basic building block for sensor-based I/O on System/7. Each module is self-contained and houses all the hardware to provide I/O functions. All I/O modules are interchangeable and can occupy any position except the processor position in the 5026 enclosure.

Three I/O modules are available for special equipment: the 5014 Analog Input Module, (Models B, C, D, and E); the 5013 Digital Input/Output Module; and the 5012 Multifunction Module. The 5014 can handle up to 384 input points. The 5012 handles analog/digital subsystems (up to 128 digital inputs, 64 digital outputs, 32 analog inputs, and two analog outputs) and the 2790 Communications

Table 2. IBM System/7: Peripherals

Model Number	Description
DISCS	
5022	
-001/-002	One fixed, 1 removable disc; 2.44M wds; 269/126-msec access
-003/-004	Fixed disc, 1.22M wds; 269/126-msec access
PRINTERS	
5024	80 to 155-lpm line printer
7431	85 or 115-cps dot matrix
CARDS	
2502	300-cpm reader
129	50- or 90-cpm reader, 12 to 50-cpm punch
5028	Keyboard printer with paper tape I/O
ANALOG/DIGITAL	
5012	Multifunction analog I/O and digital I/O module, 32 analog input pts
5013	Digital I/O, up to 128 input and 64 output pts
5014	Analog input, up to 128 pts; speed ranges from 200 pts/sec to 20K pts/sec
COMMUNICATIONS	
1610	Async communications
2074	Binary sync adapter
–	1130 channel attachment
2790 DATA COMMUNICATIONS (RJE)	Up to 16 2791/2793 area stations
8185	Control for up to 16 subsystems of 16 data entry stations each, up to 128 displays
2795/6/7	Card and badge readers
2798	Guidance display 12/subsystem
1035	Badge reader
1053	Printer
CUSTOM PERIPHERALS (RPQ)	
5029	Magnetic stripe card reader
5096-NI	Digital input multiplexor
5098-NI	Teleprocessing multiplexor, 16 lines
5098-N3	BSC module, 4 lines
5098-N5	Sensor-based control connects 64S/7 to S/370
7414-1	Interactive console (CRT, 480, or 960 char)
1017/1018	Paper tape attachment
–	Tape cassette records
–	Async comm for 1200 or 50K bps
SBCU/SBCA	System 360/370 channel attachment
3340/3348 Disc Subsystem	Up to 8 3348 discs per 3340; up to 34.2M words per data module in "native" mode; or 29.4M wds in 5022 emulation mode

Subsystem, which are remote data-entry equipment peculiar to plant automation. The 5013 modules provide for attachment of 128 digital inputs, 64 digital outputs, the 2790 control, and special devices.

Other Expanded Configurations

The 5022 Disc I/O Module occupies one position in the 5026 enclosure. Only one disc module can be mounted in an enclosure, and a maximum of eight 5022s are allowed per system. Modules not mounted in an enclosure require a 4650 Integral Power Supply. One 5022 disc provides 2.44 million words (Models 1 and 2) or 1.22 million words (Models 3 and 4).

The 3340/3348 disc subsystem differs from the 5022 in that an entire string of eight drives can attach to one enclosure "shelf" position via the D08331 Attachment Module. The D08331 attaches to a C3 or C6 enclosure; the C3 (but not the C6) requires the D08332 power supply option.

A D08331 is required for each Model A2 drive (two spindles). The A2 can then attach three more "B" drives, which can be either Model B1 (one-spindle) or Model B2 (two-spindle) drives. Each spindle can hold a Model 35, 70, or 70F pack. The storage-byte capacity is 17.1M words for the Model 35 and 34.2M words for both Model 70 and Model 70F. The 70 and 70F packs differ in that the Model 70F has five fixed heads and one movable head, whereas the Model 70 has one movable head.

The 3340/3348 subsystem can operate in a 5022 emulation mode, called "7 mode." This allows program compatibility with existing installations and a greater variety of access methods. Up to 12 5022 drives can be emulated, but this reduces total pack capacity because of the small record sizes. Maximum capacity in emulation mode is about 29.4M words for one pack.

A System/7 can use both emulation and native modes on the same subsystem. A System/7 can also use both 5022 and 3340 drives on the same system.

The optional asynchronous or bisynchronous communications feature on Processor Models A and E occupies the same space in the processor as the 1130 Channel Attachment on B models. These features are manually exclusive. The asynchronous communications feature with a line adapter can transmit data at a rate of 134.5 or 600 bits per second. Bisynchronous communications operate in half-duplex mode at a wide range of speeds: 1200, 2000, 2400, and 7200 bits per second and above. The channel attachment transmission rate is based on the cycle-stealing capability of the 1130 processor.

Software Configuration Requirements

The configurations demanded by the basic system software packages are listed in Table 3.

Table 3. IBM System/7: Software

PACKAGE	DESCRIPTION
MSP/7	Modular System Program for system control; with Disc Support System (DSS/7), requires disc, console, and 4K wds memory if program preparation on host; 8K to 12K wds if stand-alone version with program preparation on System/7
Executive/7	Adds real-time multiprogramming on-line background batch to DSS/7 level support, storage protection, 3340 disc subsystem support, and other features
ASM/7	Macro Assembler, requires 4K-wd memory, console
PREP/7 (HOST ASM/7)	Cross Assembler Link Editor and Loader for program preparation on 360/370; DOS/VS requires 14K bytes of exclusive storage, 3 disc or tape units; OS/VS requires 44K bytes of exclusive storage
HOST PROGRAM (PREP II)	For program preparation on 1130 or 1800; requires same configuration as 1130 or 1800 macro assemblers and linkage editors
FORTRAN IV	Stand-alone or host versions; stand-alone version requires 12K-wd memory, disc, console
UTILITIES	LINK/7 Linkage Editor, Format/7 formating Loader, enhanced macro library/relocatable
AML/7	Application Module Library, a set of applications-oriented macros
CCAP/7	Stand-alone Message-Switching Control Program
PCP/7	Process Control Program for monitoring, DDC control
APG/7	Application Program Generator runs on host 360/370 to generate programs using AML/7 macros

COMPATIBILITY

System/7 is not program compatible with any other system produced by IBM; it is marketed, however, as a front end for a host computer — IBM 1130, IBM 1800, System/360, or System/370. Data compatibility with these processors is maintained via the 16-bit word, which contains two eight-bit bytes. The host computers not only prepare programs for System/7, but they also transmit object programs to System/7 for execution. In addition the host computer can perform System/7 initial program load.

System/7 can communicate with System/3 via BSCA facilities.

The Axx and Bxx models of the System/7 are identical except for external interfaces. Except for the Disk Support System 7 (DSS/7), the user must provide or coordinate the basic control software for System/7. Any physical change that affects either addressing or other I/O service becomes his responsibility. It is expected that without standards for processor organization, there will be little if any program compatibility between systems. Reassembly of programs appears mandatory.

The MSP/7 program preparation facilities under DSS/7 (or EXECUTIVE/7) versions for stand-alone

System/7 configurations are compatible with host computer preparation facilities. IBM releases enhancements to stand-alone and host FORTRAN program products simultaneously to maintain compatibility.

Programs developed for the Model A will run unmodified on a 16K-word Model E, but programs must be reassembled to run on models with more than 16K words.

When a 3340 disc subsystem is added to a system, it can be operated in emulation mode to achieve compatibility with programs developed for 5022 discs. For 3348 packs to be data compatible with S/370 they must be recorded in native mode.

MAINTENANCE AND SUPPORT

As the largest computer manufacturer in the world, IBM has the most widespread sales and service facilities, reaching into all corners of the globe. Part of IBM's success has been attributed by many industry observers to the efficiency and broad services offered by the sales and service network.

IBM provides a variety of maintenance contracts, depending on what the user needs and can pay for. The standard prime shift maintenance contract provides for prompt emergency service.

TYPICAL PRICES

Model Number	Description	Monthly Rental (Incl Maint.) $	Purchase Price $	Monthly Maint. $
	IBM SYSTEM/7			
	CENTRAL PROCESSOR AND WORKING STORAGE			
5010-(1)	System/7 Processor with Integral Memory Modules			
A02	2,048 Words	199	8,670	51
A04	4,096 Words	313	12,400	63
A08	8,912 Words	541	19,900	87
A10	10,240 Words (requires 7401 over 8K words)	654	23,600	99
A12	12,288 Words	767	27,400	111
A16	16,384 Words	994	34,900	135
B02	2,048 Words	307	12,700	60
B04	4,096 Words	421	16,400	72
B08	8,192 Words	649	23,900	95
B10	10,240 Words (requires 7401 over 8K words)	762	27,700	107
B12	12,288 Words	876	31,400	120
B16	16,384 Words	1,100	38,900	144
E16	16,384 Words	1,010	35,400	247
E20	20,480 Words	1,155	40,300	281
E28	28,672 Words	1,440	49,900	347
E32	32,768 Words	1,590	54,700	379
E36	36,864 Words	1,740	59,500	413
E44	45,056 Words	2,025	69,200	478
E48	49,152 Words	2,175	74,000	512
E52	53,248 Words	2,320	78,800	544
E60	61,440 Words	2,610	88,500	611
E64	65,536 Words	2,755	93,300	644
7401	Storage Power Addition (for A2)	16	652	1
2662	Cycle Steal Basic	48	1,830	3
5026-	Processor Enclosure for Processor and Up to 11 I/O Module Positions			
A02	1 I/O Position	108	4,710	26
C03	2 I/O Positions	248	10,200	31
C06	5 I/O Positions	367	14,400	50
D03	Extension of C3/C6 by 3 I/O Positions (requires 3715)	248	10,200	40
D06	Extension of C3/C6 by 6 I/O Positions (requires 3715)	367	14,400	59
3715	Dx Enclosure Attachment	37	1,420	5
4621	Internal Air Isolation (for C3/D3)	48	2,290	12
4622	Internal Air Isolation (for C6/D6)	65	3,060	24
5731	Power Failure Detect and Restart (1/enclosure)	54	2,040	1
7401	Storage Power Addition (for C3/C6)	17	652	1
5028-(1)	Operator Station (incl keyboard/printer and 10-cps paper tape reader/punch)	150	2,280	51
	MASS STORAGE			
5022-	Disc Storage Module			
001	1 Removable, 1 Fixed Disc; 2.44M Words; (269 msec)	421	15,100	91
002	Same as 001 except 126 msec	492	16,500	100
003	1 Fixed Disc; 1.22M Words; Avg Access Time (269 msec)	324	13,500	87
004	Same as 003 except 126 msec	394	14,800	95
4650	Integral Power Supply	37	1,420	1
2664	Disk Cycle Steal	16	612	1
5440	Disk Cartridge (for 5022-001, 002 only)	NA	NA	NA
3340-A02	Two Discs and Control	1,059	40,000	80
3340-B01	One Disc Drive	592	22,000	43
3340-B02	Two Disc Drives	747	28,000	69
D08-331	Interface for 3340	1,125	39,375	168
D08-332	Power Supply (to attach D08331 to C3 enclosure; not needed for C6 enclosure)	32	1,120	1
4301	Fixed-Head Feature	47	1,900	2
3348-35	Removable Data Modules for 3340 (34M bytes)	59	1,600	–
3348-70	69M- or 41M-byte Removable Data Module	82	2,200	–
3348-70F	69M-byte Removable Data Module	165	4,400	–
	INPUT/OUTPUT			
5012-A01	Multifunction Module (requires 8185)	42	1,830	8
4115	5024 Attachment Feature	30	1,320	4
5024-1	Provides space, power, and logic to connect line printer to CPU (includes line printer)	482	18,040	71
5024-2	Provides space, power, and logic to connect card reader to CPU	276	10,340	13
5024-3	Combination of Models 5024-1 and 5024-2	640	22,500	77
	DATA COMMUNICATIONS			
	Asynchronous Communications			
1610	Async Communications Control (5010-Axx models only)	81	3,060	14

TYPICAL PRICES (Contd.)

Model Number	Description	Monthly Rental (Incl Maint.) $	Purchase Price $	Monthly Maint. $
		10	408	2
2165	Commom Carrier Adapter	27	1,020	15
4750	Line Adapter — Limited Distance Type 2B	27	1,020	15
4751	Line Adapter — Leased Line Type 1A	27	1,020	15
4752	Line Adapter — Leased Line Type 1B	194	7,340	59
2074	Binary Sync Communication Control	21	818	3
4703	Internal Clock	27	1,020	3
4800	Line Interface Type 1D	54	2,040	1
4805	Line Interface Type 1G	16	535	3
5500	IBM 1200 bps Integrated Modem, Leased	21	714	3
5501	IBM 1200 bps Integrated Modem, Switched			
	Remote Data Entry	108	4,080	8
8195	2790 Control (for up to 16 2791/2793 area stations; requires 5012 and 8195; only one 8195/system)	198	8,400	45
2791-001	Area Station Controller (for up to 16 units)	10	510	1
3330	Digital Device Read-In	10	510	1
3690	External Alarm Contacts	146	6,920	45
2791-002	Area Station Controller (used as I/O station without adapters)	130	6,180	19
2793-001	Area Station Controller (for up to 8 2795/2796/2797 units; can support one 8296 Extension Unit, one 1053 Attachment, and the following units)	96	4,400	19
2798-001	Guidance Display Unit (up to 12/area station; max 128)			

Notes:

(1) Axx models can support a 1610 Async Communications Control for communication via communications lines with the IBM 1800 and Systems/360 and 370; the Bxx models include an 1130 Host Processor Attachment for direct storage-to-storage communication with the IBM 1130.

— Not Applicable
NA Not Available

OVERVIEW

The SUE (System User Engineered) Computer systems, like their predecessors the MAC 16 and MAC Jr., are designed, marketed, and supported by the Lockheed Electronics Data Products Division, primarily as an OEM product; SUE systems are offered to the business end user as the System III product line. SUE systems are not compatible with the MAC 16 and MAC Jr., but a translator program is available for SUE to translate MAC machine language programs into SUE machine language programs.

SUE processors are 16-bit, byte- or word-oriented microprogrammed processors. Addressing is to the byte level. The SUE is the basic general-purpose system with a 108-instruction set. SUE-SIS designates a scientific version with 38 added instructions in the control ROM. Single processors can support up to 32K words of core.

The SUE systems are modular and flexible. A system can vary from an Infibus controller with user-designed modules to a multiprocessor configuration with up to four SUE processors. Multiprocessor configurations can handle up to 80K words of core by mixing dedicated and common memory banks. SUE is designed to protect the user from system obsolescence by making it easy to add new technology on a function basis. This is accomplished by designing the system around a central bus system called the Infibus, over which system modules communicate with each other on a signal-response basis. System modules operate asynchronously with respect to each other and are synchronized only for information transfer cycles.

Mainframe characteristics are summarized in Table 1. The central data bus architecture is similar to that of DEC's PDP-11 and Hewlett-Packard's HP 3000. SUE will compete with the low end of the PDP-11 line, specifically the PDP-11/05 and 11/15, which are aimed toward the OEM market, particularly the communications sector.

System software includes a Basic Operating System, a foreground/background Disc Operating System, an IOCS operator communications package, various utilities, and, recently, Fortran IV. Peripherals include discs, terminals, slow-speed devices of various kinds, and communications interfaces. Lockheed plans to introduce a multiprocessing operating system, BSC communications, and 2780 emulation during 1975.

The first SUE was delivered in March 1972. Over 2,000 systems have been delivered to date.

Table 1 lists the SUE's mainframe characteristics.

Table 1. Lockheed Electronics SUE: Mainframe Characteristics

CENTRAL PROCESSOR	
Microprogrammed	Yes
No. of Internal Registers	8 general-purpose
Addressing	
Direct (no. of words)	32K (doubleword instructions); 256 (singleword)
Indirect	Multilevel
Indexed	Yes
Instruction Set	
Number	108 (std), 146 (opt)
Decimal Arithmetic	Subroutine
Priority Interrupt	
System	
Lines	4
Levels	4 (unlimited sharing)
MAIN STORAGE	
Type	Core
Cycle Time (nsec)	800
Basic Addressable Unit	Byte/word
Bytes per Access	1 or 2
Ports to Memory	1
Min Capacity (bytes)	2K
Max Capacity (bytes)	64K
Increment Size (bytes)	8K; 16K
Parity	RPQ
Protect	RPQ
ROM	
Use	Control memory
Capacity (bytes)	256 or 512K, 2K possible
I/O CHANNELS	
Programmed I/O	Yes
DMA Channels (no.)	Yes (unlimited no.)
Multiplexed I/O	Yes
Max Transfer Rate (words/sec)	
Within Memory	2.2M (overlapped core)
Over DMA	5M

Competitive Position

The SUE competes primarily in the OEM market. Its software supports assembly language and Fortran programming, under core-based and disc-based operating systems. LEC provides discounts of up to 37 percent for quantity purchases of SUE systems. Discounts do not apply to peripheral devices because LEC buys the devices and provides only the controller interface. The company has sold SUE to communications, data entry, and COM systems OEMs, among others.

Competitors to the SUE include the DEC PDP-11/05 and 11/15; Computer Automation LSI Alpha 16 and Naked Mini 16; General Automation LSI SPC-16, Data General Nova 2, and Microdata 1600. Because SUE is similar in architecture to the PDP-11 and Digital is a large minicomputer manufacturer, it is not surprising that SUE's most vigorous competitor is the PDP-11.

LEC markets SUE chiefly in the communications and process control OEM markets. The introduction of the new DOS should make the system more competitive in these areas. This operating system is of the foreground/background type with one multitasking program operating in the foreground and one batch program operating in the background. Operating systems for real-time and multiprocessor applications will be developed later.

LEC has one advantage over many minicomputer manufacturers in the OEM market: it is a large core memory

supplier to the computer industry as a whole. Consequently, the cost of core memory for its system is low and total system cost is low.

User Reactions

SUE users we contacted were in accord both about the excellent SUE hardware, particularly for the OEM market, and the need for LEC to step up the pace of its software development. A spokesman for a cancer research group, using the system as the heart of a multiparameter analyzer for cells, went so far as to call the hardware design and overall system reliability, "Excellent enough to make Lockheed number 2 in the minicomputer market if the company would market the system more aggressively and concentrate more on software development." An OEM manufacturer developing the SUE as a communications network processor explained that the SUE is unique in the minicomputer market — the arbitration function that determines which component has control of the Infibus is separate from the CPU. Thus, it is easy to use the system building blocks in a multitude of patterns. This company developed a bus connector to allow both multiprocessor systems and multibus systems, some with memory, peripherals and processors on different busses.

CONFIGURATION GUIDE

A SUE computer system consists of a card frame guide; an Infibus and controller; power supply; SUE or SUE-SIS processors; up to 32K words of memory per processor; a control panel; and a universal serial or parallel controller for each peripheral device in the system.

The processors, like all other pluggable system modules, connect to the Infibus, which is in turn controlled by the Infibus controller; also like other pluggable modules, processors can be mixed in a multiprocessor system. Up to four processors can be connected to one Infibus.

The processor models differ basically in the functions they can perform rather than any effect on system configuration. The "SIS" models add instructions to the standard SUE to create a processor suitable for scientific processing and Fortran programming. The master processor is designated by proximity to the Infibus controller in a multiprocessor system, rather than by model. Model numbers are designated as SUE or SUE-SIS 1004, 1008, 1016, 1024, or 1032 depending on the number of words of memory included with the basic CPU.

A chassis consists of an Infibus and the card frame guide. All system modules are mounted on circuit cards that slide into a card guide slot and plug into the Infibus. Twenty-four slots are available for mounting system modules. An internal power supply requires eight slots; if an external power supply is used, other system modules can use the eight power supply slots.

Memory can consist of 4K- or 8K-word core memory modules. Any number of memory modules can be intermixed on a system, provided the total does not exceed 32K words in a single-processor system. Multiple processors can handle up to 80K words in one system by combining 16K dedicated memory banks with a 16K common area. Each core module requires three card slots. Effective memory capacity is limited to 30K words per processor, because the upper 2K-memory word addresses are reserved to address I/O device registers.

Each parallel or serial I/O controller requires one card slot. A block transfer adapter that requires one slot must be inserted next to each controller that needs block transfer capability.

Peripheral devices include Teletype units, high-speed paper tape reader/punch, card reader, line printers, industry-standard magnetic tape units, displays, discs, and asynchronous data communications controllers. A universal logic board is available for designing interfaces for special-purpose devices. The peripheral devices are listed in Table 2.

The 1825 Bus Extender allows two Infibuses to be connected to increase the system card slot capacity. Two SUE systems connected to a common Infibus via communications modules can communicate to obtain many of the advantages of a system doubled in size, including a wider variety of peripherals. The interrupt priority level of the intersystem communication modules can be assigned to any level desired by the system engineer and can be positioned on the Infibus to any priority within its assigned level. Software packages for the SUE with configuration requirements are listed in Table 3.

Table 2. Lockheed Electronics SUE: Peripherals

Model No.	Description
Disc	
6755	IBM 5444 compatible unit, one fixed and one removable cartridge, 2.5M bytes/disc, 4 drives/controller
Terminals	
6710	Teletype, ASR 33, 10 cps
6762	Printer Terminal, 100 cps
6770	CRT Terminal, 960 char
Printers	
6765	Line Printer, 200 lpm
6768	Line Printer, 600 lpm
Cards	
6733	Card Reader, 600 cpm
6734	Card Reader, 285 cpm
Paper Tape	
6717/18	Paper Tape Readers, 300 cps
6723	Paper Tape Punch, 75 cps
6719	Combination 6718 and 6723
Communications	
4651	Async Modem Controller, single line, 300/1200/1800/4800 baud
4530	Four-channel Async MUX to 9600 baud
4502	Serial I/O Controller, RS232C and 20mA polar control
4501/3/6	Parallel I/O Controller, TTL compatible

Table 3. Lockheed Electronics SUE: Software

Package	Description
DOS	Disc Operating System, foreground/background system, requires CPU, 16K words of core, disc, TTY, Card Reader; available mid 1975
BOS	Basic Operating System, includes loaders, I/O control system, Operator Utility Interface Package (OUIP), Debug, CPU Test, Memory Test, Peripheral Tests; requires 4K words of memory and Teletype; can support FORTRAN IV and assemblers.
FORTRAN IV	ANSI X3.9 - 1966 standard, requires CPU, 8K words of core, TTY.
Assemblers	Basic assembler requires 4K words and Teletypes while the Macro assembler requires 8K words and Teletype.

Compatibility

The SUE is not compatible with any other computer. Lockheed's System III product line is based on the SUE system so programs written in Fortran IV or assembly language are interchangeable, given comparable configurations. Programs developed for LEC's MAC 16 and MAC Jr., can be translated into SUE machine language code; the translator runs on SUE. Cross assemblers are available for the MAC 16 and the IBM System/360 so that SUE assembly language programs can be assembled on the MAC 16 or IBM System/360. A SUE simulator written in Fortran is available so that SUE-assembled object code can be tested or executed on any larger computer system that supports ANSI standard Fortran.

MAINTENANCE

Lockheed provides two types of maintenance contracts — a preventive maintenance contract with an extra emergency service charge per visit and an inclusive contract that provides both preventive and emergency service for a single fee. The Field Engineering Department has offices located throughout the United States. Repairs can also be handled at either the local service center or at Los Angeles headquarters. A 10-day course in the basic maintenance of a SUE system is offered free of charge for each SUE customer.

TYPICAL PRICES

Model Number	Description	Purchase $
	SUE Central Processor Systems include 16 slot chassis, SUE INFIBUS, integrai power supply panel and bezel, power distribution unit and cooling fans; CPU includes 8 general purpose registers, basic instruction set of 108 instructions, 4 levels of shared priority interrupts, power monitor/auto restart and real time clock; core memory full cycle time is 800 nsec	
1004	CPU with Primary Instruction Set and 4,096 words of 16-bit Core Memory	4,350
1008	1004 with 6,192 words of 16-bit Core Memory	5,950
1016	1004 with 16,384 words of 16-bits of Core Memory, 24 slot Chassis, External Power Supply	7,945
1024	1016 with 24,576 words of 16-bit Core Memory	9,945
1032	1016 with 32,786 words of 16-bit Core Memory	11,445
1004/8/16/ 24/32 SIS	CPU with Scientific Instruction set	+500
1004/8/16/ 24/32 NCP	No control panel option	-400
	CPU OPTIONS	
1240	Autoload-automatically loads memory from selected input device	565
	MEMORY OPTIONS	
	Can be used in any combination up to 32,768 words of memory	
3310	Random Access Magnetic Core Memory with 4,096 16-bit words	2,000
3312	Same as 3310 except 8,192 words	2,200
	MASS STORAGE	
	DISC	
6755-10	Disc Storage Unit, IBM 5444 compatible	9,630
6755-11	Add-on Disc Storage Unit	6,330
6757	Removable Disc Cartridge	200
	INPUT/OUTPUT	
	Teleprinter	
6710-10	Teletypewriter-ASR model 33, Controller, Cable	2,030
	Paper Tape	
	Includes controller & cable	
6717-10	High Speed Paper Tape Reader w/o spooler	2,155
6718-12	Same as 6717-10 except with spooler	3,255
6719-30	Combination High Speed Paper Tape Reader and Punch	5,015
6723-20	High Speed Paper Tape Punch	3,560
	Printers	
	Include controller, cable	
6762-11	Printer Terminal — 132 column, 64 character set, 100 characters per second rate, without stand	4,275
6762-12	6762-11 with stand	4,585
6765-21	Line Printer — 132 column, 64 character set, 200 LPM	12,145
6768-31	Same as 6765-21 except 600 LPM	15,820
	Card Readers	
	Include controller, cable	
6733-11	Card Reader — 80 column, 600 cards per minute	5,745
6734-10	Same as 6733-11 except 285 cards per minute	3,895
	Interfaces and I/O Controllers	
4501	Parallel I/O Controller	800
4502	Serial I/O Controller	565
4503	Parallel I/O Controller	800
4506	Low true input and high true output	800
4551	Custom Bus Interface	565
4590	Block Transfer Adapter	500
	Data Communications	
	DATA COMMUNICATIONS I/O CONTROLLER OPTIONS	
4651	Async Modem Controller	565
4530	Four Channel Async Line Multiplexor	1,050

HEADQUARTERS

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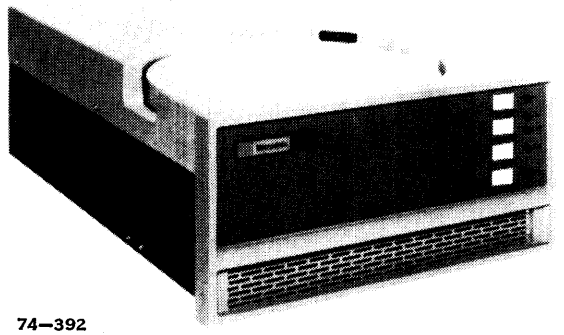

74–392

OVERVIEW

The Microdata Micro 800 and 1600 Series are microprogrammed, stack-processing, byte-oriented systems aimed at general-purpose OEM markets. The two lines differ slightly in speed and packaging; the 800 series has a 1.1-μsec memory cycle time while the 1600 series has a 1-μsec memory cycle. The 1600, moreover, has different firmware to improve performance over and above that obtained from the shorter memory cycle time.

Microdata was microprogramming its systems long before microprogramming was widely implemented. The 800 series was introduced in the spring of 1969 by Micro Systems Incorporated, then a subsidiary of Microdata. Subsequently, as the line developed Micro Systems was totally merged into Microdata Corporation. The 800 line is still in production although it is a "discontinued" product; it has been replaced by the 1600, an optimized version that retains the same architecture, instruction set and peripherals as the 800. Both series, moreover, have submodels that differ mostly by the instruction set implemented in the ROM memory. The Micro 800 series includes the 800, 810, 820, and 821, which implement from 23 to 107 instructions. The 1600 Micro Series includes the 1600, 1600/10, 1600/20, 1600/21, 1600/30, 1600/40, and 1600/60, which implement instruction sets ranging from 23 to 111 instructions. The submodels with the same 2-digit ending, for example, correspond with the 821 and 1600/21, both contain the same instruction set. Model 10 has a few less instructions than Model 20. Model 21 has the same instruction set as the Model 20, but it has been recoded to achieve higher speeds. Model 30 has a few more instructions to handle dual processor configurations. Model 40 has a superset of the Model 20, with extra instructions to handle multiuser "Basic." Model 60 has no instructions available to the user; it is designed as a communications front end in a multiple processor configuration with Model 30, and its control ROM is dedicated to handling communications terminals.

The 821 and 1600/21 are so similar there is no compatibility problem in moving from one system to the other at this level — the same peripherals can attach to either, and all programs in similar operating environments can be run on either system. Similarly, all 800 programs can run on 1600 machines. The only exception might be programs with time-dependent subroutines that run on systems without real-time clocks. The 821-1600/21 instruction set, for example, comprises 107 instructions: 16 control, 12 arithmetic and logical shifts, 17 conditional jumps, 6 I/O, 19 interregister, 8 stack control, 5 character/string manipulation, 2 decimal add/subtract, 2 multiply/divide, and 20 memory reference instructions.

Software for the two series includes an operating system, assembler, Teletype debug facility, text editor, and diagnostics. The operating system is a simple Teletype/paper tape operating system (TOS) that requires high-speed paper tape facilities and a card reader in addition to the CPU, 4K words of memory, and Teletype. The assembler (MAP 810/820) is a 2-pass macro translator that generates absolute code. The BASIC language is also available at extra cost.

PERFORMANCE AND COMPETITIVE POSITION

Until the recent introduction of the 3200 and the Reality™ small business system, Microdata sold its systems almost exclusively OEM. More than 95 percent of the current installations (which now number in excess of 6,000) are OEM. A few universities and colleges also bought Microdata systems as end-user systems. Microdata markets their systems abroad through Intertechnique in France, Tejin Limited in Japan, and Allen Crawford Associates in Canada.

Microdata is vigorously working to expand its installed base, partly because a few customers accounted for a large part of its business and this made the company somewhat vulnerable. In 1973, Microdata reported that 74 percent of its sales went to five customers with one order accounting for 39 percent of total sales.

The 1600 Series has stiff competition from other OEM-oriented manufacturers, some of whom also provide the benefits of microprogramming to OEM customers. General Automation and Computer Automation as well as DEC, Data General, and Hewlett-Packard have big OEM businesses. General Automation and Hewlett-Packard, moreover, provide extensive support for microprogramming for their systems.

Microdata has kept step with its competitors at the low end of the market by introducing the Micro-One bipolar microcomputer, a computer-on-a-board that serves as an entry system to the 800/1600 series. The 3200 Series at the upper end provides another compatible line with higher performance characteristics than the 1600. Thus, the company has an integrated series of product lines with each series upward compatible with the next higher system in the line.

User Reactions

Most Microdata users bought their 800/1600 on an OEM basis and configured them into systems for their own end-users. The users interviewed were acutely aware of the reliability and performance of the Microdata processors; the processor's performance affects the performance of their completed systems and, ultimately, the company's very existence.

All users interviewed expressed pleasure with their Microdata processors. Most users handle their own maintenance; one user has never had a reason to call Microdata. Another user said he dealt more with Microdata engineers than with the field service people. A third user simply returns faulty chips to Microdata, which sends replacements in the mail.

Before selecting the Microdata equipment, users investigated the major minicomputer manufacturers: Digital Equipment, Hewlett-Packard, Varian, Computer Automation, General Automation, Interdata, IBM, and Texas Instruments. One user also looked at Systems Engineering Labs and the Four Phase small business system. Another user considered Intel's microprocessors for the low end of his systems. The reasons for choosing Microdata equipment varied. All users spoke of Microdata's early entry into microprogramming. One user wanted a microprogrammed machine with an instruction set that could be customized and optimized. He required many machines and wanted to be near the vendor. Another user chose Microdata because of the price and the ability to communicate with a CRT and a printer at the hardware and software levels. Another user found the Microdata dual-processor configuration to be the least expensive bid to meet required specifications. One user bought the Microdata 1600 because of its ability to emulate Varisystem's P-16 controller. This emulation afforded continuity for his end-users.

Most users developed their own languages and a few also developed their own operating systems. One user translated his business language into the Microdata assembly language.

Microdata machines are used in many environments. One firm has used the 1600 for two years as a photo unit controller for photocomposition machinery. This user found that service time in the field was reduced by changing from a "repairable" controller to a card controller; replacing the defective card was fast and simple. The user thought highly of the features provided to prevent memory loss. The firm discovered a minor malfunction in the back plane — one chip kept failing. Microdata changed the chip design from thin film to discrete components. The firm is planning to add more core in the near future.

Another user has a 1600 twin-processor configuration which operates as a communication controller for an IBM 360/75; it receives information from terminals in various areas. Most of the operating system is implemented in firmware. The user feels that Microdata has produced a balance of hardware, firmware, and software resulting in a very economical communication controller. In the dual configuration, the first processor communicates with the host computer through channel communications, and the second processor is dedicated to scanning the communication lines.

A turnkey systems house uses 1600 processors as the core of medical laboratory systems to handle medical billing, accounts payable and receivable. This company also sells its systems to small furniture manufacturers. The user has developed a disc operating system, implemented mainly in firmware. The company had some system integration problems, which were not caused by defects in the processor. This user found the 1600/20 instruction set to be "pretty darn good" operating in one-byte precision.

Another systems house uses a customized 1600 as an index table and controller for data storage and retrieval system which are tied on-line to a host computer. It converts key strokes to a location on film to retrieve data. This user found the 1600 to be reliable and the only computer available in the company's price range and compatible with its application.

A user of 1600/21 and 1600/30 processors configures this equipment into turnkey systems for wholesale pharmaceutical and warehouse applications. The firm has developed its own business language and disc operating system for these purposes. The firm had a good experience with Microdata, although Microdata's response to a minor fault in the disc controller was poor. This user assumes the responsibility of maintaining the finished system.

A company that produces small business systems uses the Microdata 1600 for its central processor. Microdata installs the user's custom firmware and tests it through a comparator for bits. This company also tests the equipment with its own diagnostics. This user has experienced fewer problems than expected and is pleased that Microdata delivers equipment on the date specified. This user believes the Microdata equipment has a proven track record and that is important.

CONFIGURATION GUIDE

The 800 and 1600 differ mostly in speed, ROM control memory, packaging (different systems panel) and a few options, but configuration details for both series are nearly identical. Basic configurations consist of a CPU, power supply, bank of 16 registers (6 working registers) control ROM implementing the instructions, priority interrupt system with 8 external interrupts, bootstrap loader, 3 I/O modes (DMA, buffered I/O, programmed I/O) and 8K words of memory. Processor options include a real-time clock, 8-level increments for the interrupt system up to 64 levels, expanded DMA capability, and memory expansion to 32K words. Power-fail detect/auto restart is optional on the 800 and standard on the 1600. The control ROM can be expanded up to 1,024 words in 256-word modules. See Table 1.

Table 1. Micro 800 and 1600: Specifications

CENTRAL PROCESSOR	
No. of General-Purpose Registers	6
Addressing: Indexed	To 32K words
Indirect	± 128 words
Instruction Set (no.)	23-107
Priority Interrupt Levels	8-64
MAIN STORAGE	
Type	Core
Word Length	16 bits
Cycle Time (μsec)	1.1 (800); 1.0 (1600)
Increment Size (words)	4K, 8K
Capacity (min-max) (words)	8K, 32K
Parity	No
Protect	No
ROM	
Use	Microprogram, user macros
Capacity	1,024 words
I/O CHANNELS	
Programmed I/O	Yes
DMA	Yes
Multiplexed I/O	No
OPTIONS	
Real-Time Clock	Yes
Floating-Point Processor	No

Model 1600/30 can be coupled with a 1600/60 in a multiprocessor configuration, but smaller models do not have this capability. Model 1600/40 has extra instructions to handle multiuser "Basic" configurations.

Central Processor

Instructions for all 800 and 1600 machines are microprogrammed. ROM control memory, usually implemented in semiconductor memory, contains the microcommands that define instruction sets. Its operation proceeds at the basic 220-nanosecond clock rate of both series. For all instructions except a JUMP, the next ROM word to be used is preloaded into the processor's control register; this lookahead feature reduces instruction execution times.

The CPU uses separate registers to address control memory and to buffer its output. In addition to implementing the instruction set, control memory can store firmware program constants.

Memory referencing instructions have eight possible addressing modes; namely, direct, direct relative, indirect, indirect relative, indexed, biased indexed, extended, and literal. The basic memory reference instruction is one byte containing two fields: a 5-bit operation code and a 3-bit M field that specifies the address mode. Additional bytes (up to five) contain the operand address, indirect address, base address, or a literal depending upon the addressing mode. Direct addressing can access the first 256 memory locations. Relative addressing can access the 127 locations above or 128 locations below the next instruction in memory.

Indirect address words are located in the first 256 core memory locations. Indexing adds the indirect address word and the index register to produce the effective address. Extended addressing and indexing require a multiple-byte instruction that can address all 32,768 words of storage.

Internal interrupts on the MICRO 800 and 1600 are higher in priority than external interrupts. They have the following priorities from lowest to highest: console-triggered interrupt, direct memory access channel termination, real-time clock, memory protect, memory parity, memory boundary error, power fail, and power on.

Individual interrupts from peripheral subsystems are handled by an external interrupt module, which provides for arming/disarming individual interrupts and enabling/disabling recognition of interrupts in a group. Standard external interrupt cards with eight priority interrupt lines are available. A total of 64 external interrupts can be implemented.

Programmable registers include 16-bit accumulator and extension register, 16-bit index register, 15-bit program counter, 2-bit word-length register, and a 1-bit overflow register.

Table 2 summarizes the characteristics of the different processor models.

Input/Output

Micro 800 and 1600 Series have three input/output facilities: serial Teletype interface, direct memory access (DMA), and a byte input/output bus. The serial Teletype interface can communicate with a full-duplex Teletype; a Parallel Teletype Controller option provides for transfer rates up to 300 characters per second, instead of the standard 10 characters per second. The DMA interface allows direct data transfers between memory and device controllers on an interleaved cycle-stealing basis at transfer rates up to 910,000 (821) or 1,000,000 (1600/21) 8-bit bytes per second.

Table 2. Micro 800 and 1600 Models

Model	Instructions
800	23
810	89
820	95
821	107
1600	23
1600/20	95
1600/21	107
1600/30	111
1600/40	107
1600/60	None*

* None accessible to user; acts as communications front end in multiprocessor configuration with the 1600/30.

The byte input/output facility allows programmed byte-by-byte I/O transfers and buffered block transfers between an external device and memory; maximum transfer rate is 20,000 8-bit bytes per second. All peripherals except Teletype units and discs use the byte I/O bus; discs use the DMA channel and Teletype units use the TTY bus. The byte I/O bus can attach up to 32 devices; the DMA channel can handle 4 standard or 8 optional.

Peripherals

Low-Speed Peripherals. The following peripherals are available.

- Teletype: ASR 33 with paper tape reader and punch, 10 characters per second.
- Paper Tape: Reader/punch reads 300 characters per second and punches 75 characters per second.
- Punched Card Reader: reads 300 cards per minute.
- Line Printers: 80 columns; 150 lines per minute for 80-column lines; 250 lines per minute for 132-column lines.

Mass Storage. Subsystems include both discs and magnetic tape units.

- 2853,4,5,6 Disc Systems (use 8000 Series Drives), 2.5, 5.0, and 10.0 million bytes; one removable or one fixed and one removable platter; single or double density recording; 75-millisecond access time (60-millisecond with fast access feature); transfer rate is 195,000 (312,000 with higher-speed feature) bytes per second over DMA channel.
- Magnetic Tape: up to four transports by way of one controller on byte I/O channel, transports can be selected from the following units: 7-/9-track, 800 bytes per inch, 12.5 inches per second (10,000 bytes per second), 7-/9-track, 800 bytes per inch, 25 inches per second (20,000 bytes per second). All transports on a controller must be the same types.

Communications Devices. A variety of interfaces are provided.

- Full-Duplex Synchronous Modem Interface and Control: (programmed, concurrent I/O and interrupt data transfer modes); rates up to 9,600 baud; EIA Standard RS232C interface.
- Synchronous Modem Interface with Auto Call/Answer Unit: full-duplex in the programmed transfer mode; half-/full-duplex in the concurrent I/O mode; rates up to 9,600 baud; EIA Standard RS232C interface.
- Asynchronous Communications Controller and Interface: programmed, concurrent I/O or interrupt on input character ready transfers at 110 to 9,600 baud rates; EIA Standard RS232C or 20-ma current loop interface to be specified at time of order.
- 4-Channel Communications Interface and Controller: simultaneous operation of 4 full-duplex asynchronous lines; each channel programmable for 75 to 2,400 baud; EIA Standard RS232C or Teletype 20-ma current loop interface.
- Eight-Channel Communications Interface and Controller: simultaneous operations of 8 full-duplex asynchronous lines; 75 to 2,400 baud; EIA Standard RS232C or 20-ma current loop interface.
- Modem/Communications Control: full-duplex 16 discrete inputs; 16 discrete outputs; EIA Standard RS232C interface.
- Automatic Call Unit Controller: controls up to 4 Bell Model 801 Automatic Call Units; EIA Standard RS232C interface.
- Eight-Channel Low-Speed Modem Interface: provides 8 full-duplex RS232B interfaces.
- Sixteen-Channel, Low-Speed Modem Interface: provides 16 full-duplex RS232B interfaces.
- Eight-Channel Teletype Control: provides 8 full-duplex 20-ma Teletype interfaces.
- Sixteen-Channel Teletype Control: provides 16 full-duplex 20-ma Teletype interfaces.

MAINTENANCE

Microdata provides maintenance through 15 plant and service depots and sales offices located in all major cities in the United States.

HEADQUARTERS

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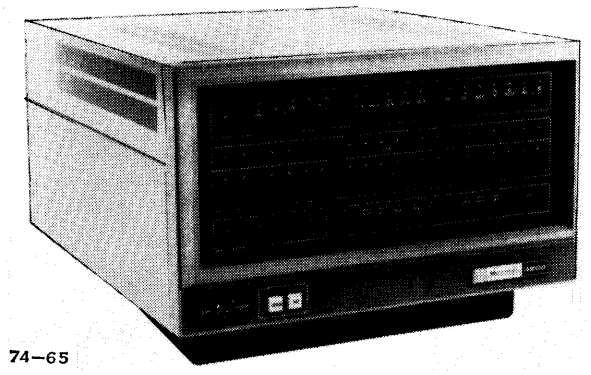
Model Number	Description	Purchase $	Monthly Maint. $
	The Microdata 800 is no longer being actively marketed.		
	PROCESSORS AND WORKING STORAGE		
1600	Basic Processor (with power fail/auto-restart; card cage with 12 assembly slots; integral power supply)	1,850	30
1600/10	Processor (same as 1600 plus 768 words ROM control memory)	2,250	34
1600/13	Processor (same as 1600 plus 768 words ROM control memory)	2,250	40
1600/20	Processor (same as 1600 plus 768 words ROM control memory)	2,250	38
1600/21	Processor (same as 1600 plus 1,024 words ROM control memory)	2,400	40
1600/30	Processor (same as 1600 plus 1,792 words ROM control memory)	2,850	40
1600/40	Processor (same as 1600 plus 1,536 words ROM control memory, with multiterminal control for use with BASIC programming language)	3,350	45
1600-40-1	System computers with 4 additional assembly slots and a 20 amp remote power supply	+200	
1600-40-2	Same as 1600-40-1 except 40 amp remote power supply	+550	
1600D	Dual Microdata 1600 basic CPUs with 40 amp remote power supply, and card cage with 15 available assembly slots	4,400	55
1600/60	Microdata 1600/60 Communications Processor (dual CPUs; 1600/30 general-purpose computer and a communications operating module (COM 60), 40 amp remote power supply, and card cage with 13 available assembly slots)	7,900	90
	Processor Options		
	Real Time Clock (for 1600 or 1600/XX)	400	
	Power Fail/Auto-Restart (for 1600 or 1600/XX)	600	
	Teletype Controller (for 1600 or 1600/XX)	150	
	Magnetic Core Memory		
2216	16,384 byte (8-bit) core memory module; requires 1 computer assembly slot	3,000	25/10
2208	8,192 byte (8-bit) core memory module; requires 1 computer assembly slot	1,800	20/10
	Control Memories		
2310-nnnn	Programmed Read Only Memory (PROM; with customer-supplied firmware; $100 one-time charge for program set up of each 256 words; for 1600 only)		
	256 Words	550	
	512 Words	450	
	768 Words	1,350	
	1,024 Words	1,750	
	1,280 Words	2,150	
	1,536 Words	2,550	
	1,792 Words	2,950	
	2,048 Words	3,350	
2320-nnnn	Bipolar Read Only Memory (BROM; with customer-supplied firmware; $2,000 one-time charge for production set up and semiconductor masks for each 256-word page; for 1600 only)		
	256 Words	300	
	512 Words	450	
	768 Words	600	
	1,024 Words	750	
	1,280 Words	900	
	1,536 Words	1,050	
	1,792 Words	1,200	
	2,048 Words	1,350	
2330-2	Firmware Set/10, 768 BROM for 1600	600	–
2330-3	Firmware Set/13, 768 words semiconductor read only memory for 1600	600	–
2331-3	Firmware Set/20, 768 words BROM for 1600	600	–
2331-4	Firmware Set/21, 1,024 words BROM for 1600	750	–
2332-1	Firmware Set/30, 1,792 words BROM for 1600 & 1600D	1,200	–
2333-1	Firmware Set/40, 1,536 words BROM. Provides multiterminal control for use with BASIC programming language, for 1600	1,700	–
2334-1	Firmware, COM-60. Requires 1600D	1,000	–
2335-1	Firmware, floating point, option for 1600/30	950	–
2335-2	Firmware, floating point, option for 1600/21	950	–
2380-512	Alterable Control Memory (ACM) 512 words. Requires 1 computer assembly slot for 2384	1,800	20
2380-1024	Alterable Control Memory (ACM) 1,024 words, for 2384	2,500	25
2310-4	Diagnostic firmware for 2310-4	1,750	–
2384	ACM control panel, cooling unit, and 20 amp remote power supply for up to two 2380 ACM modules	1,000	10
2384-1	ACM control panel, cooling unit, and 40 amp remote power supply for up to four 2380 ACM modules	1,350	13
	Control Panels		
2101	Basic panel (run-halt indicators, 4 sense switches, 6 control switches, and keylock power switch)	300	
2101-2	System panel (same as 2101 but with register display and 16-bit switch register)	600	
2102-3	System panel for 1600D CPU (same as 2102-2)	600	
	MASS STORAGE		
	Disc system (top loading, moving-head disc drive with 1 removable cartridge, (200K bytes/sec transfer rate; 35msec avg random access; DMA mpx channel; controller; slide mounts with cable retractor; cables; requires 2 computer assembly slots)		
2854	100 tpi; 5M bytes; 1,500 rpm	8,625	100
2854-1	100 tpi; 5M bytes; 2,400 rpm	8,625	100
2854-2	100 tpi; 5M bytes; 1,500 rpm	8,625	100
2854-3	100 tpi; 5M bytes; 2,400 rpm	8,625	100
2856	**MASS STORAGE (Cont'd)** 200 tpi; 10M bytes; 1,500 rpm	9,325	100
2856-1	200 tpi; 10M bytes; 2,400 rpm	9,325	100
2856-2	200 tpi; 10M bytes; 1,500 rpm	9,325	100
2856-3	200 tpi; 10M bytes; 2,400 rpm	9,325	100
	Series 8000 add-on disc drive (includes removable cartridge, slide mounts with cable retractor, daisychain cable assembly and terminator board)		
2861	100 tpi; 5M bytes; 1,500 rpm	5,025	60
2861-1	100 tpi; 5M bytes; 2,400 rpm	5,025	60
2863	200 tpi; 10M bytes; 1,500 rpm	5,725	75
2863-1	200 tpi; 10M bytes; 2,400 rpm	5,725	75
2950	Disc system controller for up to 4 disc drive units (operates with 2515 DMA/multiplexor, accommodates 100 tpi and 200 tpi drives)	3,300	30
	INPUT/OUTPUT		
	Paper Tape		
2710	Paper tape system (300 cps, fanfold, 8-channel paper tape reader; 75 cps, fanfold 8-channel paper tape punch, cables; and I/O controller; rack mountable 10.5 in. high; requires 1 computer assembly slot)	3,955	60
2711	Paper tape reader system (300 cps fanfold, 8-channel paper tape reader including I/O controller and cable set; requires 1 computer assembly slot)	2,500	30
2712	Paper tape punch system (75 cps, fanfold, 8-channel paper tape punch including I/O controller and cable set; requires 1 computer assembly slot; spooler $250 extra)	2,800	30
	Card Readers		
2720	Card reader, cable and input controller (300 cpm, 80-col cards, 1,000-card hopper, 1,000-card stacker, requires 1 computer assembly slot)	3,750	50
2720-1	Mark sense card reader (cable; controller; 300 cpm; 1,000-card hopper; 1,000-card stacker, reads mark sense cards or std punched cards)	5,250	60
2920	Card reader controller (includes cable assembly; requires 1 computer assembly slot)	900	10
	Line Printers		
2731	Line printer (80-col, 64-char, 356 lpm; cables and output controller; requires 1 computer assembly slot)	9,750	150
2732	Line printer (132-col, 64 char, 245 lpm; 12-channel VFU; cables and output controller; requires 1 computer assembly slot)	12,500	200
	Line Printer Options		
	Self Test Feature	285	NC
	Parity Check	285	NC
	Static Eliminator	390	NC
2733	Line printer (132-col, 64-char, 300 lpm, cables and controller)	9,500	150
2734	Line printer (132-col, 96-char, 200 lpm; cables and controller)	10,500	150
2733-1	12-channel vertical format unit (VFU)	400	NC
2736	Line printer (165 cps, 60 lpm, 132-col, 64 char, cable assembly, RS232C interface)	6,500	100
	MAGNETIC TAPE		
	Magnetic tape system (one 9-track, 800 bpi, mag tape transport with a read/write dual gap head, controller (2930) and cables; data transfers via the concurrent I/O mode; requires 2 computer assembly slots)		
2812	8.5-in. reel; 12.5 ips; 10K bytes/sec	5,750	75
2813	8.5-in. reel; 25.0 ips; 20K bytes/sec	5,900	75
2814	10.5-in. reel; 12.5 ips; 10K bytes/sec	6,000	75
2815	10.5-in. reel; 25.0 ips; 20K bytes/sec	6,100	75
	Add-on mag tape drive (9-track, 800 bpi, NRZI tape transport)		
2822-x	8.5-in. reel; 12.5 ips; 10K bytes/sec	3,850	48
2823-x	8.5-in. reel; 25 ips; 20K bytes/sec	3,850	48
2824-x	10.5-in. reel; 12.5 ips; 10K bytes/sec	4,100	50
2825-x	10.5-in. reel; 25 ips; 20K bytes/sec	4,100	50
2930	Magnetic tape controller (for up to 4 mag tape units, 12.5 ips, 800 bpi, 7- or 9-track includes cable assembly, requires 2 computer assembly slots)	2,000	15
2930-1	Magnetic tape controller (for up to 4 mag tape units, includes cable assembly, 25 ips, 800 bpi, 7- or 9-track)	2,000	15
2930-2	Magnetic tape controller (for up to 4 mag tape units, 12.5 ips, 800 bpi, 7- or 9-track without cable assembly)	1,775	12
2930-3	Magnetic tape controller (for up to 4 mag tape units, 25 ips, 800 bpi, 7- or 9-track without cable assembly)	1,775	12
	Terminals		
2910	IBM Selectric Typewriter Controller (24-volt operation includes power supply and cable assembly)	1,550	16
2750	CRT and kybd (split-screen operation with foreground/background intensity control; full-editing; 1,920 displayable char; 27 lines of 80 char each; switch selectable baud rates from 110 to 2,400; power supply and cable set)	3,120	25
	General-Purpose and Utility Interfaces		
2500	General-purpose I/O wire wrap board (accommodates up to 135 units of 14 or 16 pin IC sockets and 10 units of 24 pin IC sockets)	150	
2501	General-purpose I/O wire-wrap board (including 72 each 16 pin sockets, 6 each 24 pin sockets, and 4 each 40 pin sockets)	450	
2510	Byte I/O controller	800	10
2511	Full word I/O interface (provides 32 input lines and 32 output lines)	700	10

Note: tpi – tracks per inch

Model Number	Description	Purchase $	Monthly Maint. $
	General-Purpose and Utility Interfaces (Cont'd)		
2514	Selector channel operates via DMA (accommodates up to 4 I/O devices)	850	10
2515	Multiplexor channel operates via DMA (provides for simultaneous operation of up to 4 I/O devices)	300	10
	DATA COMMUNICATIONS		
	Communications Interfaces		
2600	FDX sync modem interface and control (operates in programmed, concurrent I/O and interrupt data transfer modes; accommodates std rates up to 9,600 baud, EIA Standard RS232C; requires 2 computer assembly slot)	900	10
2610	Async communications controller (for 103 and 202 data sets or Teletype 20 ma current loop; single channel, FDX programmable rates 75 to 9,600 baud char lengths, stop bits, and parity error checking; EIA Standard RS232C; requires 1 computer assembly slot)	500	10
2612	Async communications controller (provides simultaneous operation of 8 FDX async channels; switch or jumper selectable rates 75 to 9,600 baud; 1 of 4 char lengths, 1 or 2 stop bits, and parity checking; EIA Standard RS232C or Teletype 20 ma current loop; requires 1 computer assembly slot)	1,600	16
2612-1	Async communications controller (same as 2612 except 4 FDX channels)	1,000	10
2613	Async modem interface (provides simultaneous operation of 8 FDX async channels for 103 and 202-type data sets; programmable rates 75 to 9,600 baud; char lengths, stop bits, and parity error checking; requires 1 computer assembly slot)	2,000	20
2613-1	Async modem interface (same as 2613 except 4 FDX channels)	1,400	14
2614	Async communications controller (provides simultaneous operation of 8 FDX async channels; switch or jumper selectable rates 75 to 9,600 baud, 1 of 4 char lengths, 1 or 2 stop bits, and parity checking; EIA Standard RS232C or Teletype 20 ma current loop; requires 1 computer assembly slot)	1,600	16
2614-1	Same as 2614 except 4 FDX channels	1,000	10
	ACCESSORIES		
	Enclosures and Cabinets		
2001	Standard 19-in. rack mountable enclosure for cabinets 24 in. to 30 in. in depth (has single fan for use with integral power supply; second fan $50 extra)	170	
2002	Table top enclosure (with single fan for use with integral power supply; second fan $50 extra)	250	
2003	Standard 19-in. rack mounting hardware for nonenclosed card cage in cabinets 24 in. to 30 in. in depth	50	
2008	Cooling Unit for standard 19-in. rack mounting with 4 fans; unit includes 5-¼-in. front panel	280	
2006	Single bay computer cabinet (49-in. vertical mounting space, 19-in. wide, and 30 in. deep; ¾ length rear door; 30-amp receptacle; and 20-amp circuit breaker; power bus strip, removable side panels; operator's work surface; both casters and leveling legs; floor or roof mounted 600 cfm blower; second 20-amp circuit breaker and power bus strip $650)	950	
	CHASSIS		
	I/O Expansion Chassis		
2410	Expansion chassis for standard Microdata 1600 computers	1,550	16
2411	Expansion chassis for dual processor system requiring 2 I/O bus extensions	1,850	19
	POWER SUPPLIES		
1112	Power supply – internal (standard plug-in 20 amp power supply, UL listed)	675	
1112-1	Power supply – external (remote 20-amp power supply, UL listed)	875	
0800	Power supply – external (remote 40-amp power supply)	1,225	

MICRODATA CORP.

3200 Series System Report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OVERVIEW

The Microdata 3200 is a 16-bit microprogrammable minicomputer aimed at both OEM and end-user markets. It consists of the microprogrammable 3200, 32/S, 32/S1, and the 32/S with MPL.

The 3200 is the bare hardware without a microprogram instruction set; no assembly-language level instruction set has been implemented. The 32/S is a complete computer with its architecture designed to make implementation of a compiler language easy. It is designed around a push down stack and a Monobus. The 32/S1 has an extended instruction set; floating-point doubleword arithmetic; string manipulation instructions and swapword in stack instruction set.

Programs are coded in MPL (Microdata Programming Language). MPL is a block-oriented, high-level language similar to PL/1. Currently, programs are cross compiled on an IBM System/360 with PL/1 compiler. A self-compiler implemented in firmware is scheduled for delivery in the first quarter of 1975.

The 3200 hardware modules are organized around a single fast "monobus" connecting all system components. The processor, memory, and peripheral devices operate as monobus subsystems that communicate with each other in a master-slave relationship. This type of bus-centered architecture permits connecting memory modules of different speeds to a system. In addition, the various memory modules and peripheral control cards can be attached in any order to monobus slots. Once initiated, data transfers between high-speed devices and memory can continue while the processor does other work. This architecture is similar to that of the GRI-99 and Digital PDP-11. The 3200 Series addresses peripheral devices as though they were memory locations; thus it has no separate set of I/O instructions.

Main memory can consist of 4K to 128K 16-bit words of MOS memory. The microprocessor utilizes 512 to 4,096 32-bit words of control memory, which can be read-only or a combination of read-only and read/write. Main memory cycle time is 450 nanoseconds for full read cycle; 350 nanoseconds for full write cycle; control memory cycle time is 135 nanoseconds. A high-speed hardware push-down stack, coupled with a look-ahead feature that queues the next software instruction in advance, acts like a cache memory to speed up processor throughput. Addressing is to the byte or word level.

The 32/S is a completely new system; it is not compatible with any system previously offered by Microdata. At present only the MPL cross compiler for the IBM 360, the 32/S self-compiler, and a rudimentary operating system called GENASYS are available.

Peripherals for all models of the 3200 Series are the same as those for Microdata's 800 and 1600 line.

The first 3200 Series system was delivered in January 1974, about 20 have been delivered to date, and over 40 are on order.

Table 1 contains a summary of the mainframe characteristics.

COMPETITIVE ANALYSIS

The 3200 joins a growing number of minicomputers featuring microprogramming that can be extended by the user. The versatility of microprogrammed systems, as compared with earlier systems which implement assembly/machine language level instructions with "hardwired" logic, has led some industry observers to label microprogrammed systems "the fourth generation." Microdata has already had considerable experience with this type of system. Systems in the 800 and 1600 Series are all microprogrammed.

The 3200 Series combines high-speed, MOS semiconductor technology and a push-pop data stack with the inherent advantages of microprogramming. The stack-oriented Model 32/S, with its MPL language, is the first

HEADQUARTERS

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Table 1. Microdata 32/S: Mainframe Characteristics

CENTRAL PROCESSOR	
Type	Microprogrammed
Control Memory	ROM
Size of Memory	512-4,096 32-bit words
No. of Internal Registers	5 (hardware); 32K (memory)
Addressing	
Direct (no. of words)	128K
Indirect	Yes
Indexed	Yes
Instruction Set	
Implementation	Firmware
Number	151
Decimal Arithmetic	Yes
Floating-Pt Arithmetic	Opt
User Microprogramming	Yes
Priority Interrupt Levels	10 int; 8-64 ext
MAIN MEMORY	
Type	MOS
Cycle Time (μsec)	0.35
Basic Addressable Unit	16-bit word
Bytes per Access	2
Min Capacity (bytes)	8K
Max Capacity (bytes)	256K
Increment Size (bytes)	8K
Ports per Module	1 (monobus)
Error Checks	Parity, 1 bit/byte
Protection Method	Opt
Memory Management	Firmware
ROM	Yes
Use	Firmware
Capacity	512-4,096 32-bit words
I/O CHANNELS	
Programmed I/O	Std
DMA Channels	Std
Multiplexed I/O (subchannels)	Opt
Max Transfer Rate (wds/sec)	
With Memory	2.5M
Over DMA	3.0M
Simultaneous Operations	Yes

model to implement some of the special advantages of this unique combination of characteristics. The resulting system should be of interest to end users who want to do their own programming, particularly when Microdata develops more supporting software.

Currently, a cross microassembler called "CAP 32" and written in PL-1, Level F and a cross MPL compiler for execution on IBM System/360 running under OS are available. An MPL self compiler is scheduled for the first quarter, 1975.

While the Model 3200 is of greatest interest to the OEM market, Microdata is marketing to end users as well. One of the first 3200s was bought by an end user, who attached it to a PDP-11 for high-speed repetitive calculations. Another is being used to control a high-speed printing operation. Microdata anticipates that most early users of the system will come from the University market.

Microdata has over 6,000 computers currently in operation, and most have been sold to OEMs. Microdata is working to attract more end users to its customer base. In the past, a large majority of Microdata sales were to five customers, with one order accounting for over a third of total sales. To lessen the market vulnerability inherent in dependence on large accounts, Microdata hopes to extend its customer base so that no customer will account for more than 15 percent of sales.

Microdata also markets Reality, a small business system based on the 1600. For large companies, Microdata markets through its own staff while distributors handle sales to small end-user companies.

At the low end of the market, Microdata has the Micro-One microprocessor. It includes two total systems: a smart CRT terminal and an 8-channel programmable communications controller.

COMPATIBILITY

The 3200 and 32/S are not compatible with any other computer system in the Microdata line.

CONFIGURATION GUIDE

The basic 3200 system encompasses the CPU, main memories, and I/O controllers attached to a common asynchronous bus (the monobus). Units are mounted on printed circuit boards, three of which are used by the CPU control processor. Additional control memory boards are available. Main memory with power fail protect is supplied in 4K- or 8K-word modules to a 128K-word maximum. Four CPUs can operate on the same bus without overloading. MPL supports multiprogramming; moreover, all hardware is provided for communication between CPUs on a "handshaking" basis. Either a maintenance or an operator's console is included with the system. A battery option is available to maintain memory in case of power fluctuation.

The 32/S includes all the basic 3200 components plus the control memory to implement its architecture and instruction set. Maximum main memory within the CPU chassis is 128K words. System memory protect is an optional feature. An external real-time clock with a variable interval is standard.

Both rack and desktop chassis are available for the 3200. Front panel, power supply, cooling fans, and 16 card slots are included. The card slots are allocated as follows: one for the front panel, three for the processor (including control memory), one for the power supply, and one for each 8K-word main memory module or I/O controller. An expansion chassis for main memory modules and/or I/O controllers is optional. The power supply is integral and can maintain data during power irregularities. A battery pack is available for longer protection.

MAINTENANCE AND SUPPORT

Microdata has service and parts centers in major cities throughout the United States. Monthly maintenance contracts are available for all equipment marketed.

Maintenance for the 3200 Series is relatively simple. Any board can be plugged into any connector in the backplane. If a board needs service, it can be plugged directly into the first available connector. No extender boards are needed. Table 2 lists the peripheral devices that can be used with the system. Table 3 lists the available system software.

Table 2. Microdata 3200 Series: Peripherals

Model	Description
Discs	
3954	Cartridge, master, 1 fixed, 1 removable; 5M-byte capacity; access time: 35 msec; 1500 rpm
3961	Slave unit to 3954
3956	Same as 3964 but double capacity
3963	Slave unit to 3956
Magnetic Tape	
3815	9-trk, 800 bpi; master, NRZI; 25 ips
3835	9-track; 1,600 bpi, PE
3845	Slave units for 3835
Paper Tape	
3710	Reader/punch; 300-cps read/75 cps punch, Fanfold
3710-1	Same as 3710 but roller
Card Reader	
3721	200-cpm read, 20-col cards
Line Printers	
3733	132-col, 64 char, 300 lpm
3734	132-col, 96 char, 200 lpm
3737	132-col, 64 char, 60 lpm (165 cps)
Displays	
3751	CRT, 1920 char; 27 x 80 screen, 110-9,600 baud
Controllers	
1311	General-purpose I/O, 126 14 or 16 IC sockets
1314	Multipurpose I/O, 75-9,600 baud
1330	Async comm; full-/half-duplex, 75-9,600 baud
Terminals Supported	33 ASR, 33 KSR, 35 KSR, TTY, RS232C
Consoles	
Maintenance	18 pairs, register display, manual interrupt, program load
Basic	Load and interrupt buttons

Table 3. Microdata 3200 Series: Software

Package	Description
Microdata Programming Language (MPL)	A PL/1 type language used instead of assembly language
GENASYS/D	A simple, disc-based operating system that allows user program storage on disc
Cross Assembler	For IBM System/360 with PL/1, F level compiler

TYPICAL PRICES

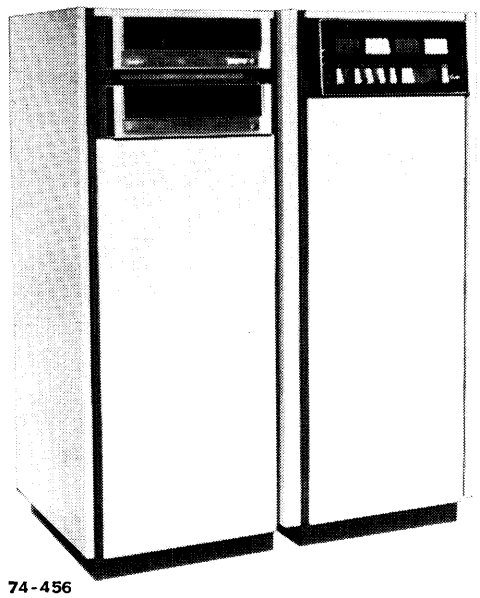
Model Number	Description	Purchase Price $
	SYSTEMS	
3251	32/S General Purpose System (Includes 3250-5 CPU, 16K-word memory with memory, 3015 programmer's console, single-bay cabinet, rack-mounting hardware, 3751 CRT system, 3815 magnetic tape system)	30,650
3252	32/S General Purpose System (same as 3251 except 3250-2 CPU, 32K-word memory, and 3954 disc system)	49,250
3252-1	32/S General Purpose System (same as 3252 except with double bay cabinet)	49,900
	CENTRAL PROCESSORS AND WORKING STORAGE	
3200-5	Microdata 3200 General Purpose Microprogrammable Computer (accommodates up to 2K 32-bit words of control memory, requires 3010 basic panel or 3015 system programmer's console)	6,300
3290-5	Microdata 3290 General Purpose Microprogrammable Computer (Same as 3200-5 except with 512-word control memory for firmware load, accommodates up to 1,536 more words of control memory)	6,750
3250-5	Microdata 32/S Stack-Architecture Microprogrammable Computer (with 2K 32-bit words of control memory; card cage with 12 available assembly slots)	8,050
3200	3200 Card Cage	5,800
1300	Main Memory Microdata MOS Memory Module	
1300-5	8K x 18 Bits, Parity	4,310
1300-6	4K x 18 Bits, Parity	2,930
	Control Memory Assemble (Requires 1 assembly slot)	
1313-X	Accommodates up to 4,096 words of Programmed Read-Only Memory (includes 16 memory)	
	512 Words	700
	1,024 Words	715
	1,536 Words	730
	2,048 Words	745
	4,096 Words	805
3000-XX	ROM with Customer-Supplied Firmware (2)	
	PROM:	
	512 Words	600
	1,024 Words	1,200
	2,048 Words	2,400
	4,096 Words	4,800
	BROM:	
	512 Words	300
	1,024 Words	600
	2,048 Words	1,200
	4,096 Words	2,400
1353	Writable Control Memory (WCM) (512 words, 32 bits)	3,000
3954	Disc System (including 100 tpi, 1,500 rpm; 5M bytes of storage)	10,000
3961	Add-On Disc Drive	7,250
3956	Disc System (200 tpi, 1,500 rpm; 10M bytes of storage)	11,000
3963	Add-On Disc Drive (includes fixed disc and removable cartridge)	7,700
3710 and 3710-1	Paper Tape System (consists of 300-cps reader, 75-cps punch)	4,630
3711	Paper Tape Reader System (300-cps reader)	2,500
3721-1	Card Reader (80-col, 200 cpm)	4,200
3733	Line Printer (132 col, 300 lpm)	10,500
3734	Line Printer (132 col, 96 char set, 200 lpm)	12,000
3733-1	12-Channel Vertical Format (VFU)	500
3737	Line Printer (165 cps, 132 cols)	5,800
	Magnetic Tape System (includes one 9-track tape) Speed, 25 ips	
3815	800 bpi	7,500
3835	1600	8,700
	Add-On Magnetic Tape Drive (9-track)	
3845-X	25 ips, 1600	4,700
	Terminals	
3751	CRT Alphanumeric Display and Keyboard	3,850
	Multipurpose I/O Interface (MPIO)	
	DATA COMMUNICATIONS	
1330-1	Asynchronous Communications Controller	1,100

Notes:

(1) Maintenance contracts on yearly or per-call basis. Cost calculated on per-diem basis for time, materials and travel.
(2) One-time charge for production set-up of each 512-word page.

MODULAR COMPUTER SYSTEMS

MODCOMP I, II and IV



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OVERVIEW

The MODCOMP computers are a family of highly modular, microprogrammed 16-bit-word machines with an assortment of RAM, ROM, and core memories that have an 0.8- or 1.0-microsecond cycle time per word. Three basic computers are offered: MODCOMP I, II, and IV, each capable of extensive expansion.

A variety of model numbers have been assigned to configurations that include various subsets of the available features and system options: I/5 and I/15; II/5, II/10, II/20, II/25, II/25 MCP, II/45, and II/45 MCP; IV/5, and IV/25. The II is also available in two system configurations, II/200 and II/220, that support the MAX III operating system. Modular has also developed a 32K-word core memory module that is mounted on one board; six new MODCOMP II computer models have been developed around the new board: II/12, II/26, II/26CP, II/201, II/221, and II/231. All models can be upgraded to higher models by adding options, except that 0.8-microsecond systems cannot use the new 1.0-microsecond 32K-word memory boards. The model package is less expensive than a lower model system that has been expanded in the field.

MODCOMP computers serve in widely varied applications. MODCOMP I was specifically designed as a small dedicated controller for real-time measurement and control functions. It can also operate as a stand-alone processor with a full complement of peripheral devices. The MODCOMP II is a general-purpose computer for measurement, control, communications (MCP models), and information processing.

The MODCOMP IV, which is upward compatible with the I and II, is a dual-word processor with a memory capacity of 262,190 16-bit words (512K bytes). Because of its dual-word orientation, MODCOMP IV can compete with 32-bit machines for many applications. The first MODCOMP IV was delivered in September 1974.

Modular Computer Systems offers a broad range of software for its computers. Packages available for MODCOMP I includes MAX I Executive, four assemblers, relocatable and link loaders, link editor, utilities, diagnostics, and communication line and remote data acquisition handlers.

MODCOMP II software includes three versions of the MAX III real-time operating system, as well as MAXCOM, MAXNET, Real-Time FORTRAN IV, three assemblers, BASIC, and Real-Time BASIC. Utility processors include a debug executive, source update, source maintenance control, library update, link editor, cataloger, and direct access maintenance processor. MAXNET is a newly announced operating system designed for distributed processing, while MAXCOM is a communications run-time system with low overhead.

MODCOMP IV software includes all the software for Models I and II, plus the MAX IV Real-Time Multiprogramming System (designed specifically for MODCOMP IV), extended BASIC, and RPG II. Machine support software incorporates a file management system, a sort/merge package, and a media-to-media conversion package. Several bisynchronous communication dialects, as well as a remote job entry capability, are available. Table 1 lists the mainframe characteristics.

The MODCOMP II was first announced in 1970 followed by the I in 1971, the II in 1972, and the IV in 1973. The III is no longer actively marketed.

PERFORMANCE AND COMPETITIVE POSITION

MODCOMP has an enviable record; it has doubled its sales each year since its founding in 1970 (a period noted for uncertain economy), and the company has consistently been ahead of sales forecasts. To date, Modular has delivered over 1,000 systems, the typical system currently shipped includes 48K words of core memory. Modular has been a quiet competitor that has never participated in the raucous fighting for the low end of the minicomputer market.

From 50 to 60 percent of new orders are from Modular customers. The company tries to stay out of markets where low price is the main criterion for an order. Instead, it seeks markets where no other company can do what Modular does.

However, as minicomputer manufacturers look for new markets to sustain their phenomenal growth rates, Modular Computer Systems, with its gross sales of $25,000,000 this year, will not be able to hide. When the company branches out into territories already served by Data General, Digital Equipment, and Hewlett-Packard,

Table 1. MODCOMP I, II, and IV: Mainframe Characteristics

MODEL			
CENTRAL PROCESSOR			
Type	Microprogrammed	Microprogrammed	Microprogrammed
Control ROM	Yes	Yes	Yes
No. of Internal Registers	3	16	Up to 16 sets of 16
Addressing			
Direct (no. of wds)	256	256	256
Indirect (no. of wds)	32K	64K	64K
Indexed	Yes	Yes	Yes
Instruction Set			
Implementation	81	106	242
Number (std, opt)	81	106-176	242
Floating Point	No	Opt	Opt
User-Microprogramming	No	Opt	Opt
Priority Interrupt			
Levels	2; 2*	4; 6*	8; 16*
Sublevels	16	64	64
MAIN STORAGE			
Types	Core; solid state	Core	Core
Cycle Times (μsec)	0.8	0.8 or 1.0	0.64
Basic Addressable Unit	Byte; word	Byte; word	Byte; word
Bytes/Access	2	2	2
Cache Memory	No	No	No
Capacity (min/max bytes)	4K-64K	8K-128K*	8K-512K*
Increment Size (bytes)		8K; 16K; 32K; 64K	
Ports/Module	1	1 std; 4 opt	1; 2; 4
Protection	—	Opt*	Opt*
Memory Management	No	No	Opt*
Error Checks	—	Parity option	—
ROM	1K; protect	No	No
INPUT/OUTPUT			
I/O Channels			
Programmed I/O	Std	Std	Std
DMA	Opt	Opt	Opt
Multiplexed	Opt	Opt (8-channel)	Opt (2-channel)
Max Transfer (wd/sec)			
Within Memory	135; 270	135; 270	769; 231
Over DMA	—	1,250,000	1,562,500
Over DMP	300K	300K	300K

*Depends on submodel or option.

the competition will be rougher. All the major manufacturers are going after the markets for substantial minicomputer systems: Digital with its PDP-11/40, 11/45, and 11/50; Data General with its ECLIPSE; and Hewlett-Packard with its 21MX and 3000. Other competitors are General Automation SPC-16, Interdata 7/16 and 7/32, Microdata 3200, Xerox 530, and CDC System 17.

The manufacturers of all these systems recognize that real-time, on-line applications and network processing fit the traditional minicomputer environment better than the batch environment exploited so long by the large mainframe manufacturers. The real-time operating systems with foreground/background processing were developed for real-time control applications, test and measurement, and data acquisition. The demands made by these real-time applications for on-line program development, backup to avoid downtime, fast response times, and program protection are the same ones now required for real-time, on-line commercial processing.

All the minicomputer manufacturers are scrambling to get a firm place in the market before the large mainframes can become on-line transaction oriented. Furthermore, the large mainframe manufacturers not only expect larger markups on their system prices than minicomputer manufacturers; they cannot yet compete on a price/performance basis with minicomputers.

Modular's spectacular success proves the validity of its goals. Its system and software orientation has worked. Still, the pressure on the low end of the minicomputer market from microprocessors and the saturation of the market to sophisticated end users have forced all serious minicomputer manufacturers to become system- and software-oriented. Thus, Modular will have to try harder if it is to continue its winning ways as an unquiet competitor.

MODCOMP IV's double-precision instruction set appears to make the system considerably faster than the PDP-11/40 and ECLIPSE for fixed-point double-precision arithmetic. The IV's floating-point hardware, on the other hand, is no faster than the floating-point hardware for the PDP-11/40 and is slower than the new unit for Data General's ECLIPSE. The main area where the IV appears to be at a competitive advantage over these other two systems is in its I/O channel arrangement and multiple ports to memory. Since MODCOMP IV can have up to four memory ports per module, the effective I/O transfer rate can be 3.75 million words per second without degrading processor throughput.

Because of its low price, systems built around MODCOMP's new memory board cost 18 to 27 percent less than comparable configurations using 16K-word boards. The 32K-word module is also substantially more reliable than two 16K-word modules; it has less components and less interconnectors to fail. The MTBF is expected to be 60,000 hours. Currently, the new memory module is available for MODCOMP II only; it will be available for the IV later.

Modular sees Hewlett-Packard as its strongest communications competitor. The Hewlett-Packard 9700 Distributed Processing System is most similar to MAXNET III. Data General's ECLIPSE system also has well-developed software and hardware facilities for distributed processing systems.

USER REACTIONS

Users interviewed included two OEMs as well as six end users. All customers except one end user are extremely satisfied with their systems and would buy more MODCOMP computers. The one user who had trouble with his system reported less than 10 percent downtime. His system has equipment built especially for the application; it had a few faulty chips, an I/C that was too fast for the application, and a fluke in a multiplexor design which caused trouble during test but not in normal operation. This user, however, is buying three more systems.

Other users feel the architecture is good, the hardware reliable, and the software powerful. One user who is not computer oriented mentioned that MODCOMP FORTRAN allows him to program the system interface to his process control hardware. Most users, including the two OEMs, consider MAX III an excellent base operating system. One OEM who uses the II/25 adds an uninterruptible power supply that keeps current within two percent of ideal; the systems have been installed for several months with no failures.

Several users mentioned that it is easy to interface nonstandard devices to the MODCOMP computers. One user selected a MODCOMP computer because an adapter to interface it to a CDC 6000 system is a standard product. This company has a MODCOMP III, another III on order, and a MODCOMP I. It plans to add 30 or more MODCOMP computers in the future.

Our interviews indicate that Modular Computer Systems maintains a good relationship with its users. Most either expressed an intent to buy more MODCOMP computers or said they would buy another MODCOMP system when needed.

CONFIGURATION GUIDE
SYSTEM DESIGN

MODCOMP I is available in two models: the bare-bones I/5 and the I/15 for larger configurations. Model I/5 can be field upgraded to a I/15. The I/15 includes the arithmetic unit, general register file (three registers), modular bus control interface, priority interrupt system with two levels (16 sublevels each), basic control panel, memory expansion to 32,768 words, power supplies and an 8¾-inch rack-mountable enclosure.

The I/15 incorporates the following features in addition to the I/5 features: an option plane with power for two optional features (multiply/divide, custom macro instructions, direct memory processor, Teletype and paper tape reader controller, and asynchronous data modem interface); hardware fill; real-time clock; Teletype controller; I/O connector assembly; and mounting slides.

Memory for either the I/5 or I/15 system can consist of up to 32K words, composed of core, solid-state RAM, solid-state ROM modules, or a combination of all three types. Core is available in modules of 2K, 4K, 8K, and 16K words. RAM is available in 2K-word modules only. ROM is available in 512-word modules only. Memory parity of the bit per byte is optional. Cycle time for all memory is 0.8 microsecond per word.

A power failsafe and auto-start feature is optionally available for either system. With the direct memory processor for automatic block transfers, the system can handle up to eight peripheral devices concurrently for an aggregate maximum transfer rate of 300K words per second.

Peripherals include a variety of high-speed, low-speed, process I/O, and communications attachments as listed in Table 2. Table 3 lists the hardware configurations required by the major software packages.

MODCOMP II is available in 15 versions, which can be roughly grouped into minimum, MAX II, MAX III, and communications configurations. Nine models use 0.8-microsecond memory modules like those on the MODCOMP I, and six models use the new 1.0-microsecond 32K-word boards. Each model represents a different configuration package, which is priced lower than a bare-bones system with all options added in the field. Table 4 shows the components of each submodel.

A minimum configuration (II/5) includes an arithmetic unit, a read-only control memory, a general register file (15 registers), register I/O and three interrupts (two I/O and unimplemented instruction trap), hardware fill, an operator console, memory expansion to 32K words, power supplies, and an 8¾-inch rack-mountable enclosure.

Four external priority interrupts are options with all models. All features are standard for a model, except maximum memory capacity and different speed memory modules, which are optionally available for the other systems. All peripherals available for MODCOMP I can be used on the II.

Table 2. MODCOMP I, II, and IV: Peripherals

DEVICE MODEL	DESCRIPTION
Discs	
4102-4103	Fixed-head discs; 128K-, 256K-, 512K-wd capacities
4106	Fixed-head discs; 1M capacity
4108	Fixed-head discs; 384K-wd capacity
4126/4127	1M-wd moving-head discs; 97.8K wds/sec transfer
4128/4129	2M-wd moving-head discs; 97.8K wds/sec transfer
4132/4133	12M-wd moving-head discs; 156K wds/sec transfer
4134/4135	26M-wd moving-head discs; 156K wds/sec transfer
Magnetic Tape	
4148/4151	9-trk; 800 bpi, 45 ips
4149/4152	7-trk; 556/800 bpi, 45 ips
4155	9-trk; 1,600 bpi, 45 ips
4160/4162	9-trk/7-; 12.5 ips
Keyboard Printers	
4233-4235	ASR 33; KSR 35; ASR 35 respectively; local
4223-4225	ASR 33; KSR 35; ASR 35 respectively; remote
Paper Tape	
4511/4513	625-cps readers
4512	625-cps reader and 110-cps punch
Cards	
4411/4412	300/1,000-cpm readers
4421	100-cpm punch
Printers	
4211/4214	600/300 lpm; 132-col
4213	50-150 lpm; 132-col
Process I/O	
1200/1500	High-level analog input subsystem; single-ended/differential input
1300	Wide-range analog input subsystem, to 512-channel bipolar signal
1400	Wide-range relay analog input subsystem, to 512-channel bipolar system
1500	Modular data acquisition subsystem; 7 I/O modules
1199	Modular I/O interface subsystem to 16 (16-bit) channels
Communications	
1906	Universal controller (2/system) for 4-32 full-duplex channels
1905	Async controller (4/system) for 2-32 full-duplex channels
5710	Freestanding process data terminal
1115/1116	Async comm interfaces; 110-9,600 baud; 1 half-duplex channel
4810/4811	Async comm interfaces; 75-9,600 baud; 2 full-duplex channels
1911/1912	Async comm channels 2 full duplex lines
4825	Sync comm interface; 110-20K baud; 2 full-duplex channels
4820	16-bit parallel computer link; 100K wds/sec
5813	Async interface with remote fill hardware; 75-9,600 baud, 1 duplex channel
5820	High-speed computer link; 15K-125K wds/sec; 2 half-duplex channels and remote fill

Table 3. MODCOMP I, II, and IV: Software

Device Model	Description
MAX I	Core-resident batch system; requires 4K words of memory, ASR 33; for MODCOMP I
MAX II	Core for disc-resident batch system; requires multiply/divide, 12K words of memory, ASR 33, binary I/O device/paper tape, card, or mag tape; disc version requires DMP channel and 128K-word disc; for MODCOMP II or III
MAX III	Real-time multiprogramming system with foreground/ middleground/ background modes; foreground requires CPU multiply/ divide, 12K words of memory, ASR 33 console; background needs protect and 24K memory; disc version requires 128K disc; extended disc version requires 24K words of memory, 256K words disc; for MODCOMP II or III
MAX IV	Mapped version of MAX III for up to 256K words, (4 maps); requires MODCOMP IV CPU, 24K words of memory, 2.5M disc, ASR 33
MAXCOM	Communications run-time system for high throughput, low overhead; requires 4K words of memory, communications interfaces
MAXNET	Distributed network operating system; requires CPU, 32K words of memory, disc, ASR 33, communications links to satellite CPUs; for MODCOMP II
Assemblers	Standard requires 2K words of Memory and ASR 33; Extended requires 4K words of memory, real-time clock, and ASR 33; Macro requires 12K-word memory and II or IV CPU
Cross Assemblers	IBM 360/370, CDC 6000; both require 65K bytes of memory, card reader, line printer, card punch, disc or mag tape
FORTRAN IV	ANSI 2.9 1966; requires CPU, 20K words of memory, console
BASIC	Subset of macro assembler; generates absolute or relocatable code; also multiterminal Extended version; requires 12K memory, ASR 33
Utilities	Diagnostics, editing, media conversion loaders, debugging, math library

MODCOMP IV Dual Word Processor Computer is marketed in two basic configurations: the IV/10 and the IV/25. The IV/10 consists of a 32-bit and 16-bit arithmetic unit with multiply and divide hardware, a 32-bit parallel bus, executive features (real-time clock, console interrupt, and task scheduler interrupt), 15 general-purpose registers, a priority interrupt system with eight levels (expandable to 16 levels), 32K bytes of core memory with an effective cycle time of 640 nanoseconds for 16-bit words and 1.2 microseconds for 32-bit words, memory parity, memory expansion to 128K bytes with one, two, or four ports to memory, a power failsafe/auto start, control console, and a stall alarm.

Table 4. MODCOMP II: Submodels

SUBMODELS	5	10	20	25, 25CP	45, 45CP	200	220	12	26, 26CP	201	221	231
MEMORY												
Capacity												
Min K Bytes	8	32	8	32	32	64	64	64	64	64	64	64
Max K Bytes	64	64	128	128	128	128	128	128	128	128	128	128
Increments (K bytes)	8/16/32	8/16/32	8/16/32	8/16/32	8/16/32	8/16/32	8/16/32	64	64	64	64	64
Cycle (μsec)	0.8	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0
Parity	—	Std	—	Std	Std	Std	Std	Std	Std	Std	Std	Std
Protect	—	—	—	—	—	Std	Std	—	—	Std	Std	—
Ports	1	1	1	1	4	1	1	1	1	1	1	1
CPU												
Multiply/Divide	—	—	—	—	—	Std	Std	Std	Std	Std	Std	Std
INPUT/OUTPUT												
DMA	—	—	—	—	—	Std	Std	—	Std	Std	Std	Std
Modular Bus Control	—	—	—	—	—	—	—	—	—	—	—	Std
Peripheral Control	—	—	—	—	—	Std	Std	—	—	—	—	Std
Communications Macros	—	—	—	On CP	On CP	—	—	—	On Cp	Std	Std	—
Universal Communications MUX	—	—	—	—	—	—	—	—	—	—	—	Std
MUX Control	—	—	—	—	—	—	—	—	—	—	—	Std
Console/Paper Tape	—	—	—	—	—	Std	Std	—	Std	Std	Std	Std
Disc	—	—	—	—	—	—	Std	—	—	—	Std	—

The IV/25 has all the features of the IV/10 plus 16 sets of general-purpose registers (16 registers per set) and a memory management system permitting expansion to 512K bytes, which includes 1,024 memory mapping registers organized in four files of 256 registers, automatic memory allocation hardware, and memory protect on the basis of a 256-word page.

Optional features for the IV include 32K-byte modules of core memory, a simultaneous direct memory processor for up to 12 device controllers, an extended arithmetic unit for floating-point arithmetic (32-bit, 48-bit, and 64-bit operands), system protect compatibility with MODCOMP II, and 3-level increment of external interrupts.

Dual II and IV processors can share common core modules by way of the multiple port option. Special system products are available to link a MODCOMP computer to a CDC 3000 or 6000 by way of the CDC 3000 data channel, or to an IBM System/360 or 370 selector or multiplexor channel. Peripheral controller switches are also available for program or manual switching of up to four controllers between two MODCOMP computers.

The 32K-word memory module and the MAXNET IV communications package are under development for the IV.

COMPATIBILITY

MODCOMP systems are upward compatible in both hardware and software. The same functional hardware modules and the same peripheral devices are used in all systems. All programs are upward compatible.

In addition, programs assembled on large MODCOMP II, III, or IV configurations can run on small MODCOMP II or III configurations because unimplemented instructions are trapped and simulated by subroutines. Programs assembled on MODCOMP II or IV using the MODCOMP I instruction set can run on MODCOMP I.

FORTRAN-coded cross assemblers allow compilation of MODCOMP programs on the IBM System/360 and System/370 computers.

MAINTENANCE

Modular Computer Systems has 14 sales and 21 service centers located in the United States, Canada, and Puerto Rico. European headquarters are in Surrey, England, with marketing also in Germany. The company plans to expand its marketing organizations in Europe, Canada, and South America in fiscal 1975; currently only 15 percent of sales are from customers outside the United States.

Modular Computer does not rent systems. The company has four maintenance plans for purchased systems: resident service, full service, scheduled maintenance, and on-call. Resident service provides a trained service engineer on a 1-shift basis. Full service provides both scheduled and on-call emergency services for a single fee, while the other two plans are priced separately.

PRICE DATA

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSORS AND WORKING STORAGE		
	MODCOMP I		
I/5	General-Purpose 16-Bit Digital Computer	2,000	16
I/15	General-Purpose 16-Bit Digital Computer (same as I/5 except includes 3130 option plane, 3742 hardware fill, 3743 real-time clock, 3751 Teletype controller, 3750 control panel interface, 3131 programmer's control panel, 0011 I/O connector assembly, 0010 mounting slides)	3,600	25
I/25	General-Purpose 16-Bit Digital Computer (same as I/15 except with 16,384-word memory module; memory parity; power fail-safe/auto start)	7,400	64
	I/5 and I/15 Memory (max 32K)		
	Read/Write Core Memory (0.8-μsec cycle time)		
3603-1	4,096 Words	2,400	12
3608	8,192 Words	4,200	21
3609	16,384 Words	6,500	33
3607	Memory Parity	500	3
	I/5 and I/15 Processor Options		
3504	Multiply/Divide	700	4
3505	Custom Macro Instructions (requires 3130)	NA	NA
	MODCOMP I Input/Output and Interrupt Options		
0010	Slides for MODCOMP I Enclosure (for I/5 only)	70	NA
0011	I/O Connector Assembly	60	NA
3130	Option Plane	200	1
3131	Programmer's Control Panel	250	2
3709	Direct Memory Processor (requires 3130)	1,000	5
3741	Power Fail-Safe/Auto Start	300	2
3742	Hardware Fill	400	2
3743	Real-Time Clock	300	2
3750	Programmer's Control Panel Interface	150	1
	MODCOMP II		
II/5	General-Purpose 16-Bit Digital Computer (with 16,384-word memory included)	9,500	8
II/10	General-Purpose 16-Bit Digital Computer (same as II/5 except has multiply/divide; power fail-safe/auto start; memory parity; priority interrupts for executive features; executive features; and 16,384-word memory)	11,500	93
II/12	General-Purpose 16-Bit Computer (same as II/5 except 32K-word memory; arithmetic unit; ROM; memory expansion to 64K words; gen reg file with 15 regs; reg I/O and 8 interrupts; multiply/divide; power fail-safe/auto start)	13,000	
	With 64K-Word Memory	21,000	
II/20	General-Purpose 16-Bit Digital Computer (same as II/5 except modular bus control interface and memory expansion to 65K words)	5,000	50
	With 16,384-Word Memory Included	10,000	83
II/25	General-Purpose 16-Bit Digital Computer (same as II/20 except has multiply/divide; power fail-safe/auto start; memory parity; interrupt levels for executive features; executive features; and 16,384-word memory)	12,500	95
II/25/CP	Communication Processor (same as II/5 with 3513 communication macros and modular bus control logic)	16,000	130
II/26	General-Purpose 16-Bit Computer (same as II/12 with modular bus control interface and controller for both console and p tape reader; expandable for high-performance floating-point processor)	16,000	
	With 64K-Word Memory	24,000	
II/26CP	General-Purpose 16-Bit Computer (same as II/26 with communications macros and modular bus control logic)	20,500	
	With 64K-Word Memory	28,500	
II/45	General-Purpose 16-Bit Digital Computer (same as II/25 with Controller for Teletype and p tape reader; executive features)	16,500	135
II/45/CP	Communications Processor (same as II/45 with communication macros and modular bus control logic)	20,000	170
II/200	Computer System (II/25 CPU with 32,768 words of 800-nsec memory; CPU options required to support MAX III together with a PCI)	19,500	148
II/201	Computer System (same as II/26 with peripheral controller interface enclosure, direct memory processor, system protect; 1 cabinet included)	16,500	
	With 64K-Word Memory	24,500	
II/220	Computer System (II/25 CPU with 32,768 words of memory; options to support MAX III, PCI; moving-head disc; 2 cabinets)	32,000	260
II/221	Computer System (same as II/201 with 2.5M-word moving-head disc; 2 cabinets)	30,000	
	With 64K-Word Memory	38,000	
II/230	Communications System (II/25/CP with CPU options to support MAXCOM software system; PCI and universal communications multiplexor; mounted in 2 std cabinets)	29,500	219
II/231	General-Purpose 16-Bit Computer (same as II/26CP with peripheral control interface enclosure; direct memory processor; multiplexor controller and universal multiplexor; 2 cabinets included)	27,500	
	With 64K-Word Memory	35,500	

PRICE DATA (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSORS AND WORKING STORAGE (Cont'd.)		
	Memory Options for MODCOMP II		
	Read/Write Core Memory (0.8-μsec cycle time)		
3601-1	4,096 Words	2,400	12
3608	8,192 Words	4,200	21
3609	16,384 Words	6,500	33
3618	8,192 Words	4,200	21
3619	16,384 Words	6,500	33
3606	Memory Parity	500	3
	II/5/10/20/25 Processor Options		
3503	Multiply/Divide	500	3
3512	Hardware Floating Point	4,000	20
	Input/Output and Interrupt Options		
3704	Direct Memory Processor	1,500	8
3708	External Direct Memory Processor	4,000	40
3629	System Protect Feature (requires 3731)	1,000	5
3730/1	Priority Interrupt Group	500	3
3732	External Priority Interrupt (4 interrupt levels)	500	3
3737	Executive Features (includes real-time clock with 5-msec interrupt, console interrupt, and task scheduler interrupt; requires 3730)	500	3
3739	Power Fail-Safe/Auto Start Feature	500	3
	MODCOMP IV		
IV/10	General-Purpose Digital Computer	15,500	148
IV/20	General-Purpose Digital Computer (same as IV/10 with memory expansion to 384K bytes; context switching file with 240 reg; memory management system including 1,024 memory mapping reg consisting of 4 files of 256 registers each; auto memory allocation hardware; memory protect on a 256-word basis)	19,500	188
IV/25	General-Purpose Digital Computer (same as IV/10 with 16 sets of general-purpose registers containing 15 registers/set; memory management system permitting expansion to 512K bytes, including: 1,024 memory mapping registers consisting of 4 files of 256 registers each, automatic memory allocation hardware, and memory protect on a 256-word basis; 4-port memory interface)	23,500	224
	IV/10 and IV/25 Memory		
3661	Core Memory Module (32K bytes; 16-bit cycle time — 640 nsec; 32-bit cycle time — 1.2 μsec; 1 module included with CPU and required for lower half of each 64K-byte module pair)	8,000	40
3662	Core Memory Module (same as 3661 except used in upper half of each 64K-byte module pair)	6,000	30
	IV/10 and IV/25 Processor Options		
3712	Simultaneous Direct Memory Processor	4,000	30
3646	Dual Memory Ports	6,500	55
3515	Extended Arithmetic Unit	5,500	28
	IV/10 and IV/25 Input/Output and Interrupt Options		
3631	System Protect	1,500	8
3734	External Interrupt Group	500	3
3134	Remote Control Console Control Panel and Enclosure	1,000	10
	Input/Output and Interrupt Options for MODCOMP II		
3751	Controller (for Teletype and p t reader)	400	2
3752X	Controller (for async RS232C-compatible console device and for p tape reader)	400	4
3753-X	Controller (for async 420 console device and for p tape reader)	400	4
	MASS STORAGE		
	Fixed-Head Discs		
4103	262,144 Words (8.7-msec avg access time)	15,000	105
4104	524,288 Words (same as 4103)	19,000	133
4106	1,048,576 Words (same as 4103)	38,000	170
	Moving-Head Discs		
4126	1,299,200 Words (70-msec avg positioning time; 20-msec avg latency)[3]	11,000	99
4127	1,299,200 Words (same as 4126 except controller not included; requires 4126)[3]	7,000	84
4128	2,598,400 Words (same as 4126)[3]	14,000	126
4129	2,598,400 Words (same as 4128 except controller not included; requires 4128)[3]	10,000	111
4132	12,312,230 Words (35-msec avg positioning time; 12.5-msec avg latency)[3]	23,000	145
4133	12,312,230 Words (same as 4132 except controller not included; requires 4132)[3]	18,000	130
4134	26,624,640 Words (same as 4132)[3]	28,000	185
4135	26,624,640 Words (same as 4134 except controller not included; requires 4134)[3]	23,000	160
4140	Disc Cartridge (for 4126-4129)	180	NA
4141	Disc Pack (for 4132-4135)	500	NA

PRICE DATA (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
	INPUT/OUTPUT DEVICES		
4903[2]	Peripheral Controller (for 1-4 controllers)	1,200	6
4906	Peripheral Controller (switch for programmed switching of up to 4 controllers between 2 MODCOMP computers)	3,000	25
4701	Interval Timer	1,000	5
4701-10	External Clock	1,000	5
4801	General-Purpose Controller Module	600	—
4705-1	General-Purpose 16-Bit Data Terminal	1,500	15
4810/4811	Asynchronous Communications Interface	1,250	13
4815/17	Synchronous Communications Interface (2 full-duplex channels)	1,250	13
4820	Computer Link	4,000	40
	Teletypewriters		
4205	Data Communication Printer (tabletop; KSR; 30 cps)	4,400	38
4206	Data Communication Printer (same as 4205 except 120 cps; 120 print col; external forms tractor)	6,100	54
	Remote Teletypewriters		
4223	ASR 33	1,250	12
4224	KSR 35	3,250	55
4225	ASR 35	5,250	61
	Console Teletypewriters (require 3744 or 3751)		
4233	ASR 33	1,500	
4234	KSR 35	3,500	
4235	ASR 35	5,500	
3747/9	Programmable Power On/Off Controls for 4233 Teletypewriters	300	—
4253	Programmable Power On/Off Control for 4223 Typewriter	300	2
	Paper Tape		
4512	Paper Tape Reader and Punch	5,000	42
4513	Paper Tape Reader	2,000	12
	Floppy Discs		
4521	150-Word Storage Capacity (controller included)	4,000	40
4522	Dual; 300K-Word Storage Capacity	6,000	60
	Punched Card [3]		
4411	Card Reader (300 cpm; controller included)	4,000	24
4412	Card Reader (same as 4411 except 1,000 cpm)	9,000	54
4421	Card Punch (100 cpm; controller included)	30,000	162
	Line Printer [3]		
4211	600 lpm, 132 Columns	17,900	125
4213	50-150 lpm, 132 Columns	7,000	91
4214	300 lpm, 132 Columns	14,000	91
	DATA COMMUNICATIONS		
1905	Controller (for async communications multiplexor)	1,200	12
1910	Asynchronous Communications Multiplexor	1,600	16
1911/2/3	Asynchronous Communications Channel	500	5
1906-1	Controller (for universal communications multiplexor)	4,500	45
1920	Universal Communications Multiplexor	1,600	16
1922/3	Synchronous Communications Channel	1,200	12
1924/5/6	Asynchronous Communications Channel	1,000	10
1941	MODCOMP-CDC Satellite Coupler	8,000	80
1950	MODCOMP-IBM 360/370 Interface	7,000*	70
4216	Electrostatic Printer	9,000*	99
4217	Electrostatic Printer/Plotter	13,000	140
4219	VERSAPLOT Plotting Software	1,500*	—
4426	Keypunch/On-Line Card Punch/Automatic Interpreter	15,000	110

* Delivery subjects to home-office quotation.

Notes:
(1) Modular Computer has 4 maintenance plans — resident service, full service, scheduled maintenance, and on-call. Resident service provides a trained service engineer on a 1-shift basis at a cost of $32,000/year. This column lists the full-service maintenance charge. Cost of other plans available on request.
(2) No charge if purchased in conjunction with 3 or more peripheral controllers or analog input subsystem controllers.
(3) Requires any 4900 Series peripheral control unit.

HEADQUARTERS

Modular Computer Systems
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MODULAR COMPUTER SYSTEMS

MODCOMP I, II, and IV Report Update

Modular Computer Systems has introduced both a new 84 megabyte stand-alone disc drive system and a File Mangagement System supported by the firm's MAX IV real-time multiprogramming operating system. The company also announced price cuts of more than 17 percent on their 12.3 and 24.6 megabyte disc storage units.

NEW DISC DRIVE

The 3330-type disc drive contains its own regulated power supply and has an access time of 28 milliseconds. The system has a single-spindle design that provides 84 megabytes of storage per drive. Capacity can be increased in 84 megabyte increments, linking up to four drives with each controller.

A dual access option makes the new system well-suited for dual processor applications. One unit can be connected to two controllers, allowing two computers to read and write on the same disc.

Four different disc drive configurations are offered. A single disc drive is $28,000 and a drive with controller is $35,000. The drive with the dual access option costs $33,000 and the drive with dual access device and two controllers is priced at $46,000. The system will be available the last quarter of 1975.

NEW FILE MANAGEMENT SYSTEM

The File Manager, based on MODCOMP's MAX IV real-time operating system, provides the mechanism to organize, define, create, or destroy files, and to allocate space to and control access to data records. Files can be multilevel; data files and directories can be nested to any level. With the File Manager, the storage medium is divided into individually accessible files, allowing the user to define file families or libraries. This makes it easier for the user to access libraries of files.

File security is maintained with the File Manager. The system provides several mechanisms that permit the user to secure the files against unauthorized use or modification. The system is supplied at no cost with the MAX IV real-time multiprogramming operating system and will be available the last quarter of 1975.

74-451

OVERVIEW

The Prime series consists of three computers particularly oriented toward software and services designed for users' convenience. The main markets for the systems are currently data communications and industrial control. The largest system also competes in time-sharing and multiprogramming environments.

The Prime 200 is the "pivot" model in the line: it was first delivered in September 1972. The Prime 100 is essentially a slow 200 with a few features missing; it was first delivered in January 1973. The Prime 300 is much more powerful than the 200; it supports virtual memory and allows up to 50 million words of disc storage to be used as an extension of main memory. The 300 was first delivered in September 1973.

All three models are 16-bit microprogrammed minicomputers that feature all-MOS memory, instruction sets compatible with Honeywell Series-16 and extensive software. The 100 is a 4K- to 32K-word system (1.0 μsec memory cycle time), the 200 is a 4K- to 64K-word system (750-nanosecond memory cycle time), and the 300 is an 8K- to 256K-word system (600- or 750-nanosecond memory cycle time). The three systems are upward compatible and use the same system software and peripherals.

All three models can address up to 64 peripheral devices: magnetic tape and disc units, printers, paper tape and card equipment, communications devices and analog/digital equipment. The larger minicomputer manufacturers currently have a larger assortment of peripherals than Prime offers with its systems. However, Prime continues to add peripherals to its line, such as an IBM-compatible floppy disc and a 2314-compatible moving head disc.

The I/O structure for the line is flexible with five types of I/O channels available. Stack manipulation instructions and a 64-level priority interrupt system are standard features on all processors. The Prime 200 and 300 can also attach floating-point hardware; the 300 supports writable control store.

The Prime systems are particularly well suited to communications because of their DMC/DMT I/O facility. DMC is like a slower-speed DMA, with channel control words stored in memory instead of the DMA register file; there is no logical limit to the number of devices it can support. The DMT channel is faster than Prime's DMA channel because the current addresses for data transfers are supplied by device controller registers for DMT, rather than channel registers for DMA.

Communications functions are further supported by a line of synchronous and asynchronous single line and multiline controllers.

The software available is quite extensive: two full-fledged operating systems — DOS and RTOS, Macro Assembler, BASIC Interpreter and FORTRAN IV compiler can operate stand-alone. The Prime 300 uses virtual memory versions of the standard operating systems (DOS/VM and RTOS/VM).

There is no software especially geared to communications except the software drivers for the line controllers and the RTOS operating system.

The Prime processors are also marketed as processors for value-added networks and for satellite voice communications.

From its beginning, Prime has used all MOS memory for its computers, thus the company has had considerable experience with it. Prime developed the first 32K-word MOS memory board. It uses 4K chips from a variety of suppliers. The board is 16 by 18 inches. Table 1 lists the mainframe characteristics.

COMPETITIVE POSITION

The Prime series computers are marketed for industrial control and data communication applications. The line is not being marketed as liberators of H316s or DDP-516s, even though the Prime computers are program compatible with the Honeywell Series 16 computers.

In general, the Prime systems are cost and performance competitive with similar systems, and their hardware and software offerings are well-rounded. The focus on industrial control and data communications is a wise path for a small company to follow, for it can concentrate its resources and be truly competitive with larger companies.

The DMC/DMT I/O channels, together with the communications facilities and related software, make the

Table 1. Prime Computer Series: Mainframe Characteristics

CENTRAL PROCESSOR	100	200	300
Type (microprogrammed)	Yes	Yes	Yes
No. of Internal Registers	26	26	26
Addressing			
Direct	Yes	Yes	Yes
Indirect	Multilevel	Multilevel	Multilevel
Indexed	Yes	Yes	Yes
Instruction Set Implementation	Hardware	Hardware	Hardware
Number	112 std, 8 opt	117 std, 37 opt	145 std, 29 opt
Decimal Arithmetic	No	No	No
Floating-Point Arithmetic	Subroutine	Subroutine	Subroutine
User Microprogramming	No	No	Optional
Priority Interrupt Levels	64	64	64
MAIN STORAGE			
Type	MOS	MOS	MOS
Cycle Time (μsec)	1.0	0.75	0.60 or 0.75
Basic Addressable Unit	Wd (16 bits)	Wd (16 bits)	Wd (16 bits)
Bytes/Access	2; 4	2; 4	2; 4
Cache Memory	No	No	No
Min Capacity (wds)	4K	4K	8K
Max Capacity (wds)	32K	32K std, 64K opt	256K
Increment Size (wds)	4K; 8K	4K; 8K	8K; 32K
Ports/Module	1	1	1
Error Checks	None	Parity	Parity
Protection Method	None	None	Software
Memory Management	No	No	Yes
ROM			
Use	Bootstrap loader, control store	Bootstrap loader, control store	Bootstrap loader, control store
I/O CHANNELS			
Programmed I/O	Yes	Yes	Yes
Direct Memory I/O (no. of subchannels)			
DMA	8 (programmable)	8 (programmable)	8 (programmable)
DMT	No limit	No limit	No limit
DMC	4,096	4,096	4,096
Max Xfer Rate (wds/sec)			
Over DMA	694,444	925,925	1,157,406
Over DMC	225,225	271,739	339,674
Over DMT	694,444	1,084,956	1,250,000

systems particularly good for communications applications. The RTOS operating system allows foreground/background processing, combining real-time data acquisition and control in the background with program development in the foreground. The addition of the larger, faster Prime 300 system adds to the line's range of processing power in both markets, and strengthens its competitive position for multiprogramming and time-sharing applications through the standard memory mapping and virtual memory techniques.

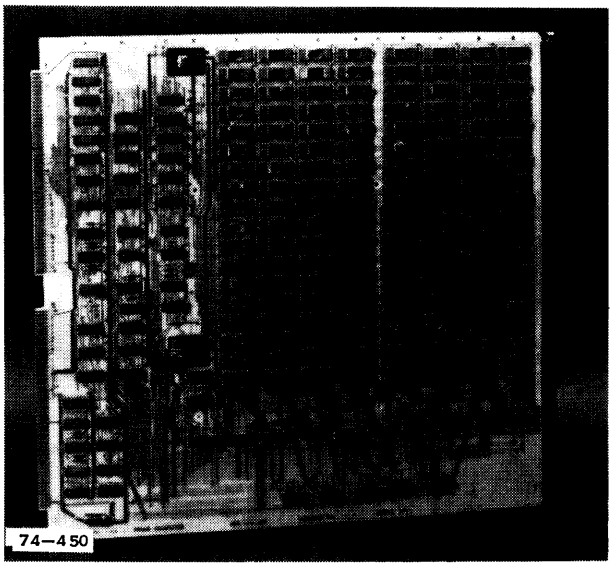
The Prime 100 competes with the DEC PDP-8, PDP-11/05, and 11/10; Data General Nova 1200, and ECLIPSE S/100; and Interdata Model 7/16. The Prime 200 competes with the DEC PDP-11/40, Data General Nova 800, ECLIPSE S/200, Interdata Models 70/80 and 7/16, and General Automation SPC-16. The Prime 300 competes in the upper range of minicomputers with such systems as DEC PDP-11/45, Interdata 7/32, Varian Data Machines V74, MODCOMP IV and Hewlett-Packard HP 21MX.

Some of the competitive systems with the 100 and 200 can expand memory beyond 64K words and can use memory management systems that make them more appropriate for multiprogramming and real-time applications. The Prime 100 and 200 computers do not have hardware memory protection, but the Prime 300 does. It also has a relatively sophisticated memory management option, allowing addressing of up to 256K words of real memory.

Although some manufacturers have had considerable difficulty with MOS memory reliability, Prime has developed a board testing technique to allow consistent production of reliable large memories.

USER REACTIONS

Users we contacted were unanimous in extolling Prime's service and support organization, and its general attitude of helpfulness when any problem arose. One user had some of its first new DAC boards and had some problems with the Digital Output module. This user expected some problems with a new item, however, and felt confident the company would soon set things right. Another user had a Prime 300 system for more than a



year, and the system had been down only twice: once for an hour, and once, when a part had to be flown in, for less than a day.

Users generally bought the Prime systems after considering the larger, well-established minicomputer manufacturers.

Appliance manufacturer. A large appliance manufacturer using a Prime 300 chose the system over those manufactured by Digital and Hewlett-Packard because the company had high performance demands and limited funds. This 32K-word virtual memory system supports engineering design and test functions in a time-shared mode. Various data acquisition instruments are attached to the system, as well as a number of Tektronix graphics terminals. This user is pleased with the result; interfacing to the system has been easy. This user felt the documentation for interfacing could be improved, however. When we spoke to him, he had placed an order for the hardware floating-point processor and was waiting for the RTOS-VM A/D and D/A software drivers to be completed, so they could run their data acquisition system under RTOS instead of DOS.

Newspaper Production. Another user bought Prime 200 systems to control a line of automated newspaper production systems. This user looked at Digital, Data General, and others before selecting the 200. The Prime system attracted them because this company already had used Honeywell 316s to run its phototypesetters, and some of the already developed software could be used on the Prime 200. This user feels Prime has particularly good documentation for its software, an important point because the documentation tended to be used over and over again, whereas hardware interfacing documentation problems were usually one-shot affairs.

Diversified Manufacturer. A very large diversified manufacturer selected the Prime 300 as the processing unit for a product line in telecommunications routing centers. The CPUs in the system will be used for switching, logging, and routing functions for TV, telephone, and data transmission via satellite. The manufacturer began developing the system using a Honeywell Series 16 processor, but became very dissatisfied with Honeywell's service. The company discovered the Prime product line and is delighted with the change; the Prime 300 is faster, costs less, and has more expansion capability than the Honeywell system. The Prime system software was one of its strong points. This user will undoubtedly become one of Prime Computer's larger accounts; each routing system will consist not only of multiple CPUs (two to four), but also discs, tape drives, and printers — in short, a whole system OEMed, not just the processor.

CONFIGURATION GUIDE

Minimum configurations include a processor with 4K or 8K words of MOS memory, programmed I/O, eight programmable DMA channels, power supply, 64-level vectored priority interrupt system, and console. Basic systems provide additional subassembly slots for memory expansion modules and I/O device interfaces. The basic models have five standard subassembly slots; 10 or 17 are optional. Each 4K-, 8K-, or 32K-word memory modules requires one slot, and the central processor requires one slot. Modules can be arranged in any order on the universal bus system.

Table 2 lists the peripherals available for the Prime computers.

Table 2. Prime Computer Series: Peripherals

Magnetic Disc. Moving Head: Capacities of 1.5M wds, 3.0M wds, 12.0M wds (access time 15 msec min, 70 msec avg, 110 msec max; 12.5 msec avg latency) and 25M wds (IBM 2314-type).
Fixed Head: 128K wds, 256K wds capacity.
Diskette: 138 wds. (IBM-compatible.)

Magnetic Tape. 7-track, 800 bpi, 45 ips; 9-track, 800 bpi, 45 ips.

Punched Card. 150 to 300 cpm reader, 400 cpm/100-285 cpm Reader/Punch.

Graphics Display. Alphanumeric Display with keyboard.

Printer. 165 cps Serial Printer; 300 lpm line printer; Both 132 col.

Paper Tape. Readers at 200 cps; reader/punch at 200/75 cps respectively. 8-channel fanfold tape.

Teletypes. TTY 33 ASR, KSR; TTY 35 ASR characteristics.

Analog/Digital. A/D Conversion, D/A Conversion subsystems; Digital Input and Digital Output Subsystems.

Communications. Async multiline controllers, sync multiline controller, multiple auto call interface.

Prime offers central processor in four submodels for the 100 Series, in 12 submodels for the 200, and in six submodels for the 300. Processor models vary in basic memory size, electrical environment, mounting chassis, and standard processor features, at prices slightly lower than adding them optionally to the processors.

The 200 Series processors have a few standard features that are available as options for the 100 Series; byte parity and an asynchronous serial communications interface are standard features, for instance. In most respects, the 100 is a slower 200, with essentially the same features on a smaller scale.

Memory can be incremented in modules of 4K, 8K, or 32K words. The I/O bus can handle a maximum of eight controllers for high-speed DMA devices like magnetic discs and tapes. All eight can operate simultaneously and time share the I/O bus. Devices with their own control registers can also use the ultra-high-speed DMT channel, which is optional on both the 100 and 200 and standard on the 300. Slower-speed devices like the serial printer, paper tape, card I/O devices, Teletypes, and the analog/digital and communications interfaces use programmed I/O or the DMC — optional on either the 100 or 200 and standard on the 300. The DMC can handle a maximum of 4,096 individual devices, although the system as a whole can directly address only 64 device controllers. The DMC channel requires four memory cycles for each word transferred.

A minimum 300 Series system is similar to a 200 Series minimum system with most options included as standard. For instance, all 200 Series models have the following options to expand processing power: extended addressing to 64K words of memory, hardware multiply/divide, double precision arithmetic, micro-verification routines, automatic program loading from paper tape, and DMC/DMT channels.

These items are standard on the 300 Series, except extended addressing is to 256K words of memory. The following major features provided for the 300 Series are unavailable for the 100/200 Series:

- Virtual memory addressing to 64K words.
- Physical MOS memory capacity to 256K words with virtual memory up to disc capacity.
- Two distinct processor modes — paging mode and restricted mode — can be designated separately or together to allow processing at user, supervisor, or base operating level.
- Memory cycle time of 600 nanoseconds per word.
- Optional floating-point processor that executes 19 floating-point instructions.
- Writable control store.

Three special interfaces are provided: one allows a user's own device to connect to a system, a second allows controllers from the Honeywell Series 16 computers to interface to a system, and the third allows a second Prime processor to be linked to a system.

COMPATIBILITY

Prime 100 and 200 Series computers are completely program-compatible; given the appropriate configuration, programs compiled on one computer can run on the other. The 100 Series uses a subset of the 200 Series instruction set. Both processors have an "unimplemented instruction" trap that allows a jump to a subroutine to perform the missing instruction. Honeywell Series 16 programs can be run on either the 100 or 200. Both Prime computers use the same software and peripherals, but they use different memory modules. The 100 Series modules do not include memory parity; the modules used with the 200 Series include two parity bits per word, one per byte.

Both the Prime 100 and 200 are upward compatible with the Prime 300. The use of the unimplemented instruction trap on the smaller computers means that programs compiled on the 300 can run on the 100 and 200 as well. The 300 also has the trap, but since all 100 and 200 instructions are standard on the 300, there is no immediate use for it. Table 3 lists the software packages available for the Prime computers.

MAINTENANCE AND SUPPORT

Prime markets its systems through its own sales and service facilities, and also through representatives. There are 11 sales offices in the United States, and four service centers (Massachusetts, Pennsylvania, Michigan, and California), as well as offices in England, Germany, Sweden, Denmark, Norway, Finland, Belgium, Switzerland, Austria, Netherlands, and Australia. All systems are sold, with monthly maintenance contracts available. These provide for both preventive maintenance and emergency service. Software is warranted for one year, with revisions and corrections made free of charge during that period.

Table 3. Prime Computer Series: Software

Package Software	Configuration Required	Comments
OPERATING SYSTEMS		
DOS	8K memory; Teletype ASR and interface; real-time clock; disc	Basic batch operating system for PRIME computers; written in Fortran; multiple directories, volume control, and access methods. Can run as background task under RTOS-VM.
RTOS	8K memory; Teletype ASR and interface; real-time clock	Compact, real-time multiprogramming system; can be disc- or memory-resident.
RTOS-VM	32K memory; Teletype ASR and interface; real-time clock; disc	Like RTOS but with paging algorithm, swapping, protection.

Table 3. (Contd.)

Package Software	Configuration Required	Comments
DOS-VM	Same as RTOS-VM	Up to 15 users can time-share with each user up to 64K words of memory.
ASSEMBLERS/ COMPILERS		
FORTRAN IV	12K memory; Teletype ASR and interface	One-pass compiler, extended instruction set, support library.
Macro Assembler	Minimum configuration	Pseudo Ops, symbol and data definition, program linking, storage allocation, user-defined macros.
Micro Assembler	32K memory; DOS or DOS-VM	For symbolic assembly of micro-code on model 300 with WCS.
BASIC UTILITIES	12K memory, Teletype	Extended; batch, conversational and immediate modes.
Desectorizing Link Loader	Minimum configuration	Loads, links, binds relocatable, or absolute program modules.
I/O Control Subsystem	Minimum configuration	Control routines and device drives; includes source file editing and merging.
Editors	Minimum configuration	Full-context editor for editing lines, characters, and multiple changes of same text in program.

TYPICAL PRICES

Model Number	Description	Purchase $
	Prime 100 Central Processors	
P1004A-05	Prime 100 Central Processor unit (with 4K wds of MOS memory; 1 μsec; 8-chan programmable DMA; full addressing modes; virtual instruction package; 4-chan, bit serial full-duplex interface; 5-board chassis; multi-level vectored priority interrupt system)	4,600
P1004A-10	Prime 100 in 10-board chassis	5,600
P1004A-17	Prime 100 in 17-board chassis	7,600
	Prime 200 Central Processors	
P2004B-05	Prime 200 Central Processor Unit (with 4K wds of MOS memory, 750 nsecs, byte parity; full addressing modes; 8-chan programmable DMA; multi-level vectored priority interrupt system; virtual instruction package; power supply; 10-board chassis; interface)	5,600
P2004B-10	Prime 200 in 10-board chassis	6,500
P2004B-17	Prime 200 in 17-board chassis	8,400
	Prime 300 Central Processors	
P3008B-05	Prime 300 Central Processor Unit (with 8K wds of MOS memory; 750 nsec; virtual memory; stack procedure instructions; microverification routines; hardware multiply/divide; double-precision arithmetic; DMC/DMT Capability; automatic program load; byte parity; full addressing modes; virtual instruction package; 8-chan programmable DMA; bit serial full duplex interface; Multi-level vectored priority interrupt system; 5-board chassis)	11,700
P3008B-10	Prime 300 in 10-board chassis	12,500
P3008C-10	P3008B-05 with 600-nsec memory in 10-board chassis	13,000
	Prime 100 Options	
157	Hardware multiply/divide, double-precision arithmetic and DMC/DMT capability	1,000
	Prime 200 Options	
253	Microverification routines	800
257	Hardware multiply/divide, double-precision arithmetic, DMC/DMT capability, and microverification routines	1,000
	Prime 300 Options	
361	Writeable control store (256 wds, 64 bits per microinstruction)	3,500
362	Double-and single-precision floating-point arithmetic, and writeable control store	5,000
369	Microprogramming training course, 1 man, 1 wk	1,000
	Prime 100 and 200 Options	
150/250	Hardware multiply/divide and double-precision arithmetic	800
151/251	DMC/DMT capability	500
142/242	Automatic program load from Teletype and paper tape reader	400
145/245	Automatic program load from multi-devices; includes Teletype, paper tape reader, disc, magnetic tape	600
	Prime 200 and 300 Options	
9501	Field Exerciser Panel (FEP); display unit, control unit and cable	600
260/360	Double-and single-precision floating-point arithmetic (14-digit accuracy)	2,000
	Prime 100, 200, & 300 Options	
146/246/346	Custom automatic program loader (256x16-bit wds)	600
147/247/347	One-time documentation charge for custom APL	1,200
140/240/340	Power monitor, power failure interrupt and automatic restart protection including battery backup for standby power for MOS memory	600
141/241/341	Additional battery	200
	MASS STORAGE	
	Discs and Diskettes	
4000	Disc controller for any combination of two fixed-head and for moving head discs	3,500
4103/5	128K/256K word fixed-head disc	9,500/ 11,000
4121	1.5M word moving-head disc	7,500
4123	3.0M word moving-head disc	9,500
4127	6.0M word moving-head disc	11,500
4300	Diskette controller and 2 drives	5,200
4166/67	Diskette cartridge, IBM/Prime format (73/77 data tracks)	25
	Prime 100 Memory Expansion	
UM008A-016A	8K board, 1-μsec cycle time; no parity	3,800

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $
UM016A-032A through UM048A-064A	16K board, 1-μsec cycle time; no parity (16K to 32K to 48K to 64K words)	6,800
UM032B-064B	32K board, 750-nsec cycle time; parity	11,000
UM008B-016B	8K board, 750-nsec cycle time; parity	3,900
	INPUT/OUTPUT	
3006/7	Real-time clock (line or external frequency), async line controller	1,800
3022	Sync line control capability	200
3023	Watchdog Timer (100 msec, RTC/PRTC, or external interval)	300
3025	Second 16-bit buffered parallel I/O controller (hdx)	500
3101	Teletype ASR 33	1,500
3103	Teletype KSR 33	1,200
3105	Teletype ASR 35	4,800
3121	Paper tape reader; 200 cps, for fan-fold 8-chan paper tape	1,900
3123	Paper tape reader/punch (reads 200 cps, punches 75 cps, for fan-fold 8-chan paper tape)	3,800
3141	Controller and card reader (300 cpm, binary and Hollerith formats)	5,000
3181	Controller and card reader/punch (400 cpm reader/100-285 cpm punch)	25,000
3161	Controller and line printer (300 lpm, 132 col, 64 char)	12,000
3191	Controller and card reader and line printer	17,000
3195	Controller and card reader/punch and line printer	34,500
3127	Character printer: 165 cps, EIA RS232-C compatible	6,000
4020	Controller for up to 4 magnetic tape transports	3,500
4141/3	Magnetic tape transport: 7/9 track, 45 ips, 556/800 bpi, industry compatible	7,000
3129	Alphanumeric CRT with keyboard, EIA RS232-C compatible	3,100
7000	General-Purpose Interface Board	1,200
7010	General-Purpose Interface Board	1,500
7030	Interprocessor Controller	3,500
	Async Multi-Line Controllers (AMLC; RS232-C/CCITT V24 compatible)	
5002/4	AMLC (for 103/202 data sets; 8/16 lines)	4,000/5,000
5052/4	AMLC (for direct connected devices; 8/16 lines)	2,600/3,000
5201/2/3/4	Multiple Sync Line Controller (RS232C compatible; for 201/203 data sets; 1/2/3/4 lines; + $200/line)	2,400
5244	Byte packing and char recognition (SYN, DLE, EOM, special)	400
5245	Byte packing, char recognition, transparent mode, and CRC12, CRC16, CRCCCITT, LRC	800
5246	Hardware bisync procedures for USASCII, EBCDIC, and SBTC codes	800
5402	MACI for 801 autocall units (4 lines)	2,000

HEADQUARTERS

Prime Computer
145 Pennsylvania Avenue
Framingham MA 01701
(617) 879-2960

PRIME COMPUTER

Prime 100, 200, and 300 Series System Report Update

A new version of Prime Computer's 300 time-sharing system allows up to 31 simultaneous users 128K bytes of virtual memory each and direct access to all peripheral devices from a user terminal. The system has 512K bytes of MOS main memory, floating-point arithmetic hardware, a 32-line asynchronous multiline controller, line printer, and 60M-byte disc pack. Programs can be written in any Prime programming language, including FORTRAN and BASIC, as well as MACRO and MICRO machine language. Each user has access to a complete virtual computer under control of microprogrammed memory management hardware and new features added to Prime's disc operating system.

The virtual memory disc operating system has the following features:

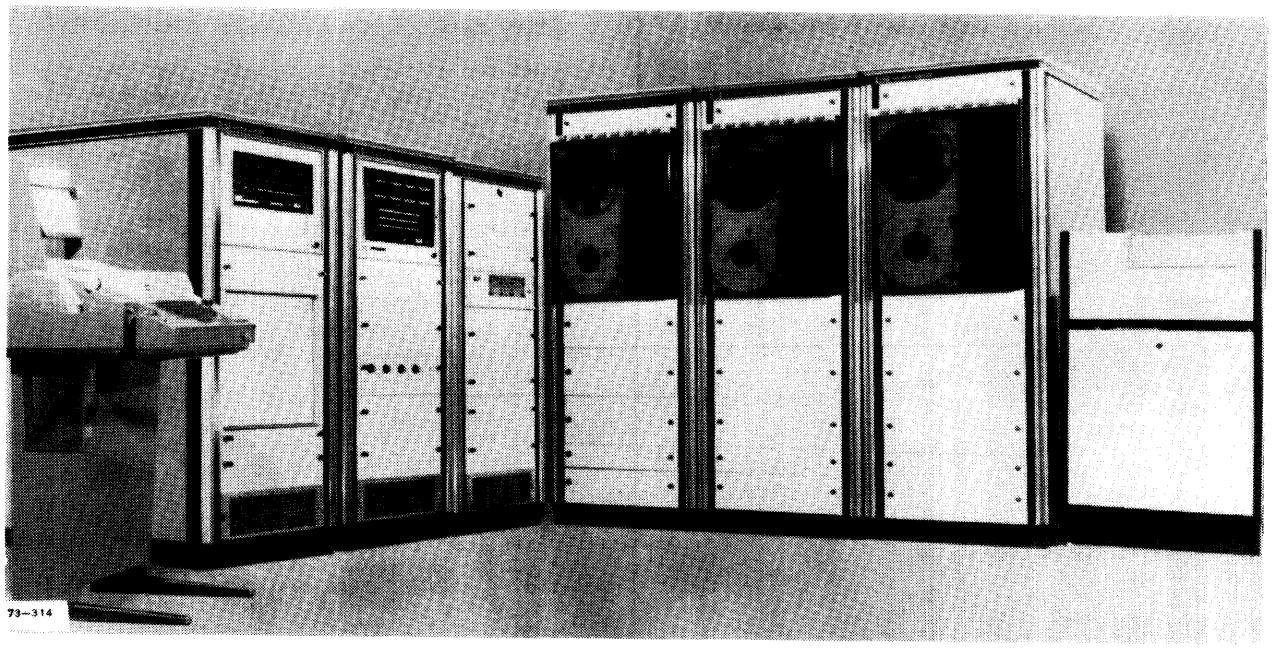
- Automatic log-out to prevent inactive but connected terminals from holding system resources beyond a predetermined time limit.
- Read/write lock for file security — controls user access to all files through a system of file access control keys, which determine how users can access files and how files can be read, written, or deleted.
- A main memory scan tests the computer's main memory and bypasses any faulty locations identified.

An important new hardware feature is the Universal Disc Controller that can control any mix of four cartridge or disc pack units (6M, 12M, or 60M bytes capacity) and a fixed-head disc. A variety of disc units can be added to a system without using multiple controllers.

Primary competition for the new system is the Hewlett-Packard HP 3000 Series and the Digital Equipment DECSystem 10. The Prime system is already in use in a variety of applications in the United States and England. Purchase price ranges from under $50,000 for a 4-user system to approximately $165,000 for a 31-user system. Deliveries are scheduled 30 to 60 days after receipt of order.

HEADQUARTERS

Prime Computer, Inc.
145 Pennsylvania Ave.
Framingham MA 01701



OVERVIEW

RDS-500 is a general-purpose minicomputer that can operate in a variety of applications: real-time control, high-speed data acquisition, medical and laboratory data collection and analysis, and commercial data processing. The system was first delivered in March 1974. Raytheon offers a number of configuration options as well as language compilers and software utility packages for the system.

One interesting feature is that memories of different speeds can be mixed on one system: the RDS-500 has an internal asynchronous "Superbus I" which connects the CPU, memory, programmed I/O, and DMA direct memory access channels. Peripheral devices can connect to the DMA, and memory can be accessed simultaneously with the CPU because a second internal "Superbus II" attaches to a second port to memory.

A microprogrammed "Apollo" array processor is available to process seismic and signal data independently of the CPU; it uses hardware floating-point, dual port attachment, bit array manipulation, and command chaining to achieve high processing speeds.

Analog/digital, digital/analog subsystems are controlled by a single universal front-end interface called the "Nest" which connects to either DMA or programmable DIO (direct input-output) channels. The Nest and Apollo are recent improvements to the 500 series. Mainframe characteristics are listed in Table 1.

Peripherals available for the system provide for a fine selection of performance ranges. Fixed or removable discs and removable disc cartridges are available. Seven tape drives, three line printers, four character printers, paper tape equipment, punched card equipment, displays, digital plotters, buffered digital channels, and communications devices round out the picture. Peripherals are listed in Table 2.

Software for the system becomes more complex as the system configuration expands. The Basic system precludes any high-speed input devices; the standard operating system (SOS) is essentially manual and runs on a "standard" configuration; it handles all peripherals but disc. The Magnetic Tape Operating System handles assembly, compilation, and execution of one or more programs automatically; it runs on an Extended configuration. The Extended configuration also supports the Real-Time Operating System (RTOS), which handles a full complement of peripheral types. The Multiprogramming System (MPS) is a superset of RTOS; it offers a variety of capabilities including time sharing. System software characteristics are listed in Table 3.

Languages offered are conversational FORTRAN, FORTRAN IV, RPG II, as well as SYM I and SYM II assembler languages.

COMPETITIVE POSITION

Raytheon supplies computers primarily for real-time control and high-speed data acquisition applications. A substantial number of systems has been supplied to similar types of military applications. Since its first system was installed in 1960, Raytheon has delivered more than 900 computer systems; over 700 of these systems are computers from the 700 line. Over 150 RDS-500 systems have been sold. Raytheon computers have been used in such diverse applications as aircraft simulator control, closed-loop process control, airline reservations, seismic data

Table 1. Raytheon RDS-500: Mainframe Characteristics

Central Processor	
Type (microprogrammed)	No
Control Memory (RAM, ROM)	No
Size	
Use	
No. of Internal Registers	8 general-purpose
Addressing	
Direct (no. of wds)	2K, combined with page pointer to make 64K
Indirect	Via register only
Indexed	64K
Instruction Set Implementation (hardware, firmware)	Hardware
Number (standard; optional)	98; 132
Decimal Arithmetic	No
Floating Point Arithmetic	Hardware or software, multiple precision
User Microprogramming	No
Priority Interrupt System Operation Modes Levels	16
Main Storage	
Type	Core
Cycle Time (μsec)	0.8; 0.9
Basic Addressable Unit	16-bit word or 8-bit byte
Bytes per Access	2
Cache Memory	No
Min Capacity (wds)	8K
Max Capacity (wds)	64K
Increments Size (wds)	8K; 16K
Ports per Module	2
Error Checks	Parity (opt)
Protection Method	opt
Memory Management	No
ROM	
Use	—
Capacity (wds)	265
I/O Channels	
Programmed I/O	16 controllers
DMA Channels	8 or 16 controllers
Multiplexed I/O (no. subchannels)	No
Max Transfer Rate	
Over DMA (words/second)	1M (2M aggregate with dual-ported memory)
Simultaneous Operations	2

processing, on-line testing, pipeline station control, signal data analyses, medical research, vibration and shock testing, and laboratory data collection and analysis. Systems are sold and maintained in Europe as well as in the United States; the company's European headquarters is in Amsterdam, Netherlands.

For general-purpose minicomputer applications like medical and laboratory data collection and analysis and commercial data processing, the Raytheon RDS-500 competes with most other minicomputers, for example, DEC's PDP-11, the Data General Nova/Supernova line, and the HP 2100 line. In the process control market, Raytheon meets both the larger minicomputer manufacturers capable of the extensive support needed for these applications and systems that aim particularly at process control, such as the Honeywell 4000 line (formerly GEPAC), IBM 1800 and its lookalikes from General Automation and Digital Scientific, and IBM System/7, Foxboro Fox 2, and General Automation's SPC-16 series.

Table 2. Raytheon RDS-500: Peripherals

Magnetic Disc — Fixed Disc: 3M/6M-wd capacity; 143K or 187K wd/sec transfer rate; 8.5 msec avg access time.

Removable Disc Cartridge: 1.28M-wd capacity; 80K wd/sec transfer rate; 70 msec avg access time.

Removable Disc Pack: 12.99M-wd or 25.98M-wd capacities; 128K wd/sec transfer rate; 32 msec avg access time.

Magnetic Tape — 7- and 9-track; either at 37.5/75/125 ips; 556/800 bpi, 800 bpi; and 800/1,600 bpi 21-track tape.

Punched Card — Readers at 300 or 1,000 cpm, 80-col cards. Punches at 100-400 cpm.

Printers — 10 cps char printer; 245-1,100 lpm/1,250 lpm/356-1,110 lpm. 80 to 132 col. 64 char.

Printer/Plotter — 3,240 lpm electrostatic nonimpact printer, 132 col/line; 32,400 plotting speed.

Paper Tape — Reads at 300 cps; punches at 110 cps.

Displays — 2,520 char; 35 lines; 72 col; 1,024 x 780 matrix.

Clock and Timer — 16-bit counter with 10- or 100-sec time base, max interval of 0.65 or 6.5 sec; also time-of-day clock in 32 or 36 programmable bits.

Digital Plotters — 11-in. Y axis, 120-ft X axis; 0.010 or 0.005-in. or 0.10mm increment; or 28.55-in. Y axis, 120-ft X axis; 0.010 or 0.005-in. or 0.10 mm increments; speeds from 200 to 300 increments/sec.

Buffered Digital Channels — Digital Input/Output Unit, "Nest" Analog-to-Digital and Digital-to-Analog Front-End Interface.

Communications — Synchronous modem controller, serial line multiplexor.

In the special data acquisition applications related to seismic and signal data processing, Raytheon meets a number of other systems from less well-known manufacturers, such as the Computer Signal Processors CSP-30 and the Unicomp COMP-16 and 18. Raytheon's past experience, in addition to the high performance capabilities of the Apollo array processor, makes the RDS-500 particularly competitive in the latter market.

User Reactions

Two RDS-500 users were interviewed for this report: one uses two systems for process research and the other uses two systems for seismic data processing. Both have Apollo array processors on their systems. The first user bought Apollo as an afterthought while array processing is integral to the second user's application. Both users had previous experience with Raytheon as a vendor because both had 704s in house. Both find the RDS-500 considerably more powerful and easier to use because it does more with upcode than the 704. Both agree the hardware is good and reliable. Both use the MPS operating system and feel the Monitor is the best on the market for interfacing to fast real-time processes. These are handled in the foreground while a batch processor for generating reports, developing programs, or executing programs runs in the background. Both systems came up quickly once power was turned on.

The user with the process control application has had the systems installed for about six weeks and has had only one memory failure since installation. The systems are running, but there are still problems with them. The problems with the Monitor are in-line with what one expects from a process control installation where real-time

Table 3. Raytheon RDS-500: Software Configurations

PACK-AGE	DESCRIPTION	MINIMUM CONFIGURATION	OTHER DEVICES SUPPORTED	SOFTWARE SUPPORTED
Basic System	Modules common to all; X-RAY executive, resident monitor, editor,* assembler,* IOS, Conversational FORTRAN, math library, operating system for use without disc	8K-wd memory; ASR 33 TTY	ASR 35; multiply/divide	PTIOS; Basic Loader; SENSOR diagnostics
SOS	Operating system for use without disc	8K-wd memory; ASR 33 TTY; paper tape or card reader	ASR 35; multiply/divide; power fail; DMA; card & tape punches; printers; plotters; mag tape serial MUX	Basic system software + std loader, FORTRAN IV, SENSOR diagnostics, Trace-Debug
MTOS	Magnetic Tape Operating System	8K-wd memory; ASR 33; mag tape; DMA; paper tape or card reader	All SOS devices + operator interrupt	Basic system software + std loader, PTIOS, FORTRAN IV, Trace-Debug, system generator
RTOS	Real-Time Operating System	8K-wd memory; ASR 33; disc; DMA; paper tape or card reader	All SOS devices + operator interrupt	Basic system software + disc loader, PTIOS, FORTRAN IV, Trace-Debug, system generator, SENSOR diagnostics, sort/merge
MPS	Multiprogramming Operating System	8K-wd memory; ASR 33; disc; DMA; paper tape or card reader	All SOS devices + time-of-day clock, MPS, memory protect, operator interrupt	Basic system software + disc loader, PTIOS, FORTRAN IV, Trace-Debug, system generator, Sort/Merge, SENSOR diagnostics

*SYM I Assembler with Basic, SOS systems; SYM II with others. Operating systems have system editor as well as symbolic program editor.

processes are interfaced. The Monitor does what Raytheon says it will do and the user is pleased with it. Raytheon is working with them to clear up problems.

This user did not look at other vendors because the system applications software was developed on the 704 and the RD5-500 is upward compatible with the 704. Originally, the 704 was selected because of its software. Before purchasing the array processor, the user did look at other vendors, notably from Floating Point Systems. Although their array processor is more powerful than Apollo, the user was afraid of incompatibility with the RDS-500 software. The user ended up writing his own driver for Apollo anyway and found it easy to do.

This user has found the utilities inconsistent from one to another and feels Raytheon fell down on the system approach when writing them, particularly with regard to the user interface. Batch Edit, for example, has been unworkable and will be replaced by a user-written version.

Overall the user is pleased with the system and expects to have the bugs ironed out on schedule.

The user with the seismic data processing application looked at the equipment from 15 vendors and determined that only two systems could do the job satisfactorily: Texas Instruments' TI980 and the RDS-500. The TI980 was eventually ruled out because the RDS-500 software was better suited to the application.

The RDS-500 was selected primarily for the following reasons:

- Raytheon produces a full range of peripherals for seismic data processing, such as 21-track magnetic tapes and large, fast fixed-head discs.
- 21-track tape.
- 3M-word fixed-head disc, 8.5-millisecond average access time.
- 6M-word fixed-head disc, 8.5-millisecond average access time.
- CPU architecture with dual-bus structure and dual-port memories.
- Reliable hardware and all available from Raytheon with no need to integrate other vendors' hardware.
- High-speed, 9-track magnetic tape, 125 inches per second.
- Almost all devices allow data chaining; not available from other vendors.

This user feels the Monitor is especially flexible because it is relocatable as are all the peripheral drivers. The Monitor can be Sypgened for a specific configuration in about ten minutes. The RDS-500 CPU was designed to operate on 500-nanosecond cycle; thus the system is memory bound with the 700-nanosecond memories currently available. When faster memories are available, they can be interfaced immediately without difficulty.

This user would like some additional features. Although the system has eight general-purpose registers,

they are not completely useable as such. Because of compatibility with the 704, instructions tend to use only the accumulator and index register. This user would like a Swap instruction to exchange the contents of any two registers.

This user's application was an RDS-500 alpha test site, and thus the systems have been operating for over a year. Raytheon has been most cooperative on software and hardware problems, and the service has ben excellent. The user volunteered that he was pleased and proud of his operating system.

We asked about the RDS-500 utilities. This user has found them more powerful than the 704 utilities. They must be used from the RDS-500 perspective because they function differently than those for the 704.

CONFIGURATION GUIDE

Three types of configurations are identified: Basic, Standard, and Extended. The configuration type indicates the hardware/software package and the devices the software can support. The Basic system has no high-speed input device. The Standard system is punched card or paper-tape oriented, but can handle magnetic tape. The Extended system accommodates magnetic tape and disc, and any other peripheral Raytheon sells for the system.

A minimum RDS-500 system includes the following components:

- CPU, with eight general-purpose registers, 98 basic instructions, DIO bus logic, 16-level interrupt system for DIO, hardware bootstrap, TTY controller, and power failsafe.
- 8K words of memory.
- ASR 33 Teletype.
- Operator panel.

DMA channels, hardware multiply/divide, multiprogramming protection, parity, and hardware floating point can be added as optional features, which also add a total of 34 instructions. Additional 8K-word (800-nanosecond cycle time) and 16K-word (900-nanosecond cycle time) core memory boards allow memory expansion to a maximum of 64K words. Memories with different speeds can be mixed on a system. Raytheon expects to add MOS, bipolar, and ROM modules with various speeds and capacities that can be mixed on the asynchronous bus. A memory module with cycle time of 500 nanoseconds is planned.

Most DIO controllers control a single device, such as a printer, card or paper tape reader or punch, or communications interface. An exception is the serial multiplexor, which controls up to four devices (possibly Teletypes). DMA controllers can usually handle multiple drives. Magnetic tape, disc cartridge, and disc pack controllers handle up to four drives each; the fixed disc controller and plotter controller handle one drive. Most devices attach to either DMA or DIO, but the Nest (process I/O interface) can attach to either.

The Apollo array processor requires both DMA multiplexors, one on each Superbus, and takes up one channel on each.

The CPU, option board, floating-point processor, and memory modules all attach to an internal asynchronous Superbus I that also connects the programmable DIO interface and one DMA multiplexor. The DIO bus can handle one to 16 DIO controllers, and up to eight DMA controllers can be multiplexed. Superbus II, a second bus, can be included in the system together with dual-port memory modules to allow a second DMA multiplexor and up to eight more DMA controllers to be attached. Thus, a maximum of 32 controllers (16 DIO, 16 DMA) can be included in a system.

COMPATIBILITY

The RDS-500 is upward compatible with Raytheon's older 700 series of 16-bit minicomputers. The RDS-500 has new internal architecture which allows better performance, greater flexibility in system size, and greater modularity.

The instruction set is larger on the RDS-500 than on the 704 processor, the most recent of the 700 series. RDS-500 also has more internal general-purpose registers, and its memory capacity has been doubled to a maximum of 64K words. All software used on the 700 series has been adapted to the 500.

Apollo and Nest represent improvements over corresponding 700 series subsystems: the Nest can be retrofitted to a 704, but the Apollo cannot because it requires the dual port attachment.

Eventually, the 500 will supplant the 704. Raytheon plans to continue marketing the 704 as long as there is still a market for it. Although the RDS-500 is more flexible than the 704 and can use all the 704 software, the 704 will be more readily available until the RDS-500 is in full production.

MAINTENANCE AND SUPPORT

Raytheon provides a world-wide maintenance for its systems. It also provides a computer maintenance school in Norwood, Massachusetts, to train customer's employees.

HEADQUARTERS

Raytheon Data Systems Company
1415 Boston-Providence Tpk.
Norwood MA 02062
(617) 762-6700

TYPICAL PRICES

Raytheon Data Systems – RDS 500

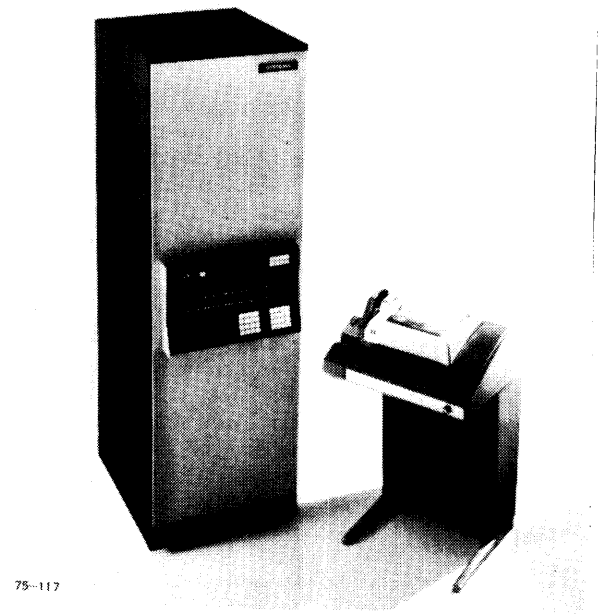
Model Number	Description	Monthly Rental $	Purchase Price $	Monthly Maint. $
51001	Apollo System (includes Apollo array processor with RDS-500 CPU; 2 16K-word multiport memories; floating point processor; extended processor features; and power fail protect)	2,465	57,000	320
51002	Same as 51001 except 4 8K word multiport Memories	2,575	61,000	340
51010	RDS Central Processor System (includes RDS 500 CPU with 2 16K word multiport memories; extended processor features and power fail protect)	560	14,500	488
51011	Same as 51010 except 4 8K word Multiport Memories	650	18,500	567
	Central Processors and Working Storage			
50002	RDS-500 Central Processor (includes high-speed cpu; 8 GP regs; 65K memory; 16 vectored priority interrupts; automatic bootstraps for 4 devices; direct input/output controls; Superbus I and II; operator consoles; printer controller)	205	5,000	30
51201	Floating Point Processor	80	2,000	10
51202	Extended Processor (includes Superbus-I DMA, HS Multiply/Divide, MPS memory protect and memory parity)	35	1,000	5
	PROCESSOR OPTIONS			
51203	Power Fail Protect	25	500	5
51204	Operator Interrupt	5	100	NA
51101	8K words of 800-nsec Multiported Memory	105	3,000	15
51102	16K words of 900-nsec Multiported Memory	160	4,000	30
	Mass Storage			
51801/3	Controller for 51802 Disc Storage Drives or for up to 4 51804s	215	5,000	35
51802	High-speed Fixed Head Disc Drive (385K wd capacity; avg access time 16.7 msec; 180K wds/sec transfer rate)	240	6,000	40
51804	Disc Storage Drive (includes high-speed fixed-head disc drive; 38.5K wd capacity; avg access time 8.33 msec; transfer rate 180K wds/sec)	260	6,500	45
51901	Cartridge Disc Controller for up to 4 51902s or 2 51903s or combination	235	6,000	40
51902	Cartridge Disc Drive (provides removable storage of 1.28M wds/cartridge; cylinder, track and sector format; track transfer rate 80K wds/sec; avg access time 70 msec)	265	5,000	35
51903	Dual Cartridge Disc Drive (with one fixed and one removable cartridge; total storage 2.56M 16-bit wds; cylinder, track, and sector format; transfer rate 80K wds/sec; 70 Msec avg access time)	375	7,500	50
51904	System Disc Cartridge (includes 1.28M wd cartridge with system software)	10	200	NA
51905	Data Storage Disc Cartridge (includes 1.28M wds)	5	125	NA
51951/5	Disc Pack Controller for up to 4 51952s or 4 51956s; includes hardware keysearch feature	400	10,000	70
51952	Disc Pack Drive includes removable storage of 12.9M wds/pack with cylinder, track and sector format; transfer rate of 166K wds/sec; avg access time 32 msec	660	13,000	90
51953/7	System Disc Pack includes 12.9M wd pack and system software; 25.9M wd pack	30	500	NA
51954/8	Data Storage Disc Pack includes 12.9M wd disc pack; 25.9M wd pack	25	325	NA
51956	Same as 51952 except removable storage of 25.9M wds/pack	755	18,000	125
	Input/Output Magnetic Tape			
51401/501/503	Magnetic Tape Controller for up to 4 51402s, 51502s, or 51504s	310	5,500	30
51402	Magnetic Tape Drive Attachment to the 51401 (37.5 ips; 7-track; dual density 556/800 bpi ; IBM compatible)	300	5,300	30
51403/05	Magnetic Tape Controller for up to 4 51404s or 51406s	335	5,500	30
51404	Same as 51402 except attaches to the 51403 (75 ips)	490	8,000	45

TYPICAL PRICES (Contd.)

Model Number	Description	Monthly Rental $	Purchase Price $	Monthly Maint. $
51406	Same as 51404 except attaches to the 51405	550	9,000	50
51490/590	Hardware Chaining	50	1,500	10
51491/591	Extended Cabinet Option (65-in. high cabinet with magnetic tape drive)	5	200	NA
51502	Same as 51402 except attaches to 51501	295	5,300	30
51504	Same as 51502 except attaches to 51503; 75 ips	410	8,000	45
51505	Controller for up to 4 51506s	310	5,500	30
51506	Same as 51504 except vacuum column, for 51506s	425	9,000	50
51509	Same as 51505 for up to 4 51510s	540	12,000	85
51510	Magnetic Tape Drive (vacuum col drive for 51509; 75 ips; 9-track; 800 and 1,600 bpi; IBM and ANSI compatible)	580	14,000	100
51601	Magnetic Tape Controller for up to 2 51602s	715	15,000	105
51602	Magnetic Tape Drive (vacuum col, for 51601; 45/90 ips; 21-track; and 712/356 bpi)	1,870	30,000	210
	Paper Tape			
52001	High-speed Paper Tape Reader; 8-channel; 300 cps	110	2,800	15
52002	Paper Tape Punch and Controller (HS paper tape punch; 8 channel; 110 cps)	175	3,300	20
52003	Paper Tape Reader, Punch, and Controller (HS paper tape rdr/pnch; 300 cps read; 110 cps punch)	260	5,500	30
52004	Paper Tape Reader Spooler (tension for takeup and supply of paper tape with 52001)	90	4,000	25
	Card Punch			
52101	Card Reader and Controller (80-col cards; 300 cpm)	190	4,000	25
52102	Same as 52101 except 1,000 cpm	285	6,500	40
52103	Card Punch and Controller (100 to 400 cpm)	1,400	22,000	130
	Printers			
52201	Printer/Plotter and Controller (11-in. paper; 10.56 in. print/plot line; 1,200 lpm print; 3 ips plot)	555	15,000	85
52202	Same as 52201 except 22-in. paper; 21-in. print/plot line	780	17,300	100
52302	Line Printer and Controller (64-char set, 132 col, 1,250 lpm)	1,685	29,800	175
52303	Same as 52302 except 245 to 1,110 lpm	1,070	17,500	100
52304	Line Printer and Controller (80-col; 64-char set; 356-1,110 lpm)	735	12,000	70
52401	Digital Plotter and Controller (Calcomp 565 Plotter)	550	9,000	50
52402	Digital Plotter and Controller (Calcomp 563 Plotter)	705	11,500	65
52403	Digital Plotter Controller	550	3,500	50
	Teleprinters			
52501	ASR-33 Teletypewriter for use with CPU	80	12,000	5
52502	ASR-35 for use with CPU	255	4,100	25
52503	ASR-33 for use as terminal	80	1,200	5
52504	ASR-35 for use as terminal	255	4,100	25
	A/N Display			
52602	A/N Graphics Display	295	5,400	30
52604	Display Copy unit	255	4,000	25
	Data Communications			
52702	Serial Line Multiplexor for DIO Bus	125	2,500	15
52706	Terminal Controller for DIO Bus	40	1,000	5
52740	Bisync Modem Controller for DIO Bus	165	3,000	15
52801	Programmable Interval Timer for DIO Bus	35	700	5
52802	Time-of-day Clock (resolution is 1 msec)	20	600	5

NA — Not Available

SYSTEMS ENGINEERING LABORATORIES
SEL 32 System Report



OVERVIEW

The SEL 32 is a microprogrammed 32-bit midicomputer designed by the manufacturer of the SEL 86, a 16-bit/32-bit system that has been popular in the process control market. The SEL 32 is a totally new system, but it implements the SEL 86 instruction set; thus, it appears to be an SEL 86 with increased flexibility. The SEL 32 gives the manufacturer a better competitive edge in the general purpose market, as well as in real-time, measurement, and process control, the company's traditional markets. The SEL 32 is extremely modular, currently ranging in size from 32K-bytes to 1,024K bytes of memory; the processor can address up to 16M bytes. Multiprocessor systems can be configured in a number of ways. The main operating system allows real-time foreground/background processing. The overall hardware is versatile and fast enough to be efficient in a wide variety of markets.

Initially, the SEL 32 has two models, which differ only in packaging. The 32/50 is an OEM version without cabinet and power supply; the 32/55 is an end-user system. Both models use the same operating system, software, and peripherals developed for the SEL 86, and both will be marketed for measurement and control applications, SEL's traditional markets.

The SEL 32 is designed around a 32-bit word. It implements 152 instructions. The CPU uses microprogrammed logic, implemented in firmware. Two boards implement the arithmetic logic and one board implements the instruction set. The micrologic uses a 150-nanosecond, single-clocked cycle. The CPU uses a mini pipeline and always has three 32-bit instructions in various stages: while one instruction is being executed, a second instruction is being decoded and a third is being fetched. About 30 percent of the instructions are half-word instructions; thus, the mini pipeline theoretically can store up to six half-word instructions.

All system units communicate with each other via the SEL bus, (which can operate at the rate of 26.67 million bytes per second) in a fashion reminiscent of the PDP-11. The SEL bus, however, is synchronous but allows asynchronous I/O and memory, which interface to the bus via Input/Output Microprocessors (IOMs) and Memory Bus Controllers (MBCs). Unlike the PDP-11, the priority of various system elements attached to the bus are determined by switches on the attached module rather than by the position of the module relative to the CPU. The switches and address lines allow for 23 bus priority levels.

MBCs control banks of up to 512 bytes each, which can be shared between two SEL 32 processors by simply attaching another MBC to the same memory bank. Processors can also be attached via interbus links. These two methods can be combined to make multiprocessor systems that interconnect in a variety of ways.

SYSTEMS Engineering Laboratories is not one of the giants of the minicomputer/midicomputer marketplace, but it has managed to carve out a competitive niche in the measurement and control markets, first with hardwired systems in the early 1960s and later with computerized systems. The company has done particularly well in the custom design of systems for nuclear power plant control. It produced the SEL 810 and 840 (1966), the larger 86 (1969), and the software compatible 85 (1970). All these systems except the 840 are still in production. Although the company has had financial problems, its financial picture has improved substantially this year; outstanding

HEADQUARTERS

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debt was cut in half. The SEL 32 should be successful. It is a powerful but low-cost system. Order backlog reached $4,000,000 in July 1975, with first delivery due in the 3rd quarter 1975. Table 1 lists the mainframe characteristics.

Table 1. SEL 32: Mainframe Specifications

Characteristics	SEL 32
Central Processor	
Microprogrammed	Yes
Control Memory	ROM
No. of Registers	8:3 can be used as index regs
Word Length	32
Addressing	
Direct	To 512K bytes
Indirect	Multilevel to 16M bytes
Indexed	Pre- and post-indexing
Mapping	Yes, to 16M bytes
Instruction Set	
Implementation	Firmware
Types	Half- and full-word
Number	152
Floating point	Firmware std
Hardware Stack	No
Instruction Execution Times (μsec)	
Fixed Point	
Add	1.2
Multiply	4.5
Divide	5.1
Floating-Point	
Add	2.5
Multiply	4.5
Divide	8.9
Writable Control Store (256 56-bit wds)	No
Interrupts	
Levels	128
Type	Hardware
Main Storage	
Type	Core
Cycle Time (μ sec)	0.6
Basic Addressable Unit	Doubleword, word, halfword, byte bit
Bytes/Access	4
Cache Memory	No
Capacity (bytes)	
Min	32,768
Max	1,048, 576
Increment Size (bytes)	32K
Ports/Module	1
Error Checks	Parity; 1 bit/byte
Memory Protection	Yes in pages of 512 words
Memory Management	Yes
Interleaving	2 reads/ 4 writes
Input/Output	
Max Devices Addressable	Via I/O Controllers
Programmed I/O	Yes, IOC
DMA	IOC
DMA Transfer Rate	1.2M bytes/each; 26.7M bytes/sec aggregate; IOC
Software	RTM: Real Time foreground/background system; IBM 2780, IBM 1100 and CDC 200 Emulators FORTRAN IV, Macro; SCORE (standalone system)

COMPETITIVE POSITION

With the introduction of its SEL 32, SYSTEMS Engineering appears to have a robust contender in the real-time, data processing market. SYSTEMS Engineering has floundered in the past by producing new high-performance but incompatible products. The SEL 32 is another matter — it is totally compatible with the SEL 86 in software and performance, and it competes with the top-of-the-line minicomputers in price. Customers are also recognizing its merits with advance orders, so SYSTEMS Engineering now has a substantial backlog. First deliveries are scheduled for third quarter 1975.

Recognizing the competition from top-of-the-line minis in the relatively large-scale, real-time processing market — SYSTEMS Engineering redesigned the SEL 86 using LSI-MSI circuitry to reduce both the amount of hardware and the price. The SEL 32 CPU, for example, is on three large boards instead of the more than 100 small boards in the SEL 86 CPU.

As shown in Table 2, the SEL 32 competes favorably in performance and price when compared to the latest top-of-the-line minicomputers or midicomputers: the Digital PDP-11/70 and the Interdata 8/32. SYSTEMS Engineering appears to have a winner in its traditional, strong markets — measurement and control. Initial orders are primarily from utility companies. The company's experience combined with truly competitive hardware will be hard to beat.

Expanding the sales effort into other markets will be another matter. Currently, the company is more limited in its complement of peripherals and software than Digital Equipment, Data General, Hewlett-Packard, Modular Computer Systems, General Automation, as well as Interdata.

The market is large, however, and success hinges on the ingenuity a company displays in selecting specific products to market.

Configuration Guide

A minimum end-user 32/55 system consists of CPU and SEL Bus with 32K bytes (8K 32-bit words) of memory; the Real Time Option Module (RTOM) with real-time clock and interval timer; floating point firmware; turnkey panel; single equipment cabinet, and 10 SEL bus slots. Packaged submodels of 32/55 differ in base memory size, base memory expansion, and number of bus slots.

Model	Configuration
2202	**32K bytes expandable to 256K bytes, 10 slots**
2204	**32K bytes expandable to 256K bytes, 28 slots**
2206	**288K bytes expandable to 512K bytes, 28 slots**
2210	**544K bytes expandable to 768K bytes, 10 slots**
2212	**544K bytes expandable to 768K bytes, 28 slots**
2214	**800K bytes expandable to 1,024K bytes, 10 slots**

Table 2. Comparison of SEL 32 With Some Competitors

SYSTEM	SEL 32	Interdata 8/32	DEC PDP-11/70	Data General Eclipse S/200
Central Processor				
No. of Registers	8	32; 128 opt	16	4
Addressing				
Word Length	32	32	16*	16
Direct, No. of bytes	512K	1024K	64K	64K
Mapping, No. of bytes	4096K	1024K	2048K	256K
No. of Instructions	152	214	400-446	86-152
Max Devices Addressable	128	1024	No limit	59
Interrupt Levels	128	1024	8	16
Max DMA, rate/SOC	6MB	6MB	4MB (Unibus) 5.8MB (HSDC)	2MB
INSTRUCTION EXECUTION TIMES, μsec				
Fixed-Point Add	1.2	1.1	3.1	0.6
Fixed-Point Multiply	4.5	5.6	5.3	7.2
Fixed-Point Divide	5.1	5.7	9.9	9.6
Floating-Point Add	2.5	2.0	9.9	2.4
Floating-Point Multiply	4.5	3.2	11.9	3.9
Floating-Point Divide	8.9	5.0	12.9	4.6
Main Storage				
Main Memory Core	Core	Core	Core	Core; MOS
Type Cycle Time, μsec	0.6	0.75	1.0	0.8; 0.7
Cache				
Type	None	Stack	Bipolar	Bipolar
Cycle Time, μsec	—	0.24	0.24	0.20
Interleaving	2-way read 4-way write	4-way	2-way	8-way core 4-way MOS
SOFTWARE				
Operating Systems	RTM; real-time & batch system; text editor for time-sharing		IAS, Real-time & timesharing & batch, also RSTX/E, RSX-D	
Compilers/Interpreters	FORTRAN IV, Macro assembler		Macro assembler	
Emulators	None		2780	

*With 32-bit wide bus between High-Speed Data Controllers (HSDC) and memory and between memory and cache

The OEM 32/50 Model is the same as the 2202, except it is in a single chassis without cabinet and power supply.

Systems can be expanded in several ways: 32K-byte memory modules can be added, RTOMs can be added (eight interrupt levels each) and I/O capacity can be increased. Increasing I/O upgrades Models 2202, 2206 and 2210 to Models 2204, 2208, and 2212, respectively. Increasing memory beyond the basic capacity changes Models 2202/2204s into 2206/2208s, then into 2210/2212s, then into 2214s (no Model 2216). Upgrading requires a field upgrade kit.

Each I/O device connects to the SEL bus via Input/Output Microprocessors (IOMs), as shown in Table 3. Two IOMs allow processors to be linked together: the 9122 asynchronous data set interface and the high-speed data interface.

Processors can share access to common data banks via a common memory bus, or SEL busses can be linked together. Memory modules do not directly interface to the SEL bus, but pass through Memory Bank Controllers (MBC). Each supports up to 512K bytes of memory (16 memory modules). By interfacing two MBCs to a common memory bus but to different SEL busses, two processors can share the same memory bank, even if the SEL busses are not linked together. Thus, multiprocessor systems can be configured with linked SEL busses or with shared memory banks or with both, and a single system can be linked with several other systems in different ways. This highly modular concept allows considerable flexibility in multiprocessor configurations, and control of specific peripherals can be distributed, each assigned to specific CPU.

Software packages, of course, make their own configuration demands. The basic standard software packages are listed in Table 4, together with brief descriptions and, wherever appropriate, configuration requirements. In addition to those listed, SEL offers "tailored" systems based on adaptions of other standard packages designed for this purpose, particularly in process control, timesharing and communications.

Table 3. SEL 32: Peripherals

Model Number Console	Performance Characteristics
9201 KSR 33 Teletypewriter	10 cps
Cards	
9210/9211 Card Readers	285/1,000 cpm
9215 Data Recorder	200 cpm reader, 45-75 cpm punch; keyboard
9216 Data Recorder	Interpreting version of 9215
9217 Card Reader/Punch	200 cpm reader, 45-75 cpm punch
9218 Card Reader/Punch	Printing version of 9217
9219 Card Punch	100 cpm
Printers	
9224 Serial Printer	100 char/sec; 132 columns
9225/9226 Line Printers	300/600 lpm; 136 columns
Discs	
9306 Moving Head Disc	5 MB/cartridge; 4 drives/controller
9308 Moving Head Disc	10 MB/cartridge; 4 drives/controller
9320 Moving Head Disc	80 MB/pack; 4 drives/controller
9335 Fixed Head Disc	1 MB/disc, 4 drives/controller
9336 Fixed Head Disc	2 MB/disc, 4 drives/controller
Magnetic Tape	
9360 Mag Tape Drive	7-track; 556/800 bpi, 45 ips; 4 drives/controller
9361 Mag Tape Drive	9-track; 800 bpi; 45 ips, 4 drives/controller
9362 Mag Tape Drive	9-track; 1,600 bpi; 45 ips; 4 drives/controller
9363 Mag Tape Drive	9-track; 800/1,600 bpi; 45 ips; 4 drives/controller
9374 Mag Tape Drive	7-track; 556/800 bpi; 75 ips; 4 drives/controller
9375 Mag Tape Drive	9-track; 800 bpi; 75 ips; 4 drives/controller
9376 Mag Tape Drive	9-track; 1,600 bpi; 75 ips; 4 drives/controller
9377 Mag Tape Drive	9-track; 800/1,600 bpi; 75 ips; 4 drives/controller
Communications	
9122 Async Interface	Programmable, 4 channels; can link 2 busses
9124 Sync Interface	Programmable, 4 channels
9126 MUX	To 128 lines
Special	
9142 Analog/Digital	6 types of subsystems
9162 General I/O	Blank IDM, no device logic
9132 High Speed Data Interface	Can serve as interbus link, or link to special devices
9134 Serial Data Interface	For attaching special devices

Compatibility

The SEL 32 is completely hardware and software compatible with the SEL 86. Programs can be run without alteration, and Model 86 peripheral devices can be attached. A new 800/32 translator also allows SEL 800 series programs to be translated into SEL 32 programs.

Table 4. SEL 32: Software

Package	Description
Real Time Monitor (RTM)	Disc-oriented multiprogramming foreground/background system; requires CPU, 128K bytes of memory RTOM option, KSR-33 console, card reader or reader/punch, printer, at least 2MB disc, mag tape
SCORE	Minimum system for program development or small applications; requires 32K bytes memory without assembler or 64K bytes with assembler, plus one input and one output device
FORTRAN IV	ANSI standard with extensions for real-time multiprogramming, runs under RTM as std feature, so no extra memory required
Macro Assembler	Assembler for RTM, with unlimited resting and recursion of macro structures; runs under RTM as standard feature, so no extra memory required; extra 32K needed for SCORE
Utilities	Mathematical subroutine library; FORTRAN support library, scientific subroutine library, and three diagnostic packages

Emulators allow the SEL 32 to "look like" an IBM 2780, an IBM 1100, and a CDC UT 200.

MAINTENANCE

SYSTEMS Engineering Laboratories has 14 U.S. sales and service offices, in addition to corporate headquarters in Florida. The company also has offices in Canada, France and Germany.

The standard maintenance contract is prime shift — on call service. Travel charges are added if the installation is more than 25 miles from the service area, or for after-hour service.

SYSTEMS Engineering does not lease its systems.

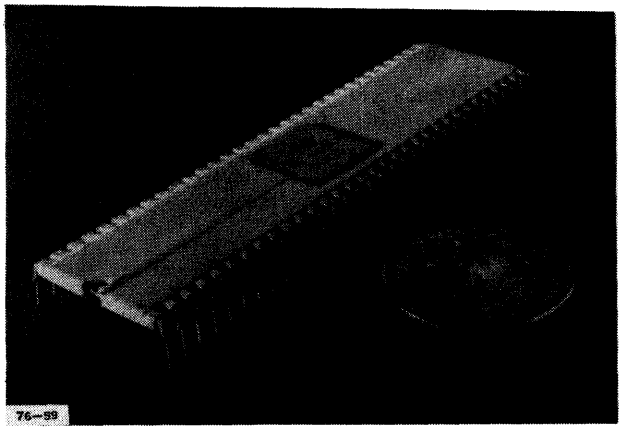
TYPICAL PRICES

Model Number	Description	Purchase Price $	Monthly Maint. $
	Central Processor and Working Storage		
2202	SEL 32/55 with 32K Bytes memory	25,000	225
2204	Same as 2202 with 28 Slots	27,000	240
2206	Same as 2202 except 288K bytes core memory expandable to 512K bytes	78,000	730
2208	Same as 2206 with double equipment cabinet and 28 SEL bus slots	81,000	745
2210	Same as 2202 except 544K bytes core memory expandable to 768K bytes; double equipment cabinet	138,000	1,260
2212	Same as 2210 with 28 SEL bus slots	140,000	1,275
2214	Same as 2210 except with 800K bytes of core memory expandable to 1,024K bytes	191,000	1,765
2200	Same as 2202 except 32K bytes of core memory, single chassis without cabinet and power supply and 4 bus slots	18,000	200
2201	Same as 2200 except double chassis, 256K bytes of core and 10 bus slots	21,450	185
	Processor Options		
2230	Dual Processor Integrator	**	**
2112	Real-time Option module	2,500	20
2142	System Control Panel	3,000	25
2145	Hexidecimal Display	600	5
2149	Over 512K Bytes Addressing Option	3,000	NC
2150	Memory Bus Controller	3,000	25
2152	32K Byte Memory Modules	6,300	60
2179	Memory Interface Adapter	3,000	25
2181	Logic Chassis	1,000	NC
2182	Memory Chassis provides slots for up to 8 memory modules and up to 2 MBC's	1,000	NC
2188	Maintenance Panel (test panel for accessing and displaying microprogram steps)	5,000	NC
2199	Bay Extender	300	—
2221/22	Input-Output Upgrade	**	**
2223/4/5/6	Memory Upgrade	**	**
	Mass Storage		
	Disc		
9008	Cartridge Disc Controller	3,000	25
9010	Moving Head Disc Controller	5,000	45
9301	Cartridge Disc Formatter	2,700	20
9306	Cartridge Disc Drive (5M bytes; 312K byte transfer rate)	6,000	75
9308	Cartridge Disc Drive (10M bytes; 312K byte transfer rate)	7,500	25
9320	Moving Head Disc Drive (80M bytes; 1.2M bytes transfer rate)	25,000	75
9321	Moving Head Disc Drive (40M Bytes; 1.2M bytes/sec transfer rate; 30M sec average access time)	18,000	165
9335	Fixed Head Disc Drive (1M Byte; 4.4M Hz; 8.5-msec average access time)	14,000	140
9336	Fixed Head Disc Drive (2M Bytes)	20,000	200
9014	Fixed Head Disc Controller	5,000	45
	Input-Output		
	Interfaces		
9102	General-Purpose I/O Module	2,500	25
9104	GP Multiplexor Controller	3,500	30
9122	Async Data Set Interface	3,000	30
9124	Sync Data Set Interface	3,500	30
9126	Communications Subsystem interface	3,500	30
9132	High Speed Data Interface	4,000	30
9134	Serial Data Interface	4,000	35
9136	Inter-Bus Link	6,000	50
	Teleprinters		
9201	KSR-33 Teletypewriter	1,600	25
	Punched Card		
9210	Card reader (285 cpm)	3,000	55
9211	Card reader (1,000 cpm)	6,000	95
9004	TLC Controller	2,500	25
9006	Card Punch Controller (requires 2 slots)	3,000	25
9215	Data Recorder (card reader-punch; 200/45-75 cpm with keyboard)	14,500	200
9216	Interpreting Data Recorder (card reader/punch/printer; 200/45-75 cpm with keyboard)	16,500	200
9217	Card Reader/Punch (card reader; 200 cpm; punch 45-75 cpm)	12,500	200
9218	Printing Card Reader/Punch (200 cpm; punch/printer 45-75 cpm)	14,500	200
9219	Card Punch (100 cpm, 80 col)	20,000	200
	Printers		
9220	Serial Printer (100 cps; 132 cols)	4,000	40
9225	Line Printer (125 lpm; 132 cpl)	5,800	85
9225	Line Printer (300 lpm; 136 cols)	10,000	95
9226	Line Printer (600 lpm; 136 cols)	16,000	200
	Magnetic Tape		
9350	Tape Formatter (7- 9-track NRZI, supports up to 4 transports)	2,000	15
9351	Tape Formatter (9-track, PE; supports up to 4 transports)	3,000	24
9352	Tape Formatter (9-track, NRZI/PE; supports up to 4 transports)	4,000	30
9360	Magnetic Tape Transport (tension arm; 45 ips; 7-track; 556/800 bpi; NRZI, 10-1/2 in. reel)	5,000	75
9361	Same as 9360 except 9-track, 800 bpi	5,500	75
9362	Magnetic Tape Transport (tension arm; 45 ips, 9-track, 1,600 bpi; PE; 10-1/2 in. reel)	8,000	75
9363	Magnetic Tape Transport (tension arm; 45 ips; 9-track; 800/1,600 bpi; NRZI/PE 10-1/2 in. reel)	9,000	80
9374	Magnetic Tape Transport (Vacuum Col; 75 ips; 7-track; 556/800 bpi; NRZI, 10-1/2 in. reel)	14,000	90
9375	Magnetic Tape Transport (Vacuum Col; 75 ips; 9-track; 800 bpi; PE; 10-1/2 in. reel)	15,000	90
9376	Same as 9375 except 1,600 bpi	16,000	90
9377	Same as 9375 except 800/1,600 bpi; NRZI/PE	17,000	100
9012	Magnetic Tape Controller (interfaces to 1 formatter with up to 4 transports requires two bus slots)	3,000	25
9399	Peripheral Cabinet	1,000	NC
	Software		
1001	Real-Time Monitor		
	Binary	1,500	
	Source	2,500	
1021	Standalone Software System		
	Binary	0	
	Source	250	
1011	Macro Assembler		
	Binary	0	
	Source	1,500	
1012	FORTRAN IV Compiler		
	Binary	800	
	Source	2,500	

Notes:

* Home Office Quote
** Price depends on configuration; available on request from SEL
— Not Applicable
NC No Charge

TEXAS INSTRUMENTS
990/9900 Family System Report



OVERVIEW

The Texas Instruments 990/9900 family is a new 16-bit line extending upwards from the 16-bit TM 9900 n-MOS microprocessor chip, to the 990/4 computer-on-a-board, up to the 990/10 systems that can map as many as two million bytes of memory. Initially, the system is aimed chiefly at the OEM market, that is, at the low end of the market; but it is by no means restricted to OEMs. This is the line Texas Instruments plans to use as the base of a concerted attack on the whole range of the micro/minicomputer markets, an attack surprisingly long overdue from one of the leaders of the semiconductor industry. Its announcement is spectacular for two reasons: The TMS 9900 is the first 16-bit, single-chip microprocessor from a major semiconductor company; and the 990 line marks Texas Instrument's first really aggressive step toward becoming a major contender in the minicomputer industry.

Although the 990 line is brand new, its architecture is not. Besides the 980 and 960 lines introduced to the public at large and developed slowly in the early 1970s, Texas Instruments had developed a precursor to the 990 for a special, large contract with Ramada Inns. The system design was oriented toward communications and distributed processing, and for that contract, it was implemented in TTL logic using medium- and large-scale integrated circuitry. The result was admirable but expensive by today's standards. When Texas Instruments began designing the microprocessor chip that was to be the basis of the new line, the 990 architecture appeared best suited to the way the market was heading. Thus, although the 990 seems to be totally new and incompatible with Texas Instruments' previous offerings, its design has actually been field tested over a respectable period of time in a TTL version.

The TMS 9900 microprocessor is the foundation of the line. It is implemented on a single 16-bit MOS chip using n-channel silicon-gate technology and a 3-megahertz clock frequency. It is not a microprogrammed chip, but it includes all of the logic for its versatile 69-instruction repertoire on its own real estate. To add flexibility, an extended-operation instruction allows 16 more instructions to be defined in external hardware or software. Also included on the chip are a vectored interrupt facility; separate data and address buses; a Communications Register Unit (CRU) I/O interface; a Direct Memory Access (DMA) interface; hardware context switching; hardware multiply/divide; bit, byte, and word addressing; and 5-mode addressing capable of handling up to 64K bytes, all in a 64-pin DIP package.

The 990/4 microcomputer puts together on a single board the TMS 9900 microprocessor, the CRU and DMA buses, up to eight priority interrupts, powerfail/auto restart logic, a CRU interface for operator or programmer panel, and up to 4K words (8K bytes) of memory. Memory can be RAM, ROM, PROM, or EROM (erasable ROM) modules of various sizes, depending on the type. The 990/4 can also be packaged in a 6-slot tabletop chassis with front panel. Either way, the system can control up to 28K words (56K bytes) of memory. A 733 ASR Data Terminal is supplied with software support, in system packages. Texas Instruments does not implement DMA, however; all mass storage devices interface to the 990/10 TILINE.

The 990/10 is a 3-board TTL version of the TMS 9900 (two boards for CPU, one or more for memory), with mapping of up to two million bytes of memory and a special asynchronous high-speed channel, the TILINE. The 990/10 is a full-blown, high-speed minicomputer system, with supporting disc-based operating systems, high-level languages, and so on. Although current peripherals are relatively low-speed and the discs are in the low storage capacity range, the high memory capacity, high-speed universal bus and rapid context switching are capabilities that will surely be needed for future devices.

Peripherals for the 990 series support the initial marketing thrust toward the low end of the market. An important

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peripheral is Texas Instrument's own "Silent 700" KSR and ASR terminals, using cassettes instead of paper tape. Floppy disc, 400 card-per-minute card readers; 88 and 120-character-per-second impact printers; and (with a subsystem) 1.5-million-byte cartridge discs provide standard I/O. Asynchronous and synchronous 1-line interfaces allow transmissions up to 9,600 baud. Two important special peripheral interfaces allow PROM/EROM writing and attachment of custom 16-bit I/O lines. The 16-bit interface allows handling each line separately; one line can be marked an interrupt line.

For a totally new system, the software is extensive. The DX-10 operating system is a multitasking, mapped, disc-based system that supports FORTRAN IV, COBOL, and multiuser Dartmouth BASIC. The cassette-based Terminal Executive TX-990 Operating System is a multitasking system for 990 configurations with up to 32K words of memory. Various smaller support packages are available, including a 990 Prototyping System for encoding PROM/EROM TMS 9900 programs as 990/4 and TMS 9900 software development. A cross assembler allows development of 990 programs on an IBM 360/370 or time-sharing network.

One of the strong points of the entire line is its low cost, which is expected from a major semiconductor manufacturer coming out with a microprocessor and semiconductor memory modules made in-house. TMS 9900 microprocessors with 256 words (512 bytes) of memory are sold in quantities of 50 for $368 each. The 990/4 board-level system costs only $575 with 512 bytes of memory and $800 with 8K bytes of memory. Adding a 6-slot chassis, power supply, and programmer's console raises the price to $1,900. A 990/10 system with 16K bytes of memory, 13-slot chassis, power supply, and programmer's panel costs $1,975; raising the memory size to 40K bytes increases the price to $3,075. Add-on 40K-byte memory boards cost $2,500 each.

The 990/10 was delivered in March and the 990/4 in April 1976.

Table 1 lists system specifications.

Table 1. TI 990; Mainframe Specifications

CENTRAL PROCESSOR	
Microprogrammed	No (extended operation instruction instead)
Stack Processing/Context Switching	Yes ("workspace registers")
No. of Programmable Registers	16
No. of Instructions	
Std	69
Opt	72
Instruction Execution Times (μ sec)	
Fixed-Point Add/Subtract	4.662 (990/4); 1.166 (990/10)
Multiply	17.316 (990/4); 11.9-16.2 (990/10)
Divide	5.328 (990/4); 5.4-8.7 (990/10)
Move	4.66 (990/4); 3.60 (990/10)
Floating Add/Subtract	Subroutine
Addressing	
Direct (no. of wds)	32K
Indirect	Yes, 1 level
Indexed	Yes
Mapped	Yes
Priority Interrupt Levels	16
MEMORY	
Cache	No
Types	MOS RAM; ROM; PROM; EROM
Word Length (bits)	16
Cycle Time/Word (μ sec)	667 (MOS RAM, PROM)
Capacity, words	
Min	8K (990/10); 256 (990/4)
Increments	4K, 8K, 16K, 24K, 32K MOS RAM; 1K EROM; 256 PROM
Max, without Mapping	32K (64K bytes)
Max, with Mapping	1M (2M bytes)
Checking	Parity, error correcting options
Protection	Option
INPUT/OUTPUT	
Max No. of Devices	4,096 CRU; 512 TILINE
Programmed I/O Channel	CRU
Multiplexed I/O Channel	TILINE universal bus on 990/10
Direct Memory Access (no. of channels)	Not supported, but available on 990/4
Max Transfer Rate (words/sec)	
Within Memory	—
Over DMA	3M

PERFORMANCE AND COMPETITIVE POSITION

By all accounts, Texas Instruments ought to make rapid inroads into the microprocessor/minicomputer markets, if it makes a reasonably serious attempt to penetrate them. It is a large company with a fine reputation in the semiconductor industry, which supplies computer manufacturers with many of their parts. Yet the firm's initial attempts at market penetration, in the form of the 960 and 980 lines were less successful than many anticipated, in spite of excellent system engineering. This is usually attributed to apathetic marketing and support efforts and partly to the specialized orientation of those computers toward machine and process control applications.

The 990 series differs from its predecessors in range of system sizes, which covers the gamut of the existing market. Also, the architectural orientation is towards communications and distributed processing. This line of systems could move Texas Instruments (TI) from a relatively minor position to one of importance. Whether the system lives up to expectations will depend on its software development, and on the energy and imagination of TI's marketing efforts. The company's marketing track record has not been very good, so that area could be a potential weakness. Of course, it is possible that TI intentionally delayed a vigorous entry into the market while the major line was under development.

In any event, TI faces stiff competition at all levels. Its major competitors in the OEM marketplace, fall into two categories. Digital Equipment, General Automation, and Computer Automation compete for the 990/4 board-level systems markets (see Table 2). Digital, Data General,

General Automation and to some extent the Hewlett-Packard 21MX compete at the 990/10 level (see Table 3). As shown in the tables, the TI systems undercut the prices of all the other systems without exception by 15 to 50 percent at the 990/4 level and to a greater extent at the 990/10 level. The DMA rate is potentially the highest available, but that is offset by the facts that more software exists for the competing systems and there are often more built-in features, especially on the larger systems. Nevertheless, the cost difference is clearly significant and is a powerful factor in TI's favor.

At the beginning of 1976, orders were already backlogged for deliveries into May. The significant price break at a time when the OEM market is on the upswing out of a recession may be a tide that will rapidly carry TI to a position of prominence.

CONFIGURATION GUIDE

The initial marketing thrust of the 990 line is toward the OEM market, and the system configurations emphasize modularity. All three models can be sold with or without chassis, power supply, and programmer's panel. All three have submodels coupling them with various sizes and types of memory. The basic 990/4, for instance, can be configured with 256 words of static RAM, 4K words of dynamic RAM with or without parity, or a self-testing feature. ROM loaders, PROM kits, and EPROMs, as well as 4K-, 8K-, 12K-, 16K-, or 20K-word single-board MOS memory modules, can be added to basic systems. Core memory is unavailable. The system can be housed in a 6-slot tabletop chassis or a 13-slot tabletop or rack-mounted chassis.

Basic 990/10 systems use the same options and memory expansion modules as the 990/4; but all are based on a 2-board TTL CPU with 8K-, 12K-, 16K-, or 20K-word memories in the basic systems. It is usually housed in a 13-slot chassis with attendant power and programmer's panel. A second series of basic systems is configured with memory mapping. The 990/10 is also available with a group of memory modules that have error-correcting circuitry (ECC). A special (standard) universal bus extension called the TILINE bus interface provides for adding extra memory and high-speed peripheral DMA devices. TILINE mapping provides one million addresses, and is a basis for the extra memory capabilities of the 990/10.

The 990/4 and 990/10 are available in several system packages. The 990/4 Prototyping System packages for development of application programs for the TMS 9900 and 990/4 board-level systems consist of CPU, chassis, power supply, programmer panel, self-testing, memory expansion with parity and write protect, 8K to 24K words of memory, and optionally a 733 ASR terminal, a ROM loader, and a PROM programming module. The 990/4 Program Development Systems are essentially the same except that the 733 terminal and ROM loader are standard items, but the PROM programming module is not supported.

The 990/10 Program Development System is designed to support the DX-10 Operating System. It includes the DS31 disc with its associated ROM loader and the 913A CRT as well as the 990/10 CPU and a 13-slot chassis. Although all peripherals can be attached to either the 990/4 or the 990/10 systems, only the 733 terminals, the PROM kits, and the communications interfaces are software-supported on the 990/4. The CRU can interface to 4,096 devices. The TMS 9900 DMA facility consists of a single line, but the 990/10 asynchronous TILINE bus can support up to 512 high-speed controllers and 1,024K words of memory. Peripheral devices are listed in Table 4.

Table 2. TI 990/4: Specifications Compared with Those of Competitors

	TI 990/4	Computer Automation LSI-3/05	GA-16/110	GA-16/220	Digital LSI-11
Word Length (bits)	16/16 + 1 parity	16	16/16 + 2 parity/ 16 + 6 EDR	16/16 + 2 parity/ 16 + 6 EDR	16
Instruction Times (μsec)					
Add	8.7	6.0	2.5	2.5	3.5-12.0
Multiply	21.3	No	21.0	21.0	24-64
Divide	9.3	No	20.0	20.0	78
Fl. Pt. Add	No	No	Opt	Opt	42.0
Fl. Pt. Multiply	No	No	Opt	Opt	52-92
Fl. Pt. Divide	No	No	Opt	Opt	151
Max Memory (bytes)	56K	32K	128K	128K	64K
No. of G.P. Registers	16	8	16	16	8
Max DMA Rate (bytes/sec)	DMA not supported	1.7M	2M	2M	1.7M
Price ($)					
CPU + Memory					
8K Bytes	800	1,145	1,185	1,575	1,536
32K Bytes	2,300	2,650	3,045	3,435	3,411
64K Bytes	—	—	5,525	5,915	5,911
128K Bytes	—	—	10,485	10,875	—

Table 3. TI 990/10: Specifications Compared with Those of Competitors

	TI 990/10	Data General Nova 3	GA-16/330	GA-16/440	HP 21MX	Digital PDP-11/45[2]
Word Length (bits)	16/16 + 1 parity/16 + 2 ECC	16	16/16 + 2 parity	16/16 + 2 parity	16	16/16 + 2 parity
Instruction Times (μsec)						
Add	3.1	1.8	4.6	0.8	1.9	1.8
Multiply	13.9-18.2	6.9[1]	21.2	11.1	12.8	4.7
Divide	7.4-10.6	7.5[1]	20.3	12.8	17.0	8.6
Fl. Pt. Add	No	7.7*	*	3.1-4.7*	22-54*	6.5*
Fl. Pt. Multiply	No	11.3*	*	4.8-7.9*	48-57*	8.2*
Fl. Pt. Divide	No	13.7*	*	7.6-8.7*	41-76*	9.9*
Max Memory (bytes)	2M	64K/256K	128K	2M	512K	253, 952
No. of G.P. Registers	16	4	16	16	4	16
Max DMA Rate (bytes/sec)	6M	2M	2M	2M	1.2M	2M
Price ($)						
CPU + Memory						
32K Bytes	2,975	4,400	5,250	11,800	7,650	23,900
64K Bytes	4,975	7,100	8,250	15,150	11,800	32,000
256K Bytes	17,900	34,200	—	38,750	36,150	55,500[3]
512K Bytes	33,900	—	—	71,850	—	—

*Optional, at extra cost.
Notes:
(1) Operands are unsigned integers on std.
(2) Core memory assumed, the PDP-11/45 can use faster MOS or bipolar.
(3) Maximum memory is 253,952 bytes.

TI can supply from 4K to 20K words of MOS memory on a single board. TMS 9900 and 990/4 systems can control up to 28K words (56K bytes) of memory. Thus a maximum 990/4 needs two additional memory boards but a 24K-word system requires only one if 4K words are on the processor board. The 990/10 has all memory on separate boards, and it can control up to 32K words without mapping or 1,024K words with mapping

Table 4. TI 990: Peripherals

Model No.	Description
LOW SPEED	
600/601	733 KSR/ASR Silent 700 Data Terminals (30 cps; 1,200 baud)
620	913A Video Display (960 char)
670	120-cps Dot Matrix Printer
677/679	Model 588 "Line" Printer (88 cps; dot matrix)
686	804 Card Reader (400 cpm)
MASS STORAGE	
650	Floppy Disc (242K wd/diskette)
655	Removable Cartridge Disc (1.55M wd/disc; 4 drives/subsystem)
656	Fixed Cartridge Disc (1.55M wd/disc; 4 drives/subsystem)
COMMUNICATIONS	
631/633	Asynchronous (to 9,600 baud)
636	Synchronous
630/632	Asynchronous
634/635	Auto Calling Kits
638	Synchronous Modem (to 2,400 baud)
MISCELLANEOUS	
690	Universal PROM Programming Kit
695	16 I/O EIA Data Module
696	16 I/O TTL Data Module

Table 5 lists the various software packages and their memory and peripheral requirements.

COMPATIBILITY

The TMS 9900, 990/4, and 990/10 processors use the same basic instruction set with expansions at the 990/10 level. With a few restrictions both hardware and software are upward compatible in the product line. The prototype system software is not compatible with the 990/10 because the software utilizes the 990/4 write protect feature.

Central programs and software modules are upward compatible. Programs written to run under the PX9MTR Prototyping System Software, for example, will also run under TX-990 and DX-10 operating systems. Conversely, programs for the PX9MTR can be created on TX-990 or DX-10 if the user is careful to limit facilities to those available to PX9MTR.

The 990 hardware and software are *not* compatible with any other series of computers, including TI's own 960 and 980 systems. The peripherals for the 990 have different interfaces than those used for the 960 and 980 computer lines, and the 990 software is entirely new.

MAINTENANCE

Texas Instruments provides three types of contract maintenance for purchased systems: basic coverage, standard, and full.

Table 5. TI 990: Software

Package	Description
Prototype System	Resident monitor, assembler, and utilities for application prototyping and PROM memory development for the 990/4 and TMS 9900; requires 990/4, 733 ASR, 8K RAM, 735 ROM programmer front panel, power supply, and chassis; supports up to 28K words of memory and PROM programming module; cannot be used with 990/10
990-733 ASR System Software	For software development on 990 with 733 ASR terminal; includes monitor, assembler, utilities; requires 990/4, 733 ASR; 8K RAM; 733 ROM programmer front panel, power supply, chassis packaging; supports up to 32K words of memory
990/10 Disc System Software	For disc-based software development; includes DX-10 Operating System, Auto-Sysgen, Macro Assembler, 913 editor, link editor, Delong Librarian, card loader (on cassette); requires 990/10, 24 words of memory, ROM, 733 ASR; 913A CRT; DS31 Disc, programmer front panel; supports up to 1M words, card reader, line printers, CRTs, floppy disc, added disc
FORTRAN IV	ANSI X3.9-1966 with ANSI clarifications and ISA recommended extensions; including IBM FORTRAN-compatible direct access I/O; requires DX-10 and 32K words of memory
COBOL	ANSI COBOL subset = Level 1 nucleus plus table handling and sequential I/O as defined in ANSI X3.23-1975, with extensions; requires DX-10 and 32K words of memory
Multiuser Basic	Dartmouth Basic equivalent for up to 8 concurrent users; requires DX-10 and 32K words of memory
Asynchronous Communications	Supports async communications to 9,600 baud; auto answer, auto call, error checking; requires 990/4 or 990/10, 2.5K words of memory, and TX-990 or DX-10 async or Bell dataset interface
Synchronous Communications	Supports sync communications to 9,600 baud; auto call, auto answer, error checking; requires 990/4 or 990/10, TX-900 or DX-10, 2.5K words of memory, access to 990/10 disc
IBM S/3xO Cross Support	Cross assembler plus a TMS 9900 simulator 2-pass assembler for System/360 and 370; requires 200K bytes under OS

Basic coverage provides for prime-shift preventive and emergency maintenance Monday through Friday for any 9 consecutive hours between 7 a.m. and 6 p.m. at the user's site. Standard coverage provides preventive and emergency service at the user's site for 16 consecutive hours between 7 a.m. and 1 a.m., Monday through Friday. Full coverage provides for on-site emergency and preventive service around the clock, 7 days a week.

In addition to these contracts, TI provides service on an on-call basis for users without a contract or outside of contracted hours, with the fee depending on whether equipment is delivered to a repair depot or is repaired on-site during the prime shift or outside the prime shift or on Sundays and holidays.

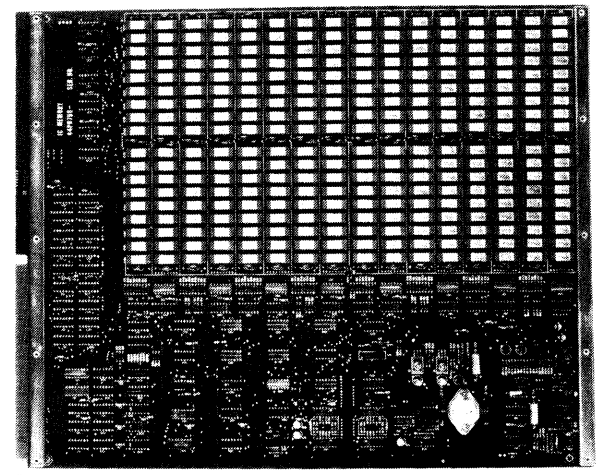
TYPICAL PRICES

Equipment	Purchase Price $
Systems	
990/4 CPU with 256 Wds of RAM	575
990/4 CPU with 4K Wds of RAM	800
990/4 and 990/10 Memory Expansion Modules	
4K Wds	625
8K Wds	1,000
12K Wds	1,500
16K Wds	2,000
20K Wds	2,500
Write Protect	50
Parity Option	
4K Wds	50
Each Additional 4K Wds	25
990/10 CPU with Memory	
8K Wds	1,975
12K Wds	2,475
16K Wds	2,975
20K Wds	3,475
990/10 CPU with Mapping and Memory	
8K Wds	2,900
12K Wds	3,400
16K Wds	3,900
20K Wds	4,400
990/10 CPU and ECC Memory	
8K Wds	2,925
990/10 CPU with Mapping and ECC Memory	
8K Wds	3,850
990/10 Memory Expansion Modules with ECC	
8K Wds	1,950
8K Wds Add-on	1,400
16K Wds Add-on	2,800
24K Wds Add-on	4,200
990 Prototyping or Program Development Systems with 733 ASR and Memory	
8K Wds	5,950
12K Wds	6,300
16K Wds	6,750
20K Wds	7,225
24K Wds	7,700
990/10 Program Development System with 733 ASR and Memory	
8K Wds	519
990/4 and 990/10 PACKAGING OPTIONS	
3-Slot OEM Chassis without Power Supply (990/4 only)	175
6-Slot Chassis with Operator Panel and 5V, 20A Power Supply	950
6-Slot Chassis with Programmer Panel and 5V, 20A Power Supply	1,100
13-Slot Chassis with Operator Front Panel and 5V, 40A Power Supply	1,400
13-Slot Chassis with Programmer Front Panel and 5V, 40A Power Supply	1,550
Tabletop Chassis Option	150
Standby Power Supply	350
I/O EXPANSION OPTIONS	
CRU Expansion Kit	525
TILINE Expansion Kit	1,200
TERMINAL OPTIONS	
Model 733 KSR Data Terminal Kit	1,975
Model 733 ASR Data Terminal Kit	3,575
TTY/EIA Interface Module	375
Model 913A Video Display Terminal Kit	2,000

TYPICAL PRICES (Contd.)

Equipment	Purchase Price $
DISC STORAGE	
990 Floppy Disc Kit	2,950
Secondary Floppy Disc Unit	1,100
990 Floppy Disc Expansion	750
Model DS31 Disc Master Kit (removable)	9,650
Model DS32 Disc Master Kit (nonremovable)	7,050
Model DS31 Disc Secondary Kit	6,600
DS31 Secondary Kit with Power Supply	7,300
Model DS32 Disc Secondary Kit	4,000
DS32 Secondary Kit with Power Supply	4,700

VARIAN DATA MACHINES
V76 Computer System Report



OVERVIEW

The big story with Varian's newest member of the V70 Series is price. The V76 costs 38 percent of the price of the earlier V75 computer with 128K bytes of memory; $18,950 for V76 versus $46,500 for V75. The difference in price is totally due to a new n-channel MOS memory developed specifically for the V76. The V76 uses the same processor as the V75, which in turn is the V73 processor with three chips added to implement an extended instruction set. The V75 was the first of the V70 computers to implement instructions to use eight general-purpose registers and to perform byte and double-precision operations.

Varian uses a large memory board and packs 32K or 64K words per board. Words are 16 bits long. A parity option adds one bit per word. Cycle time is 660 nanoseconds per word; access time is 550 nanoseconds. Maximum memory capacity is 256K bit words.

The memory is made up of 4K RAM chips housed in a 16-pin, dual-in-line package. The memory chips are currently supplied by Mostek, but plans call for both National Semiconductor, and Fairchild to supply them also. Varian optimistically offers its memory boards without parity, as well as with parity.

The Varian press announcement stated that the new memory will be compatible with 16K RAM chips when they become available, allowing 128K words or 256K words to be stored on each memory board. This implies that future V76 memory capacity will be 1M words.

The new memory is low in power consumption. This feature, combined with the dense packaging, allows either of the two mainframe chassis offered to house up to 256K words of memory with slots left over for options or peripheral device controllers.

One mainframe chassis is 7 inches high and has five P (for peripheral controller or memory module) slots. The other mainframe chassis is 14 inches high and includes 15 P slots.

The power supply for the CPU and memory is housed separately and requires 5-1/4 inches. A second power supply is required for CPU options, writable control store, memory map, and floating point. A Data Save Power Supply with battery is offered to maintain memory power in case of a main line power failure; it will maintain power to 64K words for four hours and to 256K words for 45 minutes.

Expansion chassis are available to add 22 I/O slots per chassis. Expansion chassis require additional power supplies and I/O party line expanders.

Like other members of the V70 Series, the V76 can implement memory mapping to 512K bytes, and 512 words of 64-bit writable control store (WCS). WCS can be used to implement floating point firmware, Fast FORTRAN firmware, decimal arithmetic, or user-coded firmware.

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The V76 is totally upward compatible with the other members of the V70 Series; thus, it supports all the software and peripherals currently available.

The V76 is available like the V73 from a shopping list of components; thus, systems can be configured quite precisely, see Price Data. First deliveries of the V76 are scheduled for the first quarter of 1976.

COMPETITIVE POSITION

The V70 Series of computers generally competes in the middle range of the minicomputer market. According to trade papers, Dr. Donal B. Duncan, president of Varian Data Machines, promised two new compatible computers for delivery in 1976: one at the bottom of the V70 Series and one at the top. In this context, the V76 must be classified as the top system of the line.

Table 1 compares the V76 with some competitors also in midrange: Data General Nova 3, General Automation GA-16/330, Digital PDP-11/45, and Hewlett-Packard HP 21MX. The V76 is not very price competitive for small systems; the smallest memory size is 64K bytes, and Nova 3, GA-16/330, and HP 21MX are all less expensive for 64K-byte systems. For 256K-byte systems, however, the V76 costs substantially less than the Nova 3 and HP 21MX. In all ranges, the V76 costs much less than the PDP-11/45. The GA-16/330 is unavailable with 256K-byte memory.

The software available for the V76 makes it a very competitive system for the top end of the minicomputer market.

Varian's recent marketing orientation has been toward making the software industry-compatible: COBOL, RPG II, and IBM level G FORTRAN compilers, and the TOTAL data base management system have all been introduced within the last eight months. The company's VORTEX II operating system has long been a big plus for the V70 Series.

Varian has wisely chosen to implement memory using dual-port modules. With the priority memory access (PMA) option, I/O throughput can reach 6M bytes per second.

The hardware and software features make the V76 performance competitive with the PDP-11/70 at less than one-half the price; see Table 2. The V76 is somewhat slower than the 11/70 for both fixed-point and floating-point arithmetic.

The V76 adds to the mounting evidence that Varian is finally "getting it together" on marketing. Public relations continues to lag despite the latest slogan, "Helping a fast world move faster."

Table 1. Comparison of Varian V76 with Competitors

	Varian Data V76	Data General Nova 3	General Automation GA-16/330	Digital PDP-11/45(1)	Hewlett-Packard HP 21MX
Word Length, bits	16/16 + 2 parity	16/16 + 2 parity	16/16 + 2 parity	16/16 + 2 parity	16
Inst. Times, μsec					
Add	1.3	1.8	4.6	0.8-1.8	1.9
Multiply	4.8	6.9(2)	21.2	3.6-4.7	12.8
Divide	5.2	7.5(2)	20.3	7.5-8.6	17.0
Fl. P. Add(3)	3.7*	7.7*	*	2.8-6.5*	22-54
Fl. P. Multiply(3)	6.1*	11.3*	*	3.0-8.2*	48-57
Fl. P. Divide(3)	8.6*	13.7*	*	3.0-9.9*	41-76
Max. Memory, bytes	512K	64K/256K	128K	253,952	512K
No. of GP Registers	8	4	16	16	4
Max. DMA Rate, bytes/sec	2M/6M(4)	2M	2M	2M	1.2M
Price, $					
CPU + Memory					
32K bytes	—	4,400	5,250	23,900	7,650
64K bytes	12,200	7,100	8,250	32,000	11,800
256K bytes	30,850	34,200	—	55,500(5)	36,150

*Optional, at extra cost. NA - Not available. — Not applicable.

Notes:
(1) The PDP-11/45 can use core, MOS, or bipolar memories; the first number is for bipolar memory and the second number is for core memory. Price is for core memory.
(2) Operands are unsigned integers on standard x and ÷ feature.
(3) All the floating point times are based on 2-word (32-bit) operands. The PDP-11/45 times are ranges based on memory used and the amount by which the CPU time overlaps floating processor time; the first number is CPU time and the second number is floating point processor time.
(4) Via Priority Memory Access (PMA) and dual ports.
(5) Maximum memory is 253,952 bytes.

Table 2. Varian V76 Compared to the Digital PDP-11/70

Characteristics	Digital PDP-11/70	Varian V76
CENTRAL PROCESSOR		
Microprogrammed	Yes	Yes
Control Memory	ROM	ROM
No. of Registers	10; 3 stack pointers; 1 program counter; all 16-bit; all can be used as indexers.	8; 7 can be used as index registers.
Word Length, bits	16	16
Addressing		
Direct	To 64K bytes	To 4K bytes
Indirect	Single level to 64K	Multilevel to 64K
Indexed	Yes	Pre- and post-indexing
Mapping	Yes, to 2M bytes	Yes, to 512K bytes
Instruction Set		
Implementation	Firmware	Firmware
Types	Single word	Single and double word
Number	400 std; 46 opt	187 std; 14 opt
Floating-Point	Hardware opt	Hardware opt
Hardware Stack	Yes	No
Instruction Execution Times, μsec		
Fixed-Point		
Add	1.0	1.3
Multiply	3.8	4.8
Divide	8.3	5.2
Floating-Point(1)		
Add	2.0	3.7
Multiply	3.9	6.1
Divide	4.9	8.6
Writable Control Store		
Interrupts	No	Up to 512 x 64 bits
Levels	4 lines, 8 levels	Up to 64
Type	Hardware	Hardware
MAIN STORAGE		
Type	Bipolar (cache); core (main memory)	n-channel MOS
Cycle Time, μsec	0.24 (bipolar); 1.0/32 bits (core)	0.660/16 bits
Basic Addressable Unit	Word, byte	Byte, word, doubleword
Bytes/Access	4	2
Cache Memory	Bipolar; 2,048 bytes	No
Capacity, bytes		
Min.	64K	64K
Max.	2M	512K
Increment Size, bytes	64K	64K/128K
Ports/Module	1	2
Error Checks	Parity std	Parity opt; 1 bit/byte
Memory Protection	Yes, memory management and 3 operating modes	Yes, in pages of 512 words
Memory Management	Yes	Yes
Interleaving	Yes, 2 way	No
INPUT/OUTPUT		
Max. Devices Addressable	No limit	64
Programmed I/O	Yes (UNIBUS)	Yes, firmware
DMA	Std (UNIBUS); plus 4 high-speed data channels	Std; high speed; PMA

Table 2. (Contd)

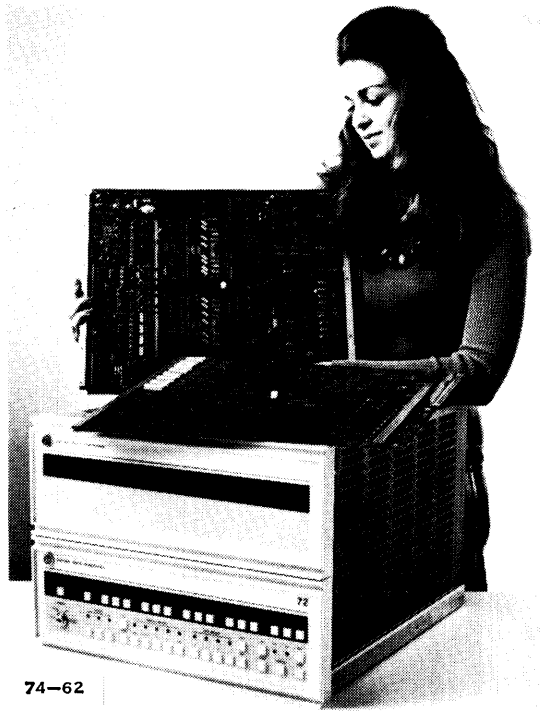
Characteristics	Digital PDP-11/70	Varian V76
DMA Transfer Rate, bytes/sec	4M (UNIBUS); 5.8M (data channel)	0.66M (std); 2M (high speed); 6M (PMA)
PRICE		
Price for System with 128K-byte memory	$54,600(2)	$20,950(3)

Notes:
(1) Times are for 2-word operands.
(2) CPU bundled with console, line clock, and installation.
(3) With byte parity, programmer's console, installation, and memory mapping to 512K bytes.

PRICE DATA

Model No.	Description	Purchase Price $	Monthly Maint. $
Processors			
	V76 Computer, includes x/÷, automatic bootstrap loader for TTY, memory parity logic, DMA logic, chassis, programmer's console, and expanded instruction set.		
76-1100	V76 Computer in 7-inch chassis with 5 slots. Memory and power supply are not included.	5,400	105
76-1101	Same as 76-1100, except 14-inch chassis with 15 slots.	6,000	105
	Memories		
76-2504	32,768-Word, Dual-Port Semiconductor Memory; 660-nsec cycle time.	4,800	45
76-2505	Same as 76-2504, except with parity.	5,300	50
76-2506	63,536-Word, Dual-Port Semiconductor Memory; 660-nsec cycle time.	8,900	85
76-2507	Same as 76-2506, except with parity	9,900	95
	Options		
76-3001	Automatic Bootstrap Loader (ABL) for paper tape reader instead of standard for Teletype.	250	6
76-3002	Same as 76-3001, except for disc and operates with DMA.	250	6
76-3003	Same as 76-3002, except for device and operates with Priority Memory Access (PMA).	950	11
76-3004	Same as 76-3003, except for device.	950	11
76-3010	Real-Time Clock (RTC) for special configurations. Customers of non-VORTEX systems may specify source inputs of 10K Hz, line frequency, external input, or alternate counter overflow for both the free-running counter and the variable-interval interrupt counter.	250	6
76-3040	Option Package: Power Failure/Restart, Real-Time Clock, and TTY/CRT Controller	600	6
76-3041	Same as 76-3040, plus Memory Protect	750	8
76-3042	Same as 76-3040, plus Priority Memory Access (PMA).	1,000	10
76-3043	Same as 76-3040, plus PMA and Memory Protect.	1,150	12
76-3060	230V AC, 50 Hz System Power Input for processor.	500	0
70-3100	Block Transfer Controller (BTC) for automatic data transfers via the PMA channel. Max. of four BTCs per V76 processor with PMA.	1,500	11
70-3101	Priority Interrupt Module (PIM) eight levels of external interrupts. Max. of eight PIMs (64 levels) per V76 processor.	500	6
70-3102	Buffer Interlace Controller (BIC), provides block transfer for up to 10 peripheral controllers. Max. of eight BICs per V76 processor.	500	6
76-3200	Data Save Power Supply and Battery for semiconductor memory.	500	6
76-3300	Memory Map with automatic allocation and control for up to 256K words of main memory; includes cable.	2,500	39
76-3400	Floating Point Processor for single and double precision floating point arithmetic operations. Direct parallel connection to CPU and memory.	4,950	39
76-4000	256-Word (64 bits) Writable Control Store (WCS); 190-nsec cycle time; 16-register stack.	3,000	22
76-4001	Same as 76-4000, except 512 word.	4,000	28
76-4002	512-Word (64 bits) Writable Control Store (WCS); 190-nsec cycle time; 16-register stack; instruction register; writable decode control store; writable I/O control store.	5,000	39
Power Supplies and Expansion Chassis			
70-4080	Power Supply for CPU and Memory; 40 Amp.	2,000	15
70-4090	Power Supply for CPU Options: WCS, Memory Map, and Floating Point; 30 Amp.	1,000	6
70-4095	I/O Expansion Power Supply; 17 Amp.	1,000	10
70-4096	I/O Expansion Power Supply; 35 Amp.	1,500	12
70-9006	I/O Party Line Expander for 10-unit load in I/O Expansion Chassis.	600	11
70-9010	First I/O Expansion Chassis with 22 I/O slots and cables. Power supply is not included.	1,400	NC
70-9011	I/O Expansion Chassis with 22 I/O slots and cables. Power supply is not included.	1,400	NC
70-9110	Memory Expansion Chassis "Slave" with cables and 7 slots. Power supply is not included	1,100	NC
70-9111	Memory Expansion Chassis "Master" with cables and 7 slots. Power supply is not included.	1,100	NC

NC — No Charge



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OVERVIEW

The Varian V-70 Series consists of four models: V-71, V-72, V-73, and V-74, all based on a general-purpose, microprogrammed digital computer. Microprogramming for the basic system is implemented by a read-only memory of 512 64-bit words contained in the processor. Up to three Writable Control Store (WCS) modules of 256 or 512 words (64-bit) can be added to a system to store microprograms. The processor can execute these microprograms from either the basic control or WCS.

Main memory for the V-71 and V-72 consists of core modules only. For the V-73 and V-74, it can consist of core modules, semiconductor modules, or a combination. Each semiconductor module and some of the core modules have two ports of entry. While the V-71 and V-72 use only single-port modules, the V-73 and V-74 basic systems are dual-port systems that can attach either single- or dual-port memory modules. Differences among the models are summarized in Table 1.

Word length is 16 bits, increasing to 18 bits with the addition of memory parity. Cycle time per word is 660 nanoseconds for core memory and 330 nanoseconds for semiconductor memory.

The basic V-71, V-72, V-73, and V-74 microprocessors are Varian 620/f emulators. Thus, they can execute all the software that has been programmed for the 620 Series of computers and can also use all the 620 Series peripherals. The internal design of the microprocessor, however, has many features that are unavailable for the 620f: facility for a WCS of 256 to 1,536 words, 16 general-purpose registers, 18-bit-wide address bus, instructions to load the WCS from main memory and to jump to and return from WCS, and (optionally) hardware-implemented floating point. In addition, the microprograms executed from WCS can implement an entirely different instruction set from that of the 620/f, and can address 65K words of memory. Optional memory mapping, standard on the V-74, extends addressing to 256K words for V-72 and V-73. (Memory mapping is unavailable on the V-71.)

Varian uses WCS in three basic ways:

- To enhance the 620/f emulator by adding such features as a microprogrammed floating-point processor, byte move and compare instructions, stack manipulation, Fortran — do-loop terminator, and parameter passing optimizing.
- To microprogram functions specific to a user's application. Varian supplies a microassembler plus test and debug aids.
- To define new instruction sets that utilize the processor's advanced features, such as multiple general-purpose registers and 18-bit-wide address bus.

Table 1. Differences among V-70 Series Models

CHARACTERISTIC	V-71	V-72	V-73	V-74
MAIN STORAGE				
Type	Core (single port)	Core (single port)	Core (single or dual port); MOS (dual port)	Core (single or dual port); MOS (dual port)
Cycle Time (μsec)	1.2	0.66, 1.2	0.66 or 1.2 (core); 0.33 (MOS)	0.66 or 1.2 (core); 0.33 (MOS)
Min Capacity (bytes)	32K	16K	16K	64K
Max Capacity (bytes)	64K	64K (in std CPU); 512K with mapping	64K (in std CPU); 512K with mapping	512K (mapping std)
Increment Size (bytes)	32K	Core: 16K, 64K	Core: 16K (dual port), 32K or 64K (single port); MOS: 16K (dual port)	Core: 16K (dual port), 32K or 64K (single port); MOS: 16K (dual port)
Parity	No	Opt	Opt	Opt
Protect	Opt	Std	Std	Std
Memory Mapping	No	Opt	Opt	Std

The memory mapping option with virtual memory addressing of 262,144 words is supported by VORTEX II, a new version of the Varian Omni-Task Real-Time Executive (VORTEX) operating system. With VORTEX II, memory mapping is transparent to the user.

When the models of the V-70 Series are operating as 620/f emulators, they are faster than the 620/f and inherit the extensive software library from the 620 Series, first introduced in 1965. The 620 Series computers have been used extensively for process control, test and measurement, scientific processing, data acquisition, and general-purpose processing. Software support ranges from monitoring for small-scale stand-alone systems to real-time and batch operating systems for medium- to large-scale installations. The V-70 and 620/f specifications are compared in Table 2.

Today, the V-70 Series is a strong contender in the data communications market. Standard hardware configurations are available for front-end preprocessing, remote concentration, data switching, remote job entry, and network control. Special software runs under the VORTEX/VORTEX II operating systems.

Varian markets its minicomputers from 20 sales offices across the United States, four in Canada, and one in Mexico. Outside North America, the company has offices in Australia, Brazil, Germany, Belgium, France, Holland, Israel, Sweden, Switzerland, and the United Kingdom. The European organization's headquarters in Zug, Switzerland, also handles marketing to Yugoslavia, Spain, Portugal, Italy, Greece, Turkey, Africa, India, the Near East, and Socialist countries.

All Varian users are invited to become members of the VOICE Users Group, which promotes library maintenance and program exchange. Varian acts as a communications channel for the group in order to eliminate redundant effort when several users are trying to solve the same problem.

COMPETITIVE POSITION

Varian Data Machines has consistently been a leader in the minicomputer field with its 520 and 620 Series of computers. The 520 Series, which is no longer marketed, was based on 8-bit words and aimed primarily at OEM buyers. The 620 Series was well-designed initially, and

Table 2. Varian V-70 Series Compared with Varian 620/f

CHARACTERISTIC	620/f	Varian 70 Series
CENTRAL PROCESSOR		
Instruction Set		
Number (std, opt)	142 std, 8 opt	175 std, 18 opt
Floating-point arithmetic	Subroutine	Subroutine or hardware
Microprogramming	No	Yes
No. of Programmable Registers	3	3
Decimal Arithmetic	No	No
Addressing		
Direct (no. of wds)	32K	2K; 32K*
Indirect	Multilevel to 32K	Multilevel to 32K
Indexed	—	Pre and post to 32K wds
Priority Interrupt Levels	0-64 in 8-level increments	0-64 in 8-level increments
MAIN STORAGE		
Type	Core (single port)	Core (single or dual port); MOS (dual port)
Cycle Time (μsec)	0.75	0.66, 1.2 (core); 0.33 (MOS)
Memory Mapping	No	Yes (opt on V-72, V-73; std on V-74)
Min Capacity (bytes)	8K	16K (core); 16K (MOS)
Max Capacity (bytes)	64K	512K with mapping
Increment Size (bytes)	8K, 16K	16K, 32K, or 64K (core); 16K (MOS)
Parity	No	Opt
Protect	Opt	Std
ROM	Opt	Std control store; WCS opt
Use	Program	Microcode
Capacity (bytes)	—	1,528 wds (64-bit wd)
I/O CHANNELS		
Programmed I/O	Std	Std
DMA Channels (no.)	Std (up to 4 with BICs); PMA opt (4)	Std (up to 4 with BICs); PMA opt (4)
Multiplexed I/O (no. of subchannels)	No	No
Max Transfer Rate (wds/sec)		
Within memory	222,222	252,525 (core); 505,050 (MOS)
Over DMA	274K; 1.3M (PMA)	382.7K; 1.5M (PMA-core memory); 3.3M (PMA-MOS memory)

its longevity rivals that of such durable competitive systems (and their compatible successors) as the DEC PDP-8, Honeywell 16 and 700 Series, Hewlett-Packard 2100 and 21MX Series, and IBM 1130. Like the manufacturers of these systems, Varian has kept the 620 Series competitive by adding new features: faster memories, better I/O facilities, more interrupt levels, new peripherals, and extensive software support.

Although the V-70 Series uses a microprogrammed processor that is quite different from the 620 Series processors, the basic system provides upward software and peripheral compatibility with the 620 by emulation. The V-70 Series, however, is much more powerful and flexible than the 620 because it can implement new features and new instruction sets in WCS. Also, fast MOS memory modules can be used on the V-70 to increase throughput.

With memory mapping, the V-70 can support up to 256K words (512K bytes) of main memory as compared to 32K words on the 620 Series (65K on 70 Series systems using WCS). The floating-point processor, released in 1974, is about 30 times faster than the 620 floating-point subroutines.

The V-70 competes with the systems mentioned previously, in real-time data acquisition, process control and industrial control applications, data communications, and general-purpose batch processing jobs. With its expanded memory capacity, using memory mapping, it also competes with such larger systems as the PDP-11/45, PDP-15, Sigma 5, Hewlett-Packard 3000, and the new Data General Eclipse.

The path Varian has chosen for the V-70 Series protects the 620 customers' investment in software and peripherals, and gives the 620 users a system for upgrading. In addition, the V-70 expands the market for Varian computers. Outside the OEM market, customers who will microprogram WCS are probably few. The feature adds considerable system flexibility and can significantly increase throughput for certain applications.

The new V-71 model, meanwhile, extends the V-70 Series downwards, providing new customers with a low-cost entry-level system. The compact 16K-word memory modules can be used on the other processors, effectively lowering the price of the whole line.

Varian's floating-point processor (delivered in 1974) handles both single and double floating-point operations. Tests run by Varian on the V-72 and V-73 indicate problems, such as double-precision A = B + C, A = B • C and A = B ÷ C running in the actual operating system environment compare favorably with a Data General 840 operating under FORTRAN V and with a PDP-11/45.

User Reactions

A southern company that specializes in computer-based law enforcement, hospital, and other special control systems selected the V-73 for its law enforcement system because of the VORTEX software. The company felt that VORTEX was the best real-time operating system on the minicomputer market. At present this company uses Digital and Hewlett-Packard computers as well as the Varian 620 in hospital and other control systems.

The largest of the five law enforcement systems that this firm currently has in operation includes dual processors. Each processor has 32K words of core, a 200-million-word disc subsystem, two tape drives, two TTYs, card reader, paper tape reader, printer, two communication controllers, a variety of user-interfaced terminals, and special peripherals and disc and line switches installed by the user. Since its introduction, the system has been used successfully to emulate IBM 2740s that can communicate with state-owned computers. This law enforcement system is basically a data bank for wanted criminals, stolen goods, vehicle registration checks, and so on. VORTEX software has lived up to the company's high expectations, and the Varian components are extremely reliable. The user noted, however, that the OEM electromechanical devices were not quite as reliable.

A second V-73 user is a manufacturer primarily involved with the design and development of NASA's mission control center in Houston. The company also has a contract with NASA to maintain the medical records' storage and retrieval system for the space center's employees.When the system was set up, the first choice was the Hewlett-Packard 3000. Although Varian 73 was the second choice, it was still selected because of price. Additional savings resulted from "borrowing" peripherals from the seven Varian 620s already being used by the firm for other purposes. The programming staff could readily handle the required major modification to VORTEX because the assembly language was already familiar.

In retrospect, this user was glad the company had chosen Varian, because the installation was set up in a reasonably short time. Hewlett-Packard would have required a longer period because it had some initial problems with the 3000 software. Varian, moreover, compares favorably with other minicomputer manufacturers for system support and hardware reliability. NASA's mission control center has 15 minicomputers, including three Digital PDP-11/45s, seven Varian 620s (used mostly in dedicated applications), the V-73, and four minicomputers from other manufacturers. The V-73 has performed very well — this user, in fact, characterized it as a "better, cheaper 11/45."

CONFIGURATION GUIDE

All models in the V-70 Series are based on the same processor hardware. The chief differences among the

four models are the type of memory used and its related options. The V-71 and V-72 use single-port core memory exclusively. The V-73 handles dual-port core and MOS memory modules. Minimum systems include 8K words (V-72 and V-73) or 16K words (V-71) of memory; memory expansion to 32K words is standard. With the memory mapping option, memory expands to 256K words. The minimum V-74 system is a 32K-word, dual-port system using either core or MOS modules. A number of V-72 and V-73 options, such as memory mapping, are standard features.

The basic processor for all three systems has hardware multiply/divide, at least one real-time clock, power fail/restart, memory protection, I/O bus with direct memory access (DMA), at least one automatic bootstrap loader (three are standard on the V-74), chassis for up to 32K words of memory, power supply, and programmer's console. In addition to a larger initial memory and memory mapping, the V-74 processor includes as standard the following features: priority memory access (PMA), 512 64-bit words of WCS, the equivalent of the first I/O chassis (18 slots), the equivalent of a memory expansion chassis with power for four memory modules, and a keyboard/CRT display terminal. All of these items are options on the V-73, so it can theoretically expand to the equivalent of any V-74 configuration. However, an expanded V-73 is more expensive than the equivalent V-74 configuration. The V-71 and V-72 are more restricted; they are single-port systems and cannot handle the faster MOS memory modules. As a result, they are slower and less powerful than the V-73 and V-74; moreover, the V-71 cannot support the mapping option.

All three systems have various submodels to designate whether core or MOS memory, memory parity, or PMA are included. Table 3 lists the features of the various processor submodels.

Up to 32K words of memory can fit the mainframe for all processors; an expansion chassis is attached for each additional 32K words of memory (one expansion chassis is standard on the V-74). Each processor has a number of printed-circuit slots within the mainframe for attachment of options and peripherals ("P" slots). An I/O expansion chassis is available to attach additional peripheral devices and related options (such as the priority interrupt modules). Peripheral devices or options require either an I/O- or P-type slot. In addition to the number of P slots, expansion of the peripheral load must consider the bus load, which expands in increments of 10 loads after the original 10 in the main chassis have been exhausted.

In addition to the optional memory parity, memory mapping, and PMA features already described, a number of important options add flexibility to the processor and facilitate use of the peripherals. The WCS option can add up to three increments of 256 or 512 64-bit words to extend the processor's read-only control memory for additional user- or Varian-defined microinstructions. A data save option provides battery power to preserve the

Table 3. Varian V-70 Series: Standard Features for Processor Submodels

Processor Submodel	Memory Size (wds)	No. of P Slots	PMA	Parity (2 bits)	Memory	Data Save	System Availability			
							V-71	V-72	V-73	V-74
1000	32K	5	—	—	Core	—	—	—	—	X
1050	32K	5	—	Yes	Core	—	—	—	—	X
1100	8K	14	—	—	Core	—	—	X	X	—
1101	8K	14	Yes	—	Core	—	—	X	X	—
1200	8K	14	—	Yes	Core	—	—	X	X	—
1201	8K	14	Yes	Yes	Core	—	—	X	X	—
1300	16K	14	—	—	Core	—	—	X	—	—
1301	16K		Yes	—	Core	—	—	X	—	—
1330	16K	4	—	—	Core	—	X	—	—	—
1340	16K	4	—	—	Core	—	X	—	—	—
1350	16K	4	—	—	Core	—	X	—	—	—
1400(1)	16K	14	—	Yes	Core	—	—	X	—	—
1400(2)	32K or 16K	8	—	—	MOS	—	—	X	—	X
1401	16K	14	Yes	—	Core	—	—	X	—	—
1450	32K	8	—	Yes	MOS	Yes	—	—	—	X
1500	8K	4	—	—	MOS	—	—	—	X	—
1501	8K	4	Yes	—	MOS	—	—	—	X	—
1600	8K	4	—	Yes	MOS	—	—	—	X	—
1601	8K	4	Yes	Yes	MOS	—	—	—	X	—

Notes:
(1) Two Model 1400 processors are defined: one is a 16K-word core-based processor and the other is a 32K-word MOS-based processor.

contents of semiconductor memory modules during a loss in line voltage. The Priority Interrupt Module (PIM), Buffer Interlace Controller (BIC), and Block Transfer Controller (BTC) are particularly important for efficient handling of the various peripheral I/O subsystems. In addition, the hardware floating-point processor can appreciably enhance throughput for some applications.

In addition to the "basic" V-71, V-72, V-73, and V-74 processors, Varian offers five "standard" hardware/software packages:

- Model 72-0001 — 16K-word, V-72-based Batch/FORTRAN Processing System with cartridge disc, line printer, paper tape reader, and Teletype.
- Model 72-0002 — 24K-word, V-72-based Batch/FORTRAN Processing System with cartridge disc, line printer, nine-track magnetic tape drives, card reader, and Teletype.
- Model 72-0011 — 24K-word, V-72-based real-time operating system under VORTEX, with cartridge disc, card reader, and Teletype.
- Model 73-0020 — 32K-word, V-73-based real-time operating system under VORTEX, with cartridge disc, line printer, nine-track magnetic tape drive, card reader, and Teletype.
- Model 74-0050 — 64K-word, V-74-based real-time operating system with 512-word WCS and FORTRAN accelerator firmware, memory mapping, high-density (14.5-million-word) disc, line printer, nine-track magnetic tape drive, card reader, paper tape reader and punch, keyboard/CRT, and BTC.

Included in each package is the appropriate number of PIMs, BICs, I/O chassis, and cabinets to support the configuration.

The peripheral device complement for the V-70 Series includes: teletypewriters, paper tape and punched card equipment, line printers, and an impressive number of magnetic tape and disc storage units. Special peripherals are an oscilloscope display, plotters, various digital I/O controllers, and an extensive list of analog/digital equipment. Controllers are also offered for a number of commercial communications data sets. See Table 4 for a listing of peripherals with specifications.

Software includes two full-blown operating systems: VORTEX, which provides multiprogramming capability with real-time foreground processing and background batch processing, and MOS, which controls batch processing systems. VORTEX II is a special version of VORTEX used on systems with memory mapping.

Several language processors are available: DAS assembler (three versions), FORTRAN IV, two versions of BASIC, and RPG IV. BEST, a real-time monitor, provides control for small, dedicated real-time systems. Maintenance, debugging, and editing programs are offered, along with a math library. Table 5 lists major software packages and configuration requirements.

Table 4. Varian V-70 Series: Peripherals

Model No.	Description
Discs	
70-7500/01	Moving-head disc, 14.5M wds/2316-type pack, 4 drives/controller
70-7510/11	Moving-head disc, 46.7M wds/2316-type pack, 2 drives/controller
70-7600/01	Moving-head dual disc, 2.34M wds/drive, 1 fixed, 1 removable 5540-type cartridge, 2 drives/controller
70-7610/11	Moving-head disc, 1.17M wds/drive, 2315-type pack, 3 drives/controller
70-7700/1/2/3	Fixed-head discs, 61K/123K/246K/491K wds capacity, 17-msec avg access
Magnetic Tape	
70-7100/1	9-trk, 800 bpi, 25 ips; 4 drives/controller
70-7102/3	9-trk, 800 bpi, 37.5 ips; 4 drives/controller
Paper Tape	
70-6300	300-cps reader
70-6310/11	75-cps punch
70-6320	300-cps reader and 75-cps punch
Punched Cards	
70-6200	300-cpm reader
70-6201	35-cpm keypunch/punch
Terminals	
70-6100/2/4	Teletype ASR 33/ASR 35/KSR 35; 10 cps
70-6401	A/N CRT display with keyboard, TTY compatible
70-6400	Oscilloscope, Tektronix 611
Printers	
70-6701	245-1,100 lpm, 132 col, 64 char set
70-6720/21	300 lpm, 136 col, 64 char set
Printer/Plotters	
70-6606	80 styli/in. (1,320 A/N lines/in); 8.5-in. paper width
70-6608/02	100 styli/in. (1,000 A/N lines/in.); 11/14.875-in. paper width
70-6640	Model 70-6606 with 7x7 dot matrix print/plot, 64 char set
70-6641/42	Model 70-6608/02 with 7x11 dot matrix print/plot, 123-char set
70-661/3/5/7	100 styli/in. printer/plotters; 460/410/370/210 A/N lpm, 8.5/11/14.875/22-in. paper widths
70-6621/3/5/7	100 styli/in. printer/plotters with linear writing head, 690/890/690/550 lpm; 8.5/11/14.875/22-in. paper widths
Process I/O	
70-8000 Series	High-Level Analog Input Systems; 16-256 channels, differential & single-ended inputs
70-8100 Series	Low-Level Analog Input Systems; 13-bit A/D conversion, 16-256 channels
70-8200 Series	Digital-to-Analog (DAC) Subsystem; 10-, 12-, and 14-bit channels, to ± 10 volts, ± 10 mA; to 64 channels
70-8300	Digital Controllers; 1 16-bit input, 1 16-bit output register
70-8310/11	Digital Output; 2 16-bit output registers, 1 buffered input
70-8410/11	Digital Input; 4-256 16-bit input registers
70-8500	Relay Contact I/O modules
70-8601	Interface Console; for 16 channels, high-level analog input, 8 analog output, 1 digital I/O, 8 sense and control lines, timer, LED display

Table 4. (Continued)

Communications	
70-5201/2/3	MUX; for 16/32/64 sync, async, or direct-connection to 9,600 baud terminals
70-5211/2/3	Like 5201/2/3 but for systems with memory map
70-5702/12	BSC MUX; for up to 8 BSC channels via DMA; without/with memory mapping system
70-5401/02	Single/Dual Data Set Controller; for Bell 103 or 202
70-5501/02/03/04	Single or Dual Synchronous Controllers; to 2,400 or to 50K baud
70-5505/06/15/16	BSC Controller; for 1 or 2 channels, with or without memory mapping system
70-5601/02/03	Universal Async Controllers; with RS-232 C/20-60 ma current loop/20 ma relay
70-570	ACU Controller; for Bell 801

Table 5. Varian V-70 Series: Software

Package	Description
VORTEX	Real-time multitasking operating system with FORTRAN IV, RPG IV; requires CPU, PIM, BIC, 24K-word memory, TTY or CRT, and card, paper tape, or magnetic tape I/O
VORTEX II	Like VORTEX but with memory mapping management; same requirements as VORTEX except 32K memory and memory mapping option
MOS	Batch operating system with FORTRAN IV and RPG IV; requires CPU, PIM, BIC, 8K words of memory, magnetic tape I/O
Dataplot II	Adds Statos 31/33 printer/plotter capability to MOS; requires 16K words of memory
BEST (stand-alone)	Core-only real-time monitor; requires PIM, BIC, console
VPERT	Minimum 8K-word system software, paper tape I/O, runs under VORTEX (II) or MOS; requires either card reader or paper tape in addition to operating system
FORTRAN (stand-alone)	Requires CPU, paper tape I/O, PIM, BIC
RPG IV (stand-alone)	Requires CPU, card reader, card punch, line printer
Microprogramming support	Runs under MOS or stand-alone; requires paper tape card or magnetic tape I/O
BASIC	Single terminal version; requires TTY or CRT, 8K-word memory, paper tape I/O; extended version requires TTY or CRT, 16K words of memory, paper tape I/O, disc
HASP/RJE	Runs under VORTEX (or VORTEX II); requires card or magnetic tape I/O
VTAM	VORTEX telecommunications access method; runs under VORTEX or VORTEX II
NCM	Network Control Module, using Network Definition Language (NDL); interface between operator and system to simplify network definition

COMPATIBILITY

The V-70 Series is upward software compatible with Varian's 620 Series computers. Magnetic tape data formats are IBM compatible. The V-70 Series uses the same peripheral devices as the 620.

MAINTENANCE

Varian supplies two types of on-call service contracts. The full-service plan provides on-call, on-site maintenance and replacement of needed parts for the contracted shift(s), while the limited-service plan charges lower monthly fees but requires the customer to pay for replacement parts. Full-time, on-site maintenance contracts are also provided. Customers who do not want maintenance contracts can choose individual, on-call, on-site repairs, charged on a per-hour basis. As an alternative, they can take equipment to an authorized factory service location.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint $
	CENTRAL PROCESSOR & WORKING STORAGE		
	V 71 CPU (includes multiply/divide, I/O bus with DMA, chassis, power supply and programmer console, 1,200-nsec cycle time)		
71 1330	With 16K Core, 4 P Slots	7,200	120
71 1340	With 16K Core (includes power fail/restart, Teletype controller, automatic bootstrap loader for teletypes, real time clock, 4 P slots)	8,100	120
71 1350	With 16K Core (same as 71 1340 except with memory protect)	9,100	120
71 2102	With 16K Core (includes single port memory)	3,250	30
	V 72 CPU, 14 P slots		
72 1100	With 8K Core	10,500	120
72 1101	With 8K Core, Priority Memory Access (PMA)	11,500	125
72 1200	With Memory Parity and 8K Parity Core	11,500	125
72 1201	Same as 72 1200 with PMA	12,500	130
	V 73 CPU Same as V 72 except (chassis for up to 32K of dual port memory, 14 P slots)	14,500	120
72 1300	With 16K Core	10,250	120
72 1301	With 16K Core (includes PMA)	11,250	125
72 1400	With 16K Parity Core (includes memory parity)	10,750	125
72 1401	With 16K Parity Core (includes memory parity and PMA)	11,750	130
73 1100	With 8K Core	14,500	120
73 1101	With 8K Core, PMA	15,500	125
73 1200	With Memory Parity and 8K Parity Core	15,000	125
73 1201	Same as 73 1200 with PMA	16,000	130
73 1500	With 8K MOS Memory, 4 P Slots	15,000	130
73 1501	With 8K MOS Memory, PMA, 4 P Slots	16,000	135
73 1600	With 8K Parity MOS Memory, 4 P Slots	15,500	135
73 1601	Same as 73 1600 with PMA, 4 P Slots	16,500	140
	V 74 CPU (same as V 73 except keyboard CRT display terminal, 3 automatic bootstrap loaders, console switch selectable PMA, direct memory access (DMA), memory map with memory protection for up to 256K of dual-port memory, 512 words of WCS, control console, processor, I/O, and memory chassis with associated power supplies in a single cabinet; provides 18 I/O slots, 8 MX slots, with power for up to four additional MOS or core memory modules and P slots as noted)		
74 1000	With 32K Core, 5 P Slots	35,900	345
74 1050	With Memory Parity and 32K Parity Core Memory, 5 P Slots	37,900	350
74 1400	With 32K MOS Memory, 8 P Slots	38,400	395
74 1450	With Memory Parity, 32K Parity MOS Memory, Data Saver, 8 P Slots	40,400	400
	CONFIGURATIONS		
V71 0007	V71 Based Real-Time Operating System (running under VORTEX 32K core memory; interleaved 1,200 nsec; ASR-33, TTY and a 2.34-M word disc; includes V71 with 16K-core memory; 16K core memory (1,200 nsec); disc – ABL; core memory interleaving; PIM; ASR-33 TTY; card reader, 300-cpm; disc., 2.34-M words; I/O chassis with PIM and BIC; equipment cabinet; VORTEX installation package; Maintain II)	29,500	305
72 0011	24K V-72-Based Real-Time Operating System (running under VORTEX w/a 2.3M-word cartridge disc, TTY, and card reader; includes V-72 with 8K core memory; 8K core memories (2); PIM (2); BIC (2); ASR-33		

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint $
	Teletype; card reader (300 cpm); disc (2.34M words); I/O chassis; cabinet; VORTEX installation package)	39,850	380
73-0020	32K Core Memory, V-73-Based Real-Time Operating System (includes V-73 with 8K core memory; 8K core memories (3); PIM (2); BIC (2); ASR-33 Teletype; card reader (300 cpm); line printer (245 lpm); 9-track mag tape (37.5 ips and control); disc (2.34M words); I/O chassis; cabinet (2))	71,600	515
74-0050	High Performance V-74-based Real-Time Operating System (includes V-74 with 32K memory; 8K core memories (4); block transfer controller; PIM (2); BIC; card reader (300 cps); paper tape reader (300 cps) and punch (75 cps); line printer (245 lpm); mag tape (9 trk, 37.5 ips and control); disc (14.5M words); I/O expansion chassis; VORTEX installation package)	101,750	942
	Core Memories		
XX-2100	8K Word (16 bits) 660-nsec Cycle	3,500	30
XX-2101	8K Word (18 bits) 660-nsec Cycle	4,000	35
XX-2102	16K Word (16-bit) Core Memory (1,200-nsec cycle time, single port)	3,250	30
XX-2103	16K Word (18-bit) Core Memory (1,200-nsec cycle time, single port)	3,750	35
XX-2400	32K Words	15,000	130
XX-2411	Same as 2401 except 18 bit.	17,000	150
	Semiconductor Memories		
	Available in dual port models for V-73 and V-74. XX indicates the CPU series.		
XX-2500	8K Words (16 bits), 330-nsec Cycle	4,000	40
XX-2501	8K Words (18 bits), 330-nsec Cycle	4,500	45
	PROCESSOR OPTIONS		
XX-3001/2	Auto Bootstrap Loader	250	5
XX-3003/04	Automatic Bootstrap Loader (for rotating memory instead of "standard" for Teletype for 72 & 73)	950	10
XX-3010	Real-Time Clock	250	5
XX-3030	Core Memory (odd/even interleaving)	2,000	10
XX-3031	Odd-Even Interleaving (for single port 1,200 nsec core memory in expansion chassis, up to 256K for 72, 73)	1,000	10
XX-3032	Odd/Even Interleaving (for 32K words of single port 1,200-nsec core memory in CPU)	500	10
XX-3050	Wrap-Around Addressing Feature	250	5
XX-3060	230V ac, 50-Hz System Power Input	500	0
XX-3100	Block Transfer Controller (BTC)	1,500	10
XX-3101	Priority Interrupt Module	500	5
XX-3102	Buffer Interface Controller (BIC)	500	5
73-3200	Data Saver Power Supply and Battery for 32K Words of Semiconductor Memory (V-73 only)	500	5
XX-3300	Memory Map	2,500	35
XX-3400	Floating-Point Processor	4,950	35
XX-4000	Writable Control Store (256 Words of Semiconductor Memory)	3,000	20
XX-4001	Writable Control Store (512 words)	4,000	25
XX-4002	Writable Control Store (512 words)	5,000	35
	MASS STORAGE*		
70-7500	Disc Memory and Controller (2316 pack, moving head, 14.5M words single spindle)	16,400	190
70-7501	Slave Unit for 70-7500	12,150	150
70-7510	Same as 7-7500 except 46.7M Words; Dual Head	30,300	275
70-7511	Slave Unit for 70-7510	25,550	235
70-7600	Disc Memory and Controller (5440 pack, moving head, 2.34M words, one fixed and one removable disc)	12,500	100
70-7601	Slave Unit for 70-7600	8,000	75
70-7610	Disc Memory and Controller (2315 pack, moving head, 1.17M words)	10,000	85
70-7611	Slave Unit for 70-7610	6,000	65
70-7700	Fixed-Head Disc and Controller (61K words, 17-msec avg access)	7,000	65
70-7701	With 123K Words	8,000	65
70-7702	With 246K Words	9,500	80
70-7703	With 491K Words	16,000	125
	INPUT/OUTPUT		
70-6100	ASR-33	1,580	35
70-6102	KSR-35	3,265	25
70-6104	ASR-35	5,320	30
70-6200	Card Reader and Controller (300 cpm)	4,000	40
70-6201	Card Punch and Controller (35 cpm)	8,000	60
70-6300	Paper Tape Reader and Controller (300 cps)	2,300	22
70-6310	Paper Tape Punch and Controller (75 cps, tabletop)	3,000	25
70-6311	19" panel mounted	3,000	25
70-6320	Paper Tape System (includes time-share controller, 300-cps reader, 75-cps punch)	4,700	47
70-6400	Oscilloscope Display	5,675	45
70-6401	Keyboard and Alphanumeric CRT	2,850	25
70-6402	Same as 70-6401 with 70-5602 controller	3,250	30
70-6403	Same as 70-6401 with kit and instructions to connect to controllers, or a spare unit	2,950	25
	PRINTER/PLOTTERS		
	STATOS® 31 FAMILY		
70-6606	8½-in. wide w/Controller (80 styli/in., 2.75 ips, 1,320 A/N lpi)	8,625	70
70-6640	Same as Model 70-6606 with 64-char 5 x 7 dot matrix hardware character generator and simultaneous print/plot options	9,325	70

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Model Number	Description	Purchase $	Monthly Maint $
70-6608	11-in. Wide Printer/Plotter with Controller/110 styli/in., 2.2 ips, 1,000 A/N lpi)	8,825	70
70-6641	Same as Model 70-6608 with 123-char uc/lc, 7 x 11 dot matrix character generator, and simultaneous print/plot options	9,525	70
70-6602	14-7/8 in. Wide Printer/Plotter with Controller (100 styli/in., 2.2 ips, 1000 A/N lpi)	9,025	70
70-6642	Same as Model 70-6602 with 123-char uc/lc, 7 x 11 dot matrix character generator, and simultaneous print/plot options	9,825	70
	Bi-Scan™ Writing Head Models		
70-6611	8½-in. Wide Printer/Plotter with Controller (100 styli/in., 1 ips, 460 A/N lpi)	7,975	70
70-6613	11-in. Wide Printer/Plotter with Controller (100 styli/in., 0.9 ips, 410 A/N lpi)	8,175	70
70-6615	14-7/8 in. Wide Printer/Plotter with Controller (100 styli/in., 0.8 ips, 370 A/N lpi)	8,875	70
70-6617	22-in. Wide Printer/Plotter with Controller (100 styli/in., 0.6 ips, 210 A/N lpi)	11,925	70
70-6621	8½-in. Wide Printer/Plotter with Controller (100 styli/in., 1.5 ips, 690 A/N lpi)	7,975	70
70-6623	Same as 70-6613 except 1.5 ips, 890 A/N lpi	8,175	70
70-6625	Same as 70-6621 except with 14 7/8-in. Wide Printer/Plotter with Controller	8,875	70
70-6627	Same as 70-6617 except 1.2 ips, 550 A/N lpi	1,925	70
	Line Printers		
70-6720	Line Printer and Controller (300 lpm, 136 col, 64 char, 11 position form length selector switch)	9,900	99
70-6721	Same as 70-6720 except 12 channel paper tape vertical format unit	10,200	102
70-6760	Static Eliminator Option	500	
70-6701	Line Printer (245 to 1,100 lpm, 132 col, segmented, buffered)	15,500	90
70-7100	Mag Tape Unit and Controller (9 trk, 800 bpi, 25 ips)	7,500	50
70-7101	Mag Tape Unit Slave	5,600	40
70-7102	Same as 70-7100 with 37.5 ips; includes control for 4 units	9,000	75
70-7103	Mag Tape Unit Slave	7,000	60
	DATA COMMUNICATIONS		
70-5201/11	Data Communications Multiplexor (including message oriented control for up to 16 high performance communication channels)	2,750	25
	Data Communications (Contd.)		
70-5202/12	Data Communications Multiplexor (for up to 32 communications channels)	4,000	35
70-5203/13	Data Communications Multiplexor (for up to 64 communications channels)	7,000	60
	DCM LINE ADAPTERS		
70-5301	Asynchronous Line Adapter with RS232C and CCITT V24	1,000	6
70-5302/3/4	Direct Connection Line Adapter	1,000	6
70-5305	Synchronous Line Adapter with RS232C and CITT V24	1,500	10
70-5306	Binary Synchronous Communication Line Adapter (for 1 communication channel)	1,500	10
70-5307	Automatic Call Unit Line Adapter	1,000	10
70-5308	Programmable Asynchronous Line Adapter (with RS232C or CCITT V24 compatibility for 4 channels of full- or half-duplex async operation up to 9,600 baud)	1,400	10
	ASYNCHRONOUS MODEM CONTROLLERS**		
70-5401	Data Set Controller	650	5
70-5402	Dual Data Set Controller	800	5
70-5501	Data Set Controller	1,250	8
70-5502	Dual 70-5501 Data Set Controller	1,800	12
70-5505/15	Binary Synchronous Communication (facilities for 1 communication channel)	3,000	20
70-5506/16	Binary Synchronous Communication (facilities for 2 channels)	4,500	20
	UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLERS		
70-5601/2/3	With RS232C Interface/20 or 60mA Current Loop or With 20 or 60mA Relay Interface	600	5
70-5701	Auto Call Unit Controller	1,250	8
	MULTIPLEXOR		
70-5702	Binary Synchronous Communication Multiplexor	2,000	20
	OPTIONS		
70-5801	Binary Synchronous Communications (wide-band interface option for Bell 300 Series modems.)	250	5

Notes:
* All controllers require ±12V dc.
(1) Varian Data Machines does not lease its systems.
(2) Maintenance prices are for full service contract; include on-call maintenance and replacement of required parts on the entire system. Prices are effective for installations within 100 miles of service center.

HEADQUARTERS

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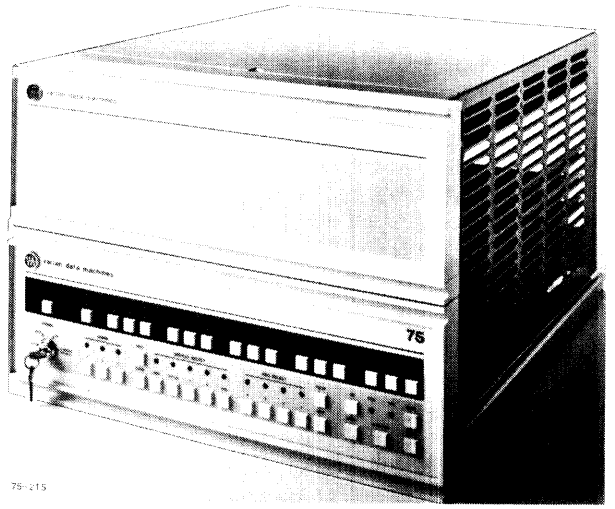
VARIAN DATA MACHINES

V-70 Series System (V-75) Special Report Update



OVERVIEW

The Varian V-75 is a V-73 processor with new control store boards added to implement an extended instruction set. The V-72 and V-74 processors can also be adapted to use the new instruction set. The new instructions operate on eight of the computer's 16 general-purpose registers, previously accessible only to the microprogrammer. The new registers R0 through R7 incorporate the three V-70 register set and add new facilities.

	V-70 Use	V-75 Use
R0	A (accumulator)	Byte or word accumulator, most significant half of double word operand
R1	B (accumulator or index register)	General-purpose register, least significant half of double word operand
R2	X (index register)	General-purpose register
R3	—	General-purpose register
R4	—	General-purpose register and most significant half of double word operand
R5	—	General-purpose register, least significant half of double word operand
R6	—	General-purpose register
R7	—	General-purpose register

The general-purpose registers R1-R7 can be used either as accumulators or index registers.

The new instructions provide the following operations.

- Register to memory — Load/Store/Add/Subtract using any register and a memory location; address can be indirect and indexed by any general-purpose register.
- Double precision — Double Load/Store/Add/Subtract/AND/OR/exclusive OR between either double word register (R0, R1 or R4, R5) and two consecutive memory locations; address can be indirect and indexed by any general-purpose register.
- Jump IF test condition met — Register Zero/Not Zero/Negative/Positive; Double Register Zero/Not Zero; test can be on any general-purpose register or either double word register.
- Byte — Load/Store Byte between right byte in R0 and any memory location; address can be indexed by any general-purpose register.
- Immediate — Load/Add immediate operand into any register.
- Register-to-Register — Transfer/Add/Subtract between any two registers.
- Single Register — Increment/Decrement/Complement any register.

The V-75 System is sold with the following features as standard items.

- V-75 CPU.
- Dual memory buses.
- 64K words of memory.
- Two-way interleaving of core memory.
- Multiply/divide.
- Eight registers.
- Three automatic bootstrap loaders: cartridge disc, high-speed paper tape, Teletype or disc pack.
- Power fail/restart and real time clock.
- Five or eight CPU slots for memory or peripherals.
- Programmer console.
- DMA I/O bus.
- PMA (priority memory access to separate memory port) bus.
- Memory map with protection for 256K words (512K bytes) of memory.
- Writable control store of 512 words, 64 bits each.
- I/O chassis with 19 I/O slots and I/O expander.
- System cabinet.
- Keyboard/CRT display terminal.
- On-site installation.
- 90-day warranty.

Memory

Memory can consist of combinations of single port, two-way interleaved/non-interleaved core memory with 800/990-nanosecond effective cycle time; dual-port, two-way interleaved core memory with 450/660-nanosecond effective cycle time; and dual-port 330-nanosecond MOS memory. Byte parity is optional on all memory modules. Memory interleaving is also optional. Core memory is available in 8K-word and 16K-word modules. Bulk core modules of 64K words are also available; they consist of four 16K modules packaged together.

A second Writable Control Store (WCS) module can be added to the system or a Floating Point Processor. The new Fast FORTRAN Firmware in addition to the floating Point Processor not only decreases the amount of memory required for FORTRAN programs but shortens execution time substantially. The Fast FORTRAN Firmware performs the following functions:

- Array indexing.
- Parameter passing.
- DO loop termination.
- Double precision integer operations.
- Floating Point compare and branch.
- Square root.
- Converts relational expression to logical value.

Peripherals

The V-75 supports all the peripherals available for the rest of the V-70 line. With dual memory ports and the PMA bus, the V-75 can support an I/O rate of 6M bytes per second as long as the CPU and the PMA channel are not in contention for the same memory module.

Software

Software for the V-75 is the same as that available for the rest of the V-70 Series, which is substantial. Recently, additional system software has been released for the V-75 as well as the rest of the V-70 line. The VORTEX II operating system release E2 supports the new V-75 instruction set. New additions to the Varian V-70 Series software include enhancements for data base management, telecommunications, and timesharing.

The Total data base management system developed by Cincom is now available to run under VORTEX II; which requires a V-70 CPU, 64K words of memory, an input device and a disc. It is the basic version of Total, a single task, fully reentrant system, which uses a random file organization. It supports the standard Total hierarchical network concept. Master files can be linked to several detail files. The random file organization is economical of disc space. The system has no query facility and no data security, thus the user must develop his own. A data base definition language and a data base generator are available to help the user develop a data base.

The Total license fee is $9,500.

Cincom under Varian's supervision, will install Total in the VORTEX II operating system. First delivery implementation is scheduled for October 1975.

A single pass RPG II compiler that is industry compatible is now available.

A Time Sharing Subsystem is available under VORTEX II to support Basic from multiple terminals.

VTAM (VORTEX Telecommunications Access Method) Communication Software provides control functions for message switching, data concentration, and front-end processing under VORTEX. A terminal or communication line is handled like a logical unit, and the user can issue READ and WRITE commands to a terminal once it has been "Opened." The VTAM software handles line, data and device-dependent constraints.

Additions have recently been made to the FORTRAN IV compiler to bring it more in line with IBM FORTRAN Level G as well as to optimize the output code.

First production line deliveries of the V-75 are scheduled for August 1975. The VORTEX II support of the V-75 was released in July 1975.

Competitive Position

The V-75 mainframe characteristics are compared to some of its major competitors in Table 1. These are Digital's PDP-11/70, the Interdata 8/32, and the SEL 32. Other strong competitors are the MODCOMP IV, Data General ECLIPSE 200, Digital Computer Control DCC-616, PRIME 300, and Hewlett-Packard HP 21MX. As Table 1 shows, members of the pack at the top of the minicomputer lines have a lot in common, yet there are significant differences inherent in innocuous-looking numbers. For example, the number of ports to memory modules entry shows that only the V-75 of those listed has dual memory ports. Memory modules on other systems, however, have multiple ports — MODCOMP IV modules can have up to four ports, the DCC 616 can have two. An operating system with any kind of elegance, even almost by accident, can substantially increase throughput using multiple-ported rather than single-ported memory. For multiple processor configurations, multi-ported memory allows processors to share memory modules with little contention.

A second item unique to the V-75 among the computers shown is writable control store. Interdata will probably provide it eventually for the 8/32, but it is not now available. It is available for the HP 21MX and the DCC 616. Writable Control Store is of little interest except to sophisticated users, but it is useful for OEM's who want to implement special features.

Of course, the V-75 is a 16-bit, word-oriented processor but, like the PDP-11/70, it has instructions for double word operands. Unlike the PDP-11/70 or Interdata 8/32, the V-75 does not have cache memory.

Instruction execution times on the four systems are very comparable, but the fixed-point times given are for 32-bit operands on the 8/32 and SEL 32 and for 16-bit operands on the PDP-11/70 and V-75.

For features not listed in the table, such as peripherals, the V-75 has a broad range of standard peripherals, disc and tape drives, printers, card and paper tape readers and punches. One device that Varian is well known for is its STATOS® Printer/Plotter. It is extremely fast and versatile. It is software supported by MOS under Data Plot II and by VORTEX.

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Varian is also a major instrumentation supplier, thus many A/D, D/A, and digital controllers are available.

Varian's strongest selling point must be its software. Although data base management systems are being discussed, selected, or whipped into shape by software gnomes at all the minicomputer factories, few are being delivered. Only Hewlett-Packard beat Varian's version of TOTAL to the punch with its Image 2000, which is like Total in many ways.

VORTEX II is a fine operating system, rivaled only by Digital's RSX-11D and MODCOMP's MAX IV. For commercial processing, Varian offers RPG II and IV, but Digital offers COBOL and Diversified Data Systems, Inc., with Interdata's blessing, offers COBOL for the 8/32.

Over the years, Varian's biggest problem has been public relations and a discernible, consistent, or sustained marketing policy. Varian's new president appears to be bringing new stock and climate to the vineyards from which rarer, finer policies can spring and, hopefully, flourish.

The Varian hardware has been good since the company brought out 620 in the 1960s. Its current software is outstanding. If the marketing and sales forces do team up and catch up with the hardware and software, the V-70 Series will be hard to beat.

TYPICAL PRICES

Model Number	Description	Purchase Price $	Monthly Maint. $
75-1000	V-75 computer with 64K words of single-port, 800-nsec core memory	35,000	380
75-1050	V-75 computer with 64K words of single-port, 800-nsec core memory with byte parity	37,000	385
75-1200	V-75 computer with 32K words of dual-port, 400-nsec core memory and 32K words of single port, 800-nsec core memory	44,500	380
75-1250	Same as 75-1200 with byte parity	46,500	385
75-1400	V-75 computer with 32K words of dual-port, 330-nsec MOS memory and 32K words of single-port, 800-nsec core memory	48,500	435
75-1450	Same as 75-1400 with byte parity	50,500	440
75-1600	V-75 computer with 64K words of dual-port, 330-nsec MOS memory	55,000	440
75-1650	Same as 75-1600 with byte parity	57,000	440
	Core Memory		
75-2100	8K words of 450/660-nsec dual-port	3,500	33
75-2101	Same as 75-2100 with byte parity	4,000	39
75-2104	16K words of 800/990-nsec single-port	3,500	36
75-2105	Same as 75-2104 with byte parity	4,000	42
75-2400/1	32K words (4 8K-word modules) of 450-nsec, dual-port — includes slave/master memory expansion chassis and power supply	15,000	143
75-2410/1	Same as 75-2400/1 with byte parity	17,000	165
75-2420/1	64K words (4 16K-word modules) of 800-nsec, single port; includes slave/master memory expansion chassis and power supply	16,000	150
75-2430/1	64K words (4 16K-word modules) of 800-nsec, single port memory; includes memory expansion chassis and power supply	18,000	172
	Semiconductor Memory		
75-2500	8K-word dual port MOS 330-nsec cycle time	5,000	44
75-2501	Same as 75-2500 with byte parity	5,500	50
	Processor Options		
75-3100	Block transfer controller	1,500	11
75-3101	Priority interrupt module (automatic storing and vectoring of 8 levels of external interrupts)	500	6
75-3102	Buffer Interlace controller	500	6
75-3400	Floating point processor (single precision and double precision operations)	4,950	39
75-4000	256-word writable control store	3,000	22
75-4001	512-word writable control store	4,000	28
75-4002	512-word writable control store (with instruction register, writable decoder control store, writable I/O control store)	5,000	39

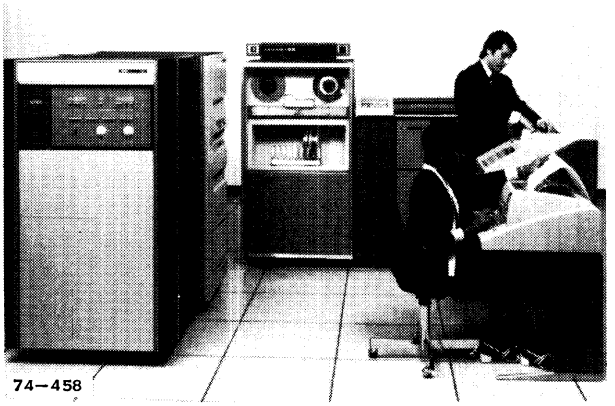
Table 1. Varian V-75 Compared to Major Competitors

Characteristics	Digital PDP-11/70	Interdata 8/32	SEL 32	Varian V-75
CENTRAL PROCESSOR				
Microprogrammed	Yes	Yes	Yes	Yes
Control Memory	ROM	ROM	ROM	ROM
No. of Registers	10 accs: 3 stack pointers; 1 PC; all 16-bit; all can be used as indexers	2 stacks of 16 32-bit gen regs std; 6 more sets opt	8:3 can be used as index regs	8:7 can be used as index regs
Word Length	16	32	32	16
Addressing				
Direct	To 64K bytes	To 1M bytes	To 512K bytes	To 4K bytes
Indirect	Single level	No	Multilevel to 16M bytes	Multilevel to 65K bytes
Indexed	Yes	Yes	Pre- and post-indexing	Pre- and post-indexing
Mapping	Yes, to 2M bytes	Yes, to 1M bytes	Yes, to 16M bytes	Yes, to 512K bytes
Instruction Set				
Implementation	Firmware	Firmware	Firmware	Firmware
Types	Single word	Single and double word	Half and full word	Single and double word
Number	400 std; 46 opt	214	152	187 std; 14 opt
Floating-Point	Hardware opt	Hardware opt	Firmware std	Hardware opt
Hardware Stack	Yes	No	No	No
Instruction Execution Times (μsec)				
Fixed Point				
Add	1.0	1.1	1.2	0.7/1.3/2.0[2]
Multiply	3.8	5.6	4.5	4.5/4.8/5.4[2]
Divide	8.3	5.7	5.1	4.8/5.2/6.0[2]
Floating-Point[1]				
Add	7.9	2.0	3.0	3.7
Multiply	9.9	3.2	4.5	6.1
Divide	10.9	5.0	8.9	8.6
Writable Control Store	No	No	No	Up to 512 x 64 bits
Interrupts				
Levels	4 lines, 8 levels	1,024	128	Up to 64
Type	Hardware	Hardware	Hardware	Hardware
MAIN STORAGE				
Type	Bipolar (cache); core (main memory)	Core	Core	Core (2 speeds); MOS
Cycle Time* (μsec)	0.24 (bipolar); 1.0 (core; 32 bits)	0.750	0.600	0.660/0.990; 0.330
Basic Addressable Unit	Word, byte	Word, half word, byte	Double word, word, half word, byte, bit	Byte, word, double word
Bytes/Access	4	4	4	2/4
Cache Memory	Bipolar, 2,048 bytes	Bipolar, 16 bytes	No	No
Capacity (bytes)				
Min	64K	131,072	32,768	131,072
Max	2M	1,048,576	1,048,576	512K
Increment Size (bytes)	64K	128K	32K	8K/16K (Core); 8K (MOS)
Ports/Module	1	1	1	1/2
Error Checks	Parity std	Parity opt	Parity: 1 bit/byte std	Parity (opt); 1 bit/byte
Memory Protection	Yes, memory management and 3 operating modes	Yes, with memory management	Yes, in pages of 512 words	Yes, in pages of 512 words
Memory Management	Yes	Yes	Yes	Yes
Interleaving	Yes, 2-way	4-way	2 reads/4 writes	2-way
INPUT/OUTPUT				
Max Devices Addressable	No limit	1,024	Via IO Crs	64
Programmed I/O	Yes (UNIBUS)	Yes	Yes, IOC	Yes, firmware
DMA	Std (UNIBUS); plus 4 high-speed data channels	Std for 112 devices	IOC	Std; high speed; PMA
DMA Transfer Rate	4M bytes/sec (UNIBUS); 5.8M bytes/sec (data channel)	6M bytes/sec	1.2M bytes/sec each; 26.7M bytes/sec aggregate	0.66M bytes/sec (std); 2M bytes/sec (high speed); 6M bytes/sec (PMA)
Price for System with 128K-byte Memory	$54,600[3]	$51,900	$43,900	$46,500[4]

Notes:

*Effective memory cycle time varies with type of memory and number of memory modules interleaved.

(1) PDP-11/70 times include operand load times. Also floating-point processor operates in parallel with central processor. Floating-point times are for 64-bit operands.
(2) Three times are for 330-nsec MOS/660-nsec core/990-nsec core.
(3) CPU bundled with console, line clock, and installation.
(4) With 64K bytes of 660-nanosecond, dual-port interleaved core memory with byte parity, 64K bytes of 990-nsec, interleaved, single-port, core memory with byte parity, keyboard/CRT console, installation, memory mapping to 512K bytes, and writable control store.



OVERVIEW

Xerox 530 is a small, fast, modular computer that is designed to handle any type of processing, from business to process control. The basic 530 model contains a central processing unit (CPU), one input/output processor (IOP) with 16 channels, and one basic 8K-word core memory module. An expanded version of the 530 can include up to seven more 8K-word memory modules, a second IOP with 12 channels, a DIO interface, two DMA interfaces, and a dual processor adapter.

The 530 is intended for multiprogramming and multiprocessing environments. Its major applications are in process control, data acquisition and applications that require some scientific processing support. Always one of Xerox's strong points, the I/O capabilities of the 530 are good for a system of its size although not as extensive as the capabilities of larger members of the series. The I/O facilities function efficiently, especially in a process control or data acquisition application where the capabilities of the processor are directed almost exclusively toward I/O control.

A dual processor adapter (DPA) can connect two 530s (but not a 530 and a Sigma Series System) in master/master or master/slave relationships which are useful for back-up processors, front ends, and shared memory banks; DPA is not yet supported under BCM and RBM operating systems, however.

The priority interrupt system handles up to 40 unique hardware interrupt levels. Interrupts are divided into internal and external categories. The priorities are hardware defined and are sorted and identified by the CPU.

Xerox offers a useful standard maintenance feature on the 530, called Remote Assist, which allows the user to link into a Xerox maintenance office through a special Teletype interface built into the CPU. A Xerox Remote Assist specialist can link into the system through this interface to interrogate the fault system, run diagnostics, and even debug programs. Communication is over the common carrier dialup network.

The 530 is supported by two real-time operating systems, three FORTRAN compiler versions, a COBOL compiler, an RPG compiler, two assemblers, sort, a substantial set of users' aids, and a large library of engineering and scientific subroutines. All of the applications packages developed for the Sigma 3 will run on the 530.

The Xerox 530 was first delivered in August 1973.

COMPETITIVE POSITION

Although completely compatible with the Sigma 3, the Xerox 530 is an architecturally different computer. It uses extensive MSI/LSI technology, a microprogrammed CPU and a different memory. In addition, the 530 has features unavailable for the Sigma 3: remote assist, floating-point hardware, and field addressing. The floating-point hardware will increase throughput dramatically over that of Sigma 3 for many applications. Field addressing allows the programmer to manipulate bits and bytes around the constraints of word boundaries for table and string processing. The field addressing hardware also provides for storing and retrieving data in pushdown stacks.

Xerox has also improved the basic 530 hardware by standardizing many Sigma 3 options. These include the memory protect feature (for foreground/background processing), several internal interrupt levels, and a comprehensive fault detection and interpretation system. The internal fault detection system, which includes a multipurpose fault register, is substantially augmented by a standard communications link to a full-time, on-call Xerox Remote Assist specialist (maintenance technician) 24 hours a day. This provision allows the user to establish a Teletype land-line link directly into a Xerox office, where the specialist can communicate with the 530 (hardware and software) for remote diagnosis. The specialist can run diagnostics, interrogate the fault system, and even debug programs — all remotely.

Xerox has reduced the number of available interrupt levels from 116 (Sigma 3) to 40, has eliminated multiple memory ports, and has gone to an internal busing technique that utilizes a fairly elaborate cycle-stealing/priority memory accessing technique. The results of these changes are difficult to evaluate, especially within the context of what Xerox is trying to achieve for the 530. Obviously, fewer interrupt levels reduce the 530's process control capabilities, and less simultaneity affects the throughput rate, even with the shorter core memory cycle time (800 nanoseconds compared to 975 nanoseconds). But all this is not necessarily bad, because it does create a price versus capabilities balance that can be a bargain for the small to medium user. Furthermore, 40 interrupts are adequate for most applications.

The 530 is aimed at enlarging the market area filled by the Sigma 3, concurrent real-time and batch processing. The 530 offers the user a substantially better

price/performance ratio, as well as COBOL and RPG. The Sigma 3, on the other hand, is still available for those users who need a more elaborate interrupt structure and more simultaneity.

Strongest competition for the Xerox 530 will come from the Digital Equipment line, specifically the PDP-11/40 and 11/45. other competing systems include the Interdata Model 80, MODCOMP II, Varian Data Machines V70 Series, Prime 300, and Hewlett-Packard 21MX. All of these systems compete across a broad range of applications.

Although the Xerox 530 system is well designed and price competitive, it does not have elaborate memory management hardware like that available for the PDP-11/40 and 11/45, or the writable control store available with some of the other systems. Writable control store, however, has limited utility for most end users. On the other hand, memory management hardware supported by a good operating system should be an asset for real-time processing. It should be pointed out, however, that the 11/40 and 11/45 require memory management to address memory beyond 28K words, while the 530 does not. The Xerox 530 has a good structure for applications requiring extensive I/O.

One of the Xerox 530's strong points is its major operating system, the Real-Time Batch Monitor (RBM), which provides for real-time foreground processing, combined with background scientific or commercial processing. RBM supports ANSI FORTRAN IV, RPG, COBOL. Xerox has had considerable experience with the RBM software and its environment. The new features of the 530 and the COBOL compiler, combined with the overall system cost should make the 530 attractive for small to medium scale users. Of the major competitors, only Digital supplies COBOL.

Xerox also supplies a Satellite Processing Package allowing the system to submit jobs to any computer using IBM's "HASP" BSC multileaving protocol. This enables the user to send jobs and receive output from Xerox CP-V IBM HASP hosts, such as IBM 1130, 1800, 360/370, UCC COPE, and other 530 systems. Remote communications are concurrent with real-time and batch processing. These facilities allow the 530 to compete in the growing distributed processing market served by both intelligent terminals and small business systems with extensive communications capabilities. In this market, the 530 competes with companies like Four-Phase, Datapoint, MDS, and Sanders, who offer large terminal systems capable of a considerable amount of local processing, as well as with established small business suppliers like Basic Four and IBM (to some extent) who have popular business systems with extensive communications capabilities. Competition is also offered by major minicomputer manufacturers like Honeywell, Univac, Digital, and many others who have minicomputer systems with the hardware and software to function both as RJE terminals and business systems.

The 530 has also been adapted to attack the data entry market, with the Interactive Data Entry package (IDEN) allowing on-line data entry from up to 64 terminals. The Intelligent Display System package simulates an IBM 3790 entry system. These allow the 530 to compete in the growing market for multiterminal shared processor (disc-based) entry systems, with a number of companies devoted to this market, like Computer Machinery and Inforex, as well as major mainframe manufacturers like Honeywell.

User Reactions

Xerox 530 users interviewed for this report were very satisfied with both the system's performance and its reliability. All users reported excellent experiences with Xerox software support and maintenance service.

A Phoenix-based manufacturer of sounding rockets and satellites has three Xerox 530s, the first one installed a year ago. They chose the 530 to replace their IBM 1130 because of increased speed. One of the systems is used for normal data processing applications, while the other two are used to track rockets in a real-time situation. This company had two Xerox 530s operating on board a ship for several months and reports that the system performed admirably even under adverse conditions.

A school district uses the Xerox 530 as a remote batch terminal in conjunction with a Xerox Sigma 9. The system was chosen as part of a bid and is being used for student accounting, budgetary accounting, grade reporting, truant tracking, and other student processing applications. Sigma 9 software is being used successfully on the 530.

In an unusual application, one Xerox 530 is being used by a California fire department to dispatch fire apparatus to areas where it is needed most. The fire department has had the system for six months and has been very satisfied with it. According to the fire chief, none of the fire department members are computer-oriented, although two people are being sent to school to learn about the 530, so Xerox has provided excellent start-up and continuing support. The fire district plans to purchase two more systems to expand its capabilities.

A scientific research organization uses the Xerox 530 for process control. The company has four 530s and has had them for one year. Each system has a 65K-word memory and a 48-megabyte moving-head disc. The systems have paper tape, punched card, magnetic tape, and printers. The firm chose the 530 because it was compatible with the Sigma 2s and 3s they had used previously; and this firm's 530s have proved more reliable than the Sigma models.

CONFIGURATION GUIDE

The overall configuration of the 530 CPU, with its standard and maximum configurations and its general internal organization, is illustrated in Figure 1.

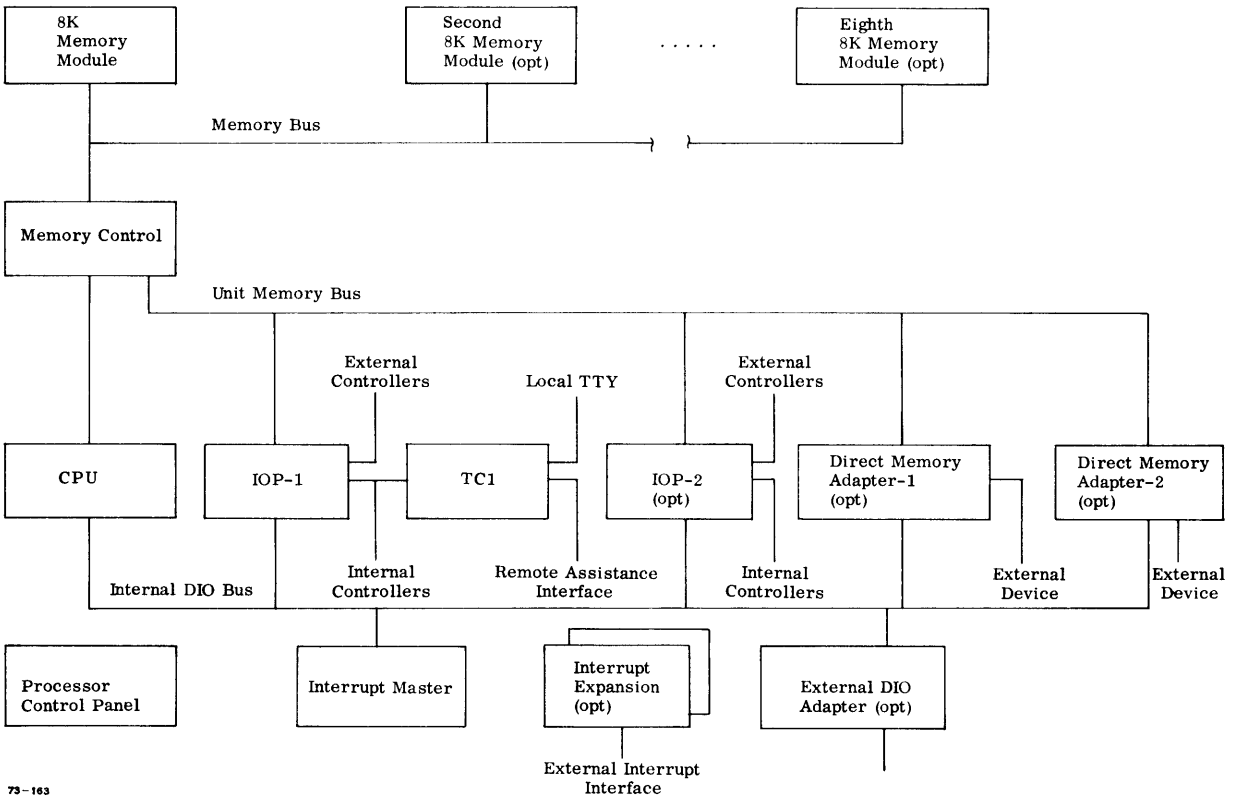


Figure 1. Xerox 530: Central System Block Diagram

Xerox sells the 530 in a basic 4101 configuration and in seven standard configurations that are considerably lower in price than the sum of the component prices.

The 4101 includes the CPU, one IOP (input/output processor) processor control panel, interrupt master, memory control, and 8K-word memory module. The IOP includes 16 I/O subchannels, and the CPU incorporates extended arithmetic (multiply/divide), two real-time clocks, fault interrupts, memory protect, power monitor, 10 internal and six external interrupt levels, and keyboard/printer control. A telecommunications controller, if included, interfaces to the IOP.

Optional features include: a second IOP with 12 subchannels, up to two direct memory access adapters, external DIO (direct input/output) adapter, up to seven additional memory modules of 8K words each (total 64K words), and Interrupt Expansion to 30 external levels. System options are available for floating-point arithmetic, field addressing, 2-byte interface on the standard or optional IOP, and dual processor adapter.

Xerox 530 mainframe characteristics are shown in Table 1.

The first eight channels of IOP-1 and the first four channels of IOP-2 can handle single- or multiunit controllers. All other channels are restricted to single-unit

Table 1. Xerox 530: Mainframe Characteristics

CENTRAL PROCESSOR	Xerox 530
Type (microprogrammed)	Yes
Control Memory	
Size	NA
Use	NA
No. of Internal Registers	8 general, 16 protection, 4 arithmetic/control
Addressing	
Direct	1,024 wds
Indirect	Forward/backward, 256 locations
Indexed	2 levels
Instruction Set	
Implementation	Hardware
Number	72 std, 10 opt
Decimal Arithmetic	No
Floating-Point Arithmetic	Yes
User Microprogramming	No
Priority Interrupt Levels	16 std; 28/40 opt
Main Storage	
Type	Core
Cycle Time (μsec)	0.8
Basic Addressable Unit	16-bit wd
Bytes/Access	2
Cache Memory	No
Min Capacity (wds)	8,192
Max Capacity (wds)	65,536
Increment Size (wds)	8,192
Ports/Module	1
Error Checks	Parity
Protection Method	Registers
Memory Management	No
ROM	No

controllers. Each multiunit channel can address up to eight controllers and up to 16 devices per controller. The theoretical device handling capacity of a Xerox 530 system with two IOPs is 144 devices. The two types of controllers cannot be mixed on a single channel.

The DIO interface can, again theoretically, address up to 65,536 separate devices through its 16-bit control word. Table 2 lists available peripheral devices.

Table 2. Xerox 530: Peripherals

Magnetic Disc. Rapid Access Data (RAD) files: capacities of 0.75, 1.5, or 3.0M bytes/storage unit; transfer rate of 188,000 bytes/sec; avg access time of 17 ms.
Removeable Disc: capacities from 24.5M to 196.6M bytes; transfer rate of 312,000 bps; avg access time of 87.5 ms.

Magnetic Tape (IBM-compatible). 7-track units (37.5 ips, transfer rates up to 20,800 bps); 9-track (75 ips, transfer rates up to 60,000 bps).

Punched Card. Reading speeds up to 200 or 400 cpm; punching speeds up to 100 cpm.

Line Printers (buffered). 310 to 1,100 lpm; up to 132 print positions; up to 91 char.

Keyboard/Printers (10 cps). Avail with paper tape reader (20 cps) and punch (10 cps).

Paper Tape. Reading speeds up to 300 cps; punching speeds up to 120 cps.

Graph Plotters. Digital incremental, drift-free plotting in 2 axes in up to 300 steps/sec at speeds from 30 millimeters to 3 ips.

Data Communications. Char-oriented and message-oriented equipment to connect remote user terminals via common carrier line, and local terminals directly.

Analog/Digital. Input/output controllers (analog and digital) IOP-DIO adapter, frequency controller, device subcontroller.

Obviously, the total device-handling capacity of the 530 can never be used completely; however, the I/O interfaces are significant indications of the multipurpose design of the 530 system architecture. Normal business/scientific data processing is supported by the IOPs and, to some extent, the DMAs. Large-scale data base manipulation and swapping require the high-speed bulk data transfer capability given by the DMAs. The DIO interface is naturally suited for process control operations.

The remaining seven standard configurations offered by Xerox are: 41C1 Paper Tape System; 41C2 Paper Tape and Card System; 41C3 Paper Tape, Card, and Printer System; 41C4 Card System; 41C5 Card and Printer System; 41C6 Card, Printer, and Magtape System; and 41C7 Card, Printer, and Magtape System (two drives).

The Xerox Interactive Data Entry Network (IDEN) for distributed processing, which runs under RBM, requires 32K words of memory, a disc, communications controller, magnetic tape unit, network of CRTs, and keyboard/printer.

The Xerox Satellite Processor package runs under RBM or BCM. Thus, it requires a configuration to support the operating system. The RBM with Satellite Processor requires ACPU, 16K words of memory, Teletype KSR 33, Disc (0.75M-byte capacity), card reader, and procedure-oriented communications controller. The BCM version requires only 8K words of memory and does not require the disc. Otherwise, the configuration is the same as for RBM.

Several processor features are interesting. Field addressing, for example, allows the processor to address up to 16 bits without regard to internal word boundaries. This useful bit and byte manipulation feature gives the 530 the ability to construct pushdown stacks and to operate on tables and strings.

External priority interrupts are expanded in two increments of 12 levels each to a maximum of 40 interrupt levels.

The Model 4185 Dual Processor Adapter (DPA) is an option that requires some changes to the CPU backplane. The changes are standard to all processors manufactured after April 1, 1974. Configurations can be either master/master or master/slave. Masters attach the DPA to communicate with DMA on a slave. Slaves can become masters by adding a DPA unit to the slave to connect to the other processor's DMA channel. A total of 64K words of memory can be addressed by either processor. All combinations of memory arrangements are possible, as long as each processor has a minimum of 8K words: 8K in the master, and 56K in the slave, 48K in the master and 16K in the slave, 32K in each, and so on.

In addition to an extensive line of standard peripherals, Xerox offers impressive analog/digital and data communication subsystems. A 530 with a fully expanded I/O system can interface to 144 peripheral devices. Most of the standard peripherals available for the rest of the Sigma line can interface to the 530. The configurations required for BCM and RBM and their supporting software are shown in Table 3.

COMPATIBILITY

The 530 is completely compatible with the Sigma 3. Unlike the Sigma 3, however, the 530 cannot share common memory with other Sigma computers or with the 550 and 560, which reduces its usefulness as a front-end processor for the larger Sigma computers. Xerox manages a reasonable degree of compatibility between the 16-bit 530 and the 32-bit 550 and 560 and Sigma

Table 3. Xerox 530: Software Systems

SOFTWARE	SYSTEM RBM(1)	BCM(2)
FORTRAN COMPILERS		
ANS FORTRAN IV	X	–
BASIC FORTRAN IV	X	–
BASIC FORTRAN	–	X
ASSEMBLERS		
Extended Symbol	X	–
Symbol	X	X
SCIENTIFIC SUBROUTINES	X	X
COMMERCIAL		
RPG Compiler	X	–
Sort	X	–
PHSORT (FORTRAN callable) Commercial Subset(3)	X	–
COBOL Compiler	X	–
IBM 1130 CONVERSION KIT	–	–
USER SYSTEM AIDS	X	X
Real-Time Debug	X	–
RAD Editor	X	–
Debug	X	X
Math Library	X	X
Concordance	X	X
Media Copy	X	X
Source Text Editor	X	X
Absolute Loader	X	X
Relocatable Loader	X	X
Plotter Handler*	X	X
RAD Handler	X	–
COC Handler	X	–
SIU Handler*	X	–
Applications Packages		
Satellite Processor	X	X
Interactive Data Entry Network (IDEN)	X	–
Civil Engineering Coordinate Geometry (COGO)	X	X
Structural Engineering System Salver (STRESS)	X	X
Heating Ventilation and Air Conditioning (HCC III) Design System	X	X
Project Control System (PCS)	X	X
UCLA Biomedical Statistical Package (BMD)	X	X
Event Oriented Simulation (GASP II)	X	X
Continuous System Simulator (CSS/3)	X	X

Notes:
(1) RBM requires 16K memory, 750K wds of RAD auxiliary storage, a RAD controller, a keyboard printer with paper tape reader/punch, and 1 interrupt level.
(2) BCM requires 8K memory, a Teletype unit, and 1 interrupt level.
(3) Available through the Xerox Users' Group Library.

Series computers through a byte-oriented interface. The source or destination computer is responsible for word assembly or partitioning to establish format consistency. The 530 can operate in a distributed processing system as an interactive remote data entry terminal communicating with a host computer such as Sigma 6 or 9, Xerox 560, or IBM Systems 360/370 via HASP BISYNC multileaving protocol.

MAINTENANCE AND SUPPORT

Xerox supplies standard maintenance and support contracts via 13 district sales and service offices and three around-the-clock remote assist centers. The 13 district offices have full spare parts inventory and are staffed by both software and system engineers. On-site maintenance contracts are available for large remote sites.

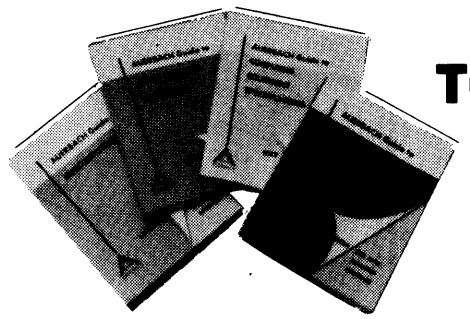
HEADQUARTERS

XEROX Corporation
701 S. Aviation Boulevard
El Segundo CA 90245

PRICE DATA

Model Number	Description	Monthly Rental $[1]	Purchase $	Monthly Maint. $
	CENTRAL PROCESSOR AND WORKING STORAGE			
	Xerox 530 Processor			
4101	Central Processor (includes first IOP with 16 I/O char, 2 real-time clocks, memory protect, power monitor, 6 levels of external interrupt, first keyboard/printer control and 8,192 wds core memory)	700	20,000	150
	Processor Options			
4105	2-Byte Interface for First IOP	50	1,500	15
4118	Floating-Point Arithmetic	167	3,500	35
4119	Field Addressing Instruction	50	1,500	15
4125	Priority Interrupt (12 levels)	20	600	5
4151	Core Memory Expansion (8,192 wds)	300	5,500	45
4170	External Interface Feature	14	400	5
4171	Second IOP with 12 I/O Channels	167	5,000	35
4175	2-Byte Interface for Second IOP (requires 4171)	50	1,500	15
4180	Direct Memory Adapter	40	1,200	10
4190	Second Keyboard/Printer Control	14	400	5
4191	Keyboard/Printer-KSR35 (requires 4101 or 4190)	110	3,300	15
4192	Keyboard/Printer-ASR35 (requires 4101 or 4190)	165	5,000	15
4193	Keyboard/Printer-KSR33 (requires 4101 or 4190)	45	1,300	15
4194	Keyboard/Printer-ASR33 (requires 4101 or 4190)	60	1,700	15
	MASS STORAGE			
7201	Rapid Access Data (RAD) Storage Controller (for 7202, 7203, and 7204 RAD units)	200	8,000	36
7202	RAD Storage Unit (0.75 Mb; 188 kb/sec transfer rate; requires 7201)	325	13,000	95
7211	RAD Controller	398	18,000	52
7212	RAD Storage Unit, 5.3 + MB	1,235	60,000	265
7240	Removable Disc Controller	500	20,000	104
7241	Extended Width Interface Feature (for 7240; 2 or 4 bytes)	63	2,500	16
7242	Removable Disc Dual Spindle Storage Unit (24.5M words; 156K word/sec transfer rate; requires 7240)	800	25,000	281
7243	Device Pooling Feature (for 7242)	200	8,000	52
7244	Disc Pack (for 7242 or 7246)	31	600	NC
7246	Removable Disc Single Spindle Storage Unit (12.2M words; 156K word/sec transfer rate; requires 7240)	450	15,000	212
7250	Cartridge Disc Control (requires IOP)	200	8,000	35
7251	Cartridge Disc, 2.3Mb (requires 7250)	140	5,500	50
7252	Cartridge Disc, 4.6Mb (requires 7250)	225	9,000	75
	Paper Tape			
7060	7062 Reader, 7063 Punch, 7064 Spooler with 7061 Controller and Rack (requires IOP)	200	11,000	90
7062	Reader (300 cps; requires 7061)	50	2,000	16
7063	Punch (120 cps; requires 7061)	63	2,500	27
7064	Spooler	38	1,500	11
	Punched Card			
7121	Reader (200 cpm)	220	7,500	55
7122	Reader (400 cpm)	400	12,000	127
7165	Punch (100 cpm)	490	19,600	140
	Buffered Line Printer			
3451	350 lpm, 64-Char Set	500	22,000	250
7441	1,100 lpm, 64-Char Set	1,250	46,000	292
7442	1,100 lpm, 91-Char Set	1,250	50,000	292
	Magnetic Tape			
7315	Mag Tape Controller (with 1 7316 drive; requires IOP); Max 1 Controller/CPU	600	16,000	200
7316	Add-On Tape Drive; Max Drives/Controller (requires 7315)	450	12,000	180
7361	Mag Tape Controller (for 7362)	150	6,000	42
7362	Mag Tape Unit (37.5 ips, 556 bpi)	475	19,000	133
	Display Equipment			
7530	11-In. Graph Plotter	325	13,000	80
7531	30-In. Graph Plotter	550	22,000	106
7601	Data Set Controller	175	7,000	36
7602	Full-Duplex Feature (requires 7601)	20	800	NC
7603	Automatic Dialing Feature (requires 7601)	20	800	NC
7604	Local Batch Terminal Controller	210	8,400	36
7605	Procedure-Oriented Data Set Controller (requires IOP)	230	9,500	50
7611	Communications Controller	253	10,500	47

Note:
(1) Rental prices are based on a 1-year lease.
NC No Charge.



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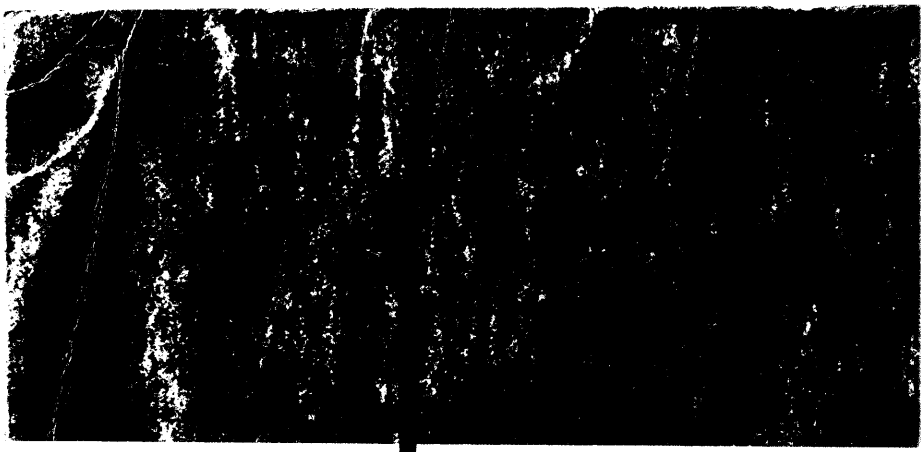

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