

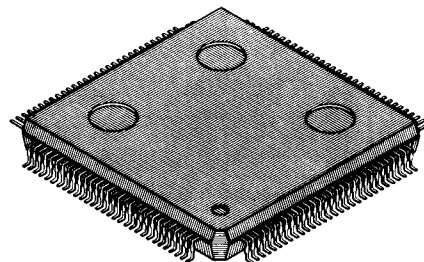
## Integrated Peripheral For PC/AT™ Systems

### INTEGRATED PERIPHERAL FOR PC/AT™ SYSTEMS

The MB89396 is a highly integrated cost-effective peripheral controller for PC/XT and PC/AT enhanced personal computers based on the 80286 and 80386 microprocessors. The MB89396 integrates two DMA controllers, two interrupt controllers, one interval timer, plus DMA address latches, chip select logic and bus interface, thus offering an efficient and flexible system solution.

- Integrates:
  - 2 MB89237A (DMA Controller)
  - 2 MB89259A (Interrupt Controller)
  - 1 MB89254 (Interval Timer)
  - DMA Controller Address latches
  - Chip Select Logic
  - Bus Interface Logic
- 8MHz Operation
- Low-Power CMOS process
- 5V Single power supply
- 120-Pin Flatpak

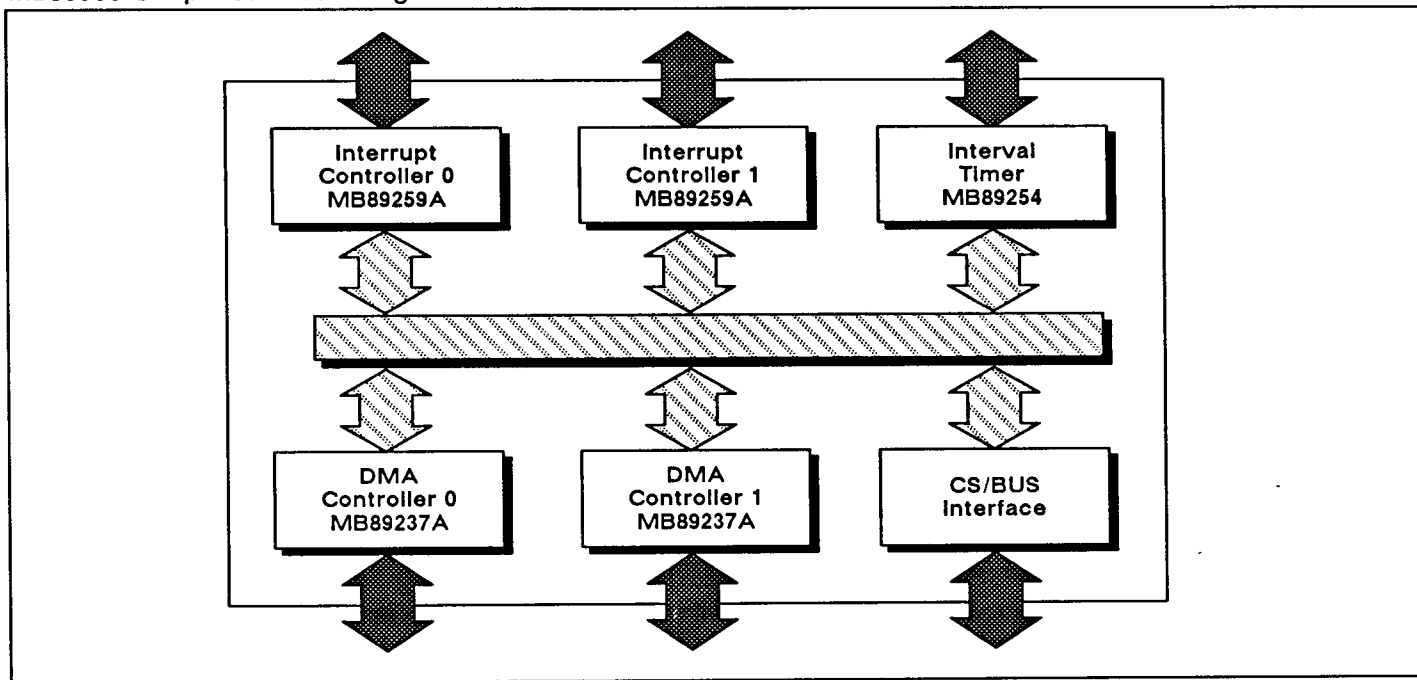
**ADVANCE  
INFORMATION**



**PLASTIC PACKAGE  
FPT-120P-M01**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

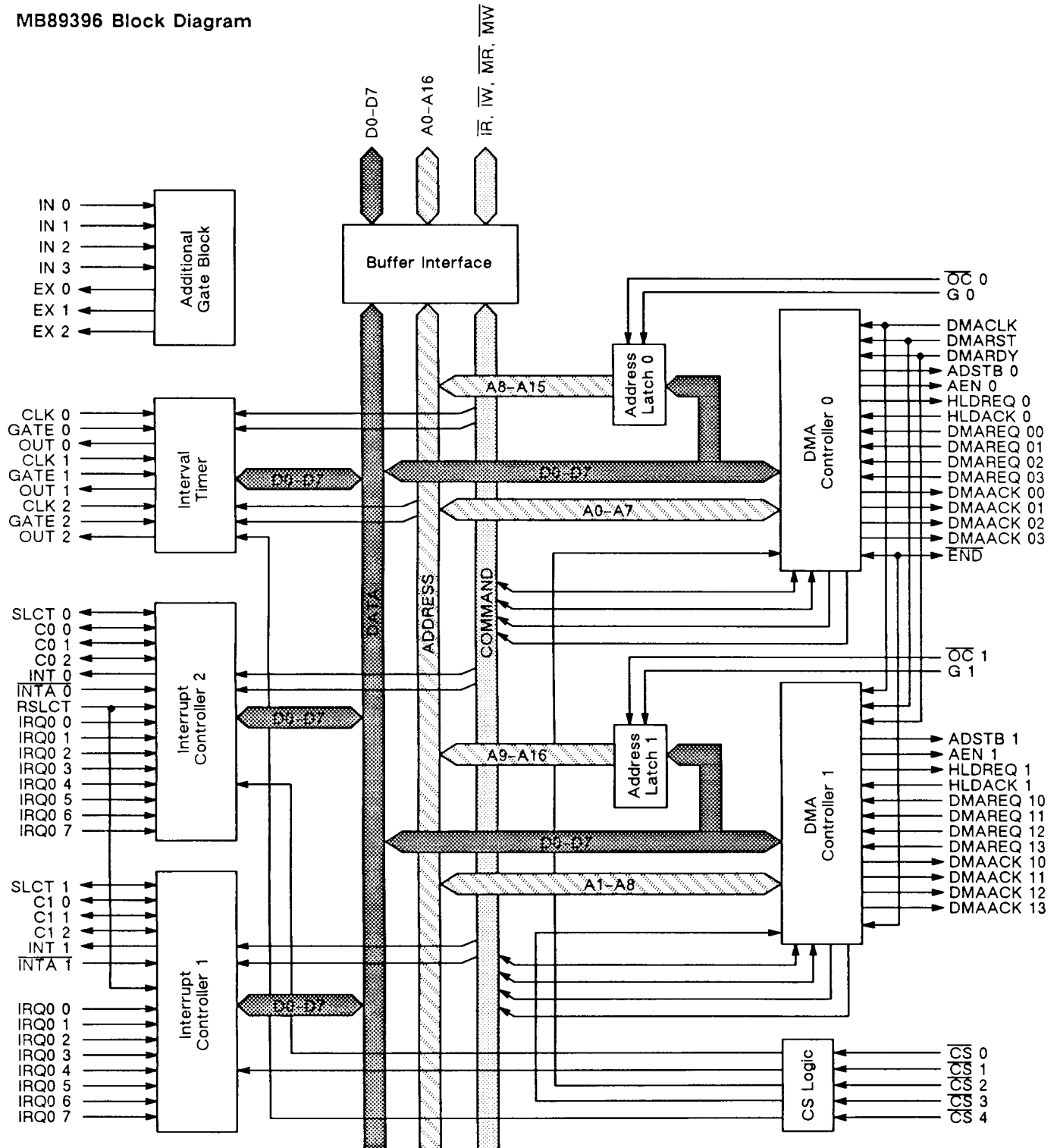
### MB89396 Simplified Block Diagram



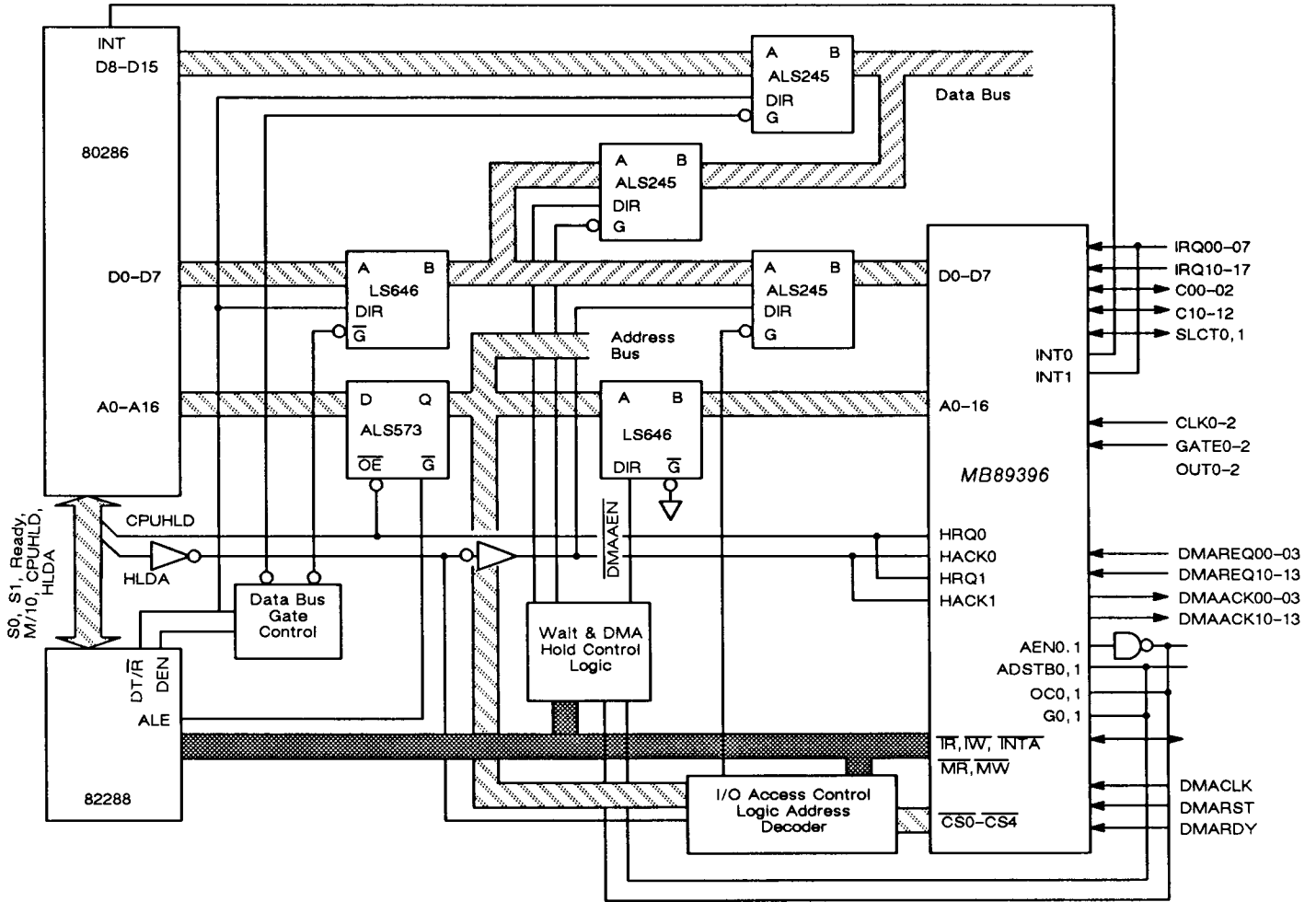
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# MB89396

MB89396 Block Diagram



**MB89396 Typical System Application**

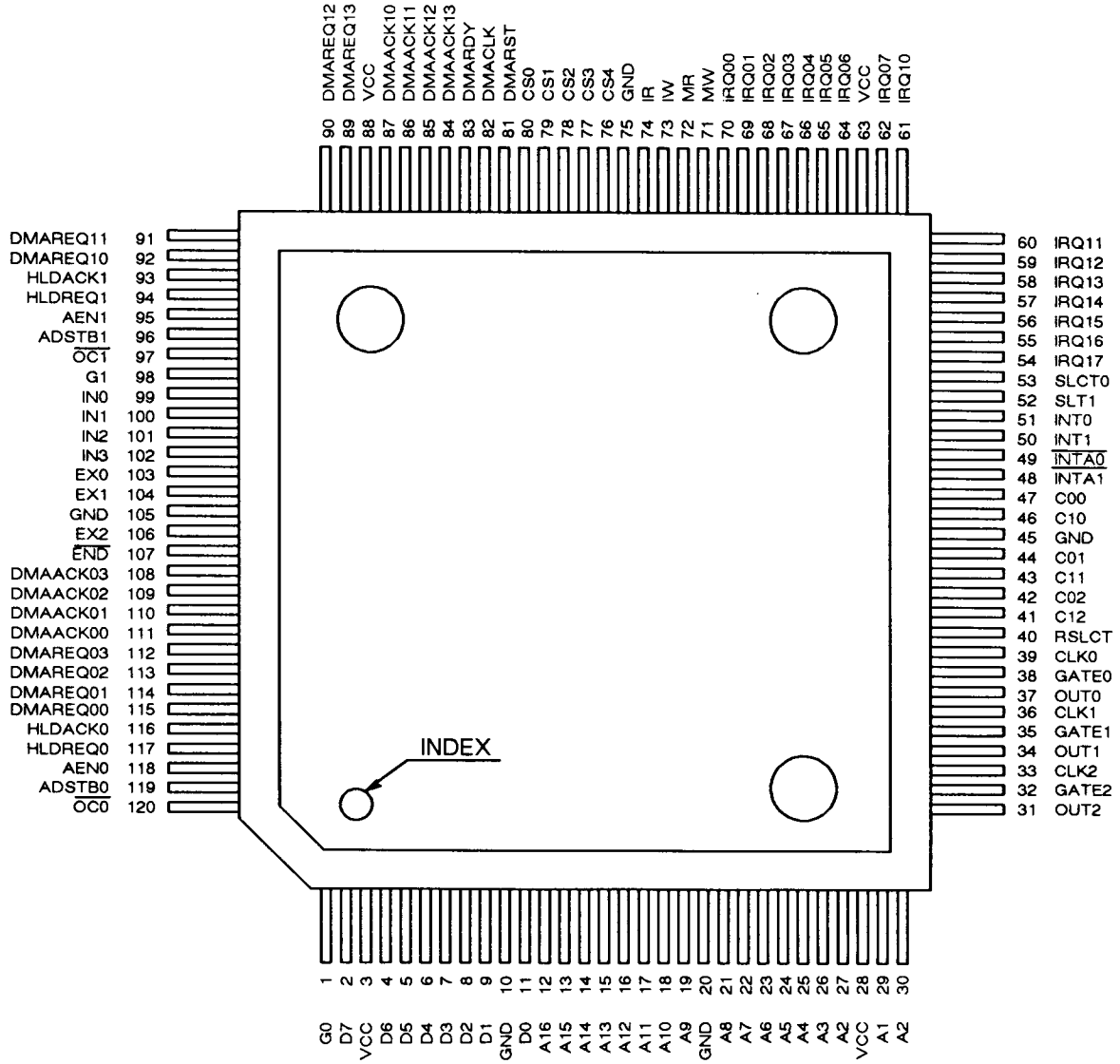


# MB89396

## PIN ASSIGNMENTS

PIN #	I/O	PIN NAME	PIN #	I/O	PIN NAME	PIN #	I/O	PIN NAME	PIN #	I/O	PIN NAME
1	I	G0	31	O	OUT2	61	I	IRQ10	91	I	DMAREQ11
2	I/O	D7	32	I	GATE2	62	I	IRQ07	92	I	DMAREQ10
3	-	VCC	33	I	CKLK2	63	-	VCC	93	I	HLDACK1
4	I/O	D6	34	O	OUT1	64	I	IRQ06	94	O	HLDREQ1
5	I/O	D5	35	I	GATE1	65	I	IRO05	95	O	AEN1
6	I/O	D4	36	I	CLK1	66	I	IRQ04	96	O	ADSTB1
7	I/O	D3	37	O	OUT0	67	I	IRQ03	97	I	$\overline{OC1}$
8	I/O	D2	38	I	GATE0	68	I	IRQ02	98	I	G1
9	I/O	D1	39	I	CLK0	69	I	IRQ01	99	I	IN0
10	I/O	GND	40	I	RSLCT	70	I	IRQ00	100	I	IN1
11	I/O	D0	41	I/O	C12	71	O	$\overline{MW}$	101	I	IN2
12	O	A16	42	I/O	C02	72	O	$\overline{MR}$	102	I	IN3
13	O	A15	43	I/O	C11	73	I/O	$\overline{IW}$	103	O	EX0
14	O	A14	44	I/O	C01	74	I/O	$\overline{TR}$	104	O	EX1
15	O	A13	45	-	GND	75	-	GND	105	-	GND
16	O	A12	46	I/O	C10	76	I	$\overline{CS4}$	106	O	EX2
17	O	A11	47	I/O	C00	77	I	$\overline{CS3}$	107	I/O	$\overline{END}$
18	O	A10	48	I	$\overline{INTA1}$	78	I	$\overline{CS2}$	108	O	DMAACK03
19	O	A9	49	I	$\overline{INTA0}$	79	I	$\overline{CS1}$	109	O	DMAACK02
20	-	GND	50	O	INT1	80	I	$\overline{CS0}$	110	O	DMAACK01
21	O	A8	51	O	INT0	81	I	DMARST	111	O	DMAACK00
22	O	A7	52	I/O	SLCT1	82	I	DMACK	112	I	DMAREQ03
23	O	A6	53	I/O	SLCT0	83	I	DMARDY	113	I	DMAREQ02
24	O	A5	54	I	IRQ17	84	O	DMAACK13	114	I	DMAREQ01
25	I/O	A4	55	I	IRQ16	85	O	DMAACK12	115	I	DMAREQ00
26	I/O	A3	56	I	IRQ15	86	O	DMAACK11	116	I	HLDACK0
27	I/O	A2	57	I	IRQ14	87	O	DMAACK10	117	O	HLDREQ0
28	-	VCC	58	I	IRQ13	88	-	VCC	118	O	AEN0
29	I/O	A1	59	I	IRQ12	89	I	DMAREQ13	119	O	ADSTB0
30	I/O	A0	60	I	IRQ11	90	I	DMAREQ12	120	I	$\overline{OC0}$

**MB98396 PINOUT**



# MB89396

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>CC</sub>	-0.3 - +7.0	V
Input Voltage	V <sub>IN</sub>	-0.3 - V <sub>CC</sub> +0.3	V
Output Voltage	V <sub>OUT</sub>	-0.3 - V <sub>CC</sub> +0.3	V
Operating Temp.	T <sub>a</sub>	0 - +70	°C
Storage Temp.	T <sub>stg</sub>	-55 - +150	°C

### Recommended Operating Conditions

Parameter	Symbol	Rating
Supply Voltage	V <sub>CC</sub>	+5. V ±10%
	V <sub>SS</sub>	0 V
Operating Temp.	T <sub>a</sub>	0°C - +7.0 °C

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics** ( $V_{CC} = 5V \pm 10\%$ ,  $GND=0V$ ,  $0^{\circ}C \leq STA \leq +70^{\circ}C$ )

Parameter		Symbol	Condition	Min.	Max.	Unit
Supply Current	Active	$I_{CC}$	Output open $V_{IH}=V_{CC}$ $V_{IL}=GND$		35	mA
	Standby	$I_{P/sB}$	Clock Inactive $V_{IH}=V_{CC}$ $V_{IL}=GND$		60	$\mu A$
Input leakage current	Input	$I_{ILKR}$	$0V < V_{IN} < V_{CC}$	-200	10	$\mu A$
	Others	$I_{ILK}$	$0V < V_{IN} < V_{CC}$	-10	10	$\mu A$
Output leakage current		$I_{OFL}$	$0V < V_{IN} < V_{CC}$	-10	10	$\mu A$
Input "L" Voltage		$V_{IL}$		-0.3	0.8	V
Input "H" Voltage		$V_{IH}$		2.2	$V_{CC} + 0.3$	V
Output "L" Voltage		$V_{OL}$	$I_{OL} = 2.5 \text{ mA}$		0.45	V
Output "H" Voltage		$V_{OH}$	$I_{OH} = 2.5 \text{ mA}$	3.0		V
			$I_{OH} = 100 \mu A$	$V_{CC} - 0.4$		V

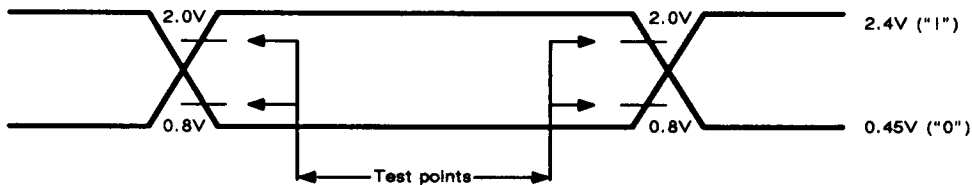
# MB89396

## AC CHARACTERISTICS

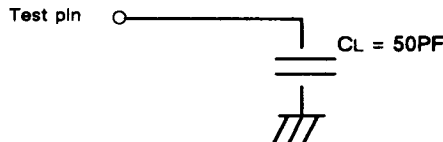
Interrupt Controller [COMPATIBLE WITH MB89259A] ( $V_{CC} = 5V \pm 10\%$ ,  $GND=0V$ ,  $0^{\circ}C \leq T_A \leq +70^{\circ}C$ )

Parameter	Symbol	Value	
		Min.	Max.
Write pulse width	TWT	100	
Address set up time (to $\overline{W}$ "L" )	TADWT	0	
Address hold time (to $\overline{W}$ "H" )	TWTAD	0	
Data set up time (to $\overline{W}$ "L" )	TDTWT	100	
Data hold time (to $\overline{W}$ "H" )	TWTDT	0	
Read pulse width	TRD	150	
Address set up time (to $\overline{R}, \overline{INTA}$ "L" )	TADRD	0	
Address hold time (to $\overline{R}, \overline{INTA}$ "H" )	TRDAD	0	
$\overline{R}$ "L" $\rightarrow$ Data access	TRDDT		120
$\overline{R}$ "H" $\rightarrow$ DB float delay	TDTRD	10	85
Address valid $\rightarrow$ data access	TADDT		200
$\overline{R}$ "L" $\rightarrow$ $\overline{EN}$ valid (SLCT pin output)	TRDEN1		100
$\overline{R}$ "H" $\rightarrow$ $\overline{EN}$ valid (SLCT pin output)	TRDEN2		150
IRQ Input width	TIRQ	100	
IRQ delay output	TIRQDL		270
Cascade valid from $\overline{INTA}$ (master)	TINTACAS		290
Cascade set up before $\overline{INTA}$ (slave)	TCASINTA	30	
Cascade valid to valid data (slave)	TCASDT		200
Write operation precharge time	TRVW	120	
Read operation precharge time	TRVR	120	
Control signals precharge time	TRVC	250	

### AC test wave form



### AC test load circuit



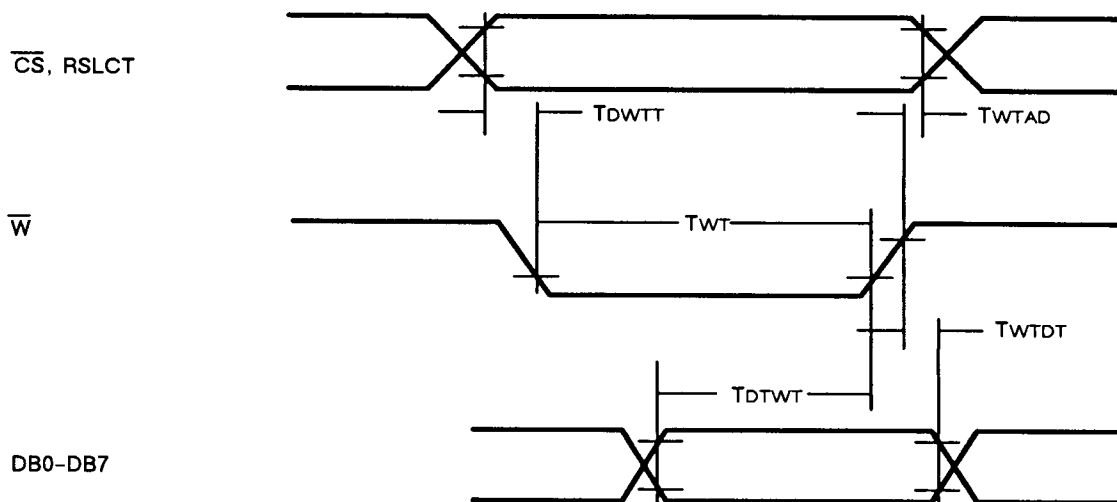
CL contains the capacitance of probe as well



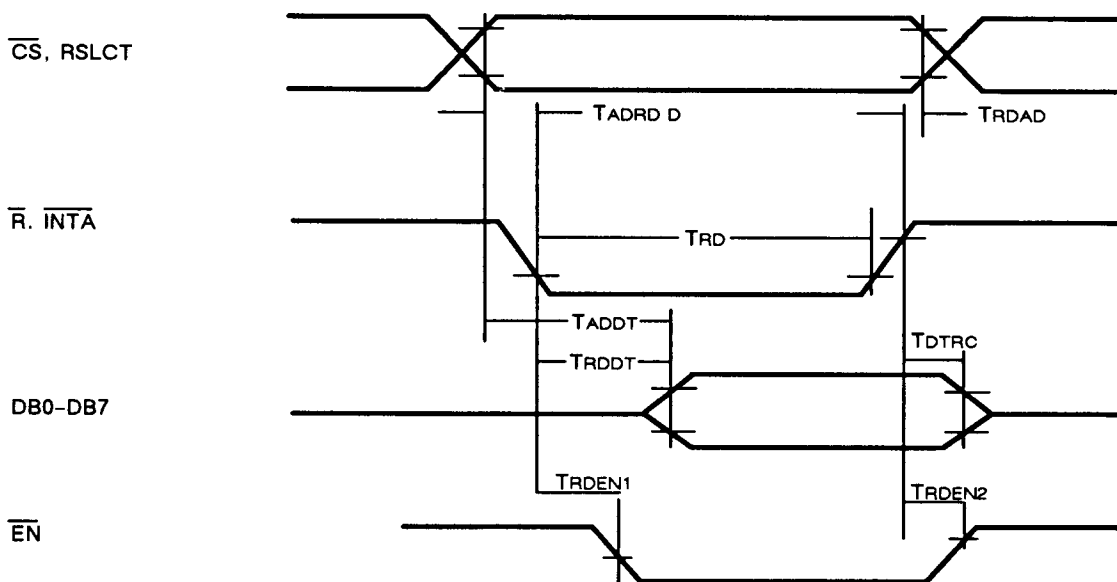
**AC CHARACTERISTICS**

**Interrupt Controller Timing**

**Write mode**



**Read and INT response mode**



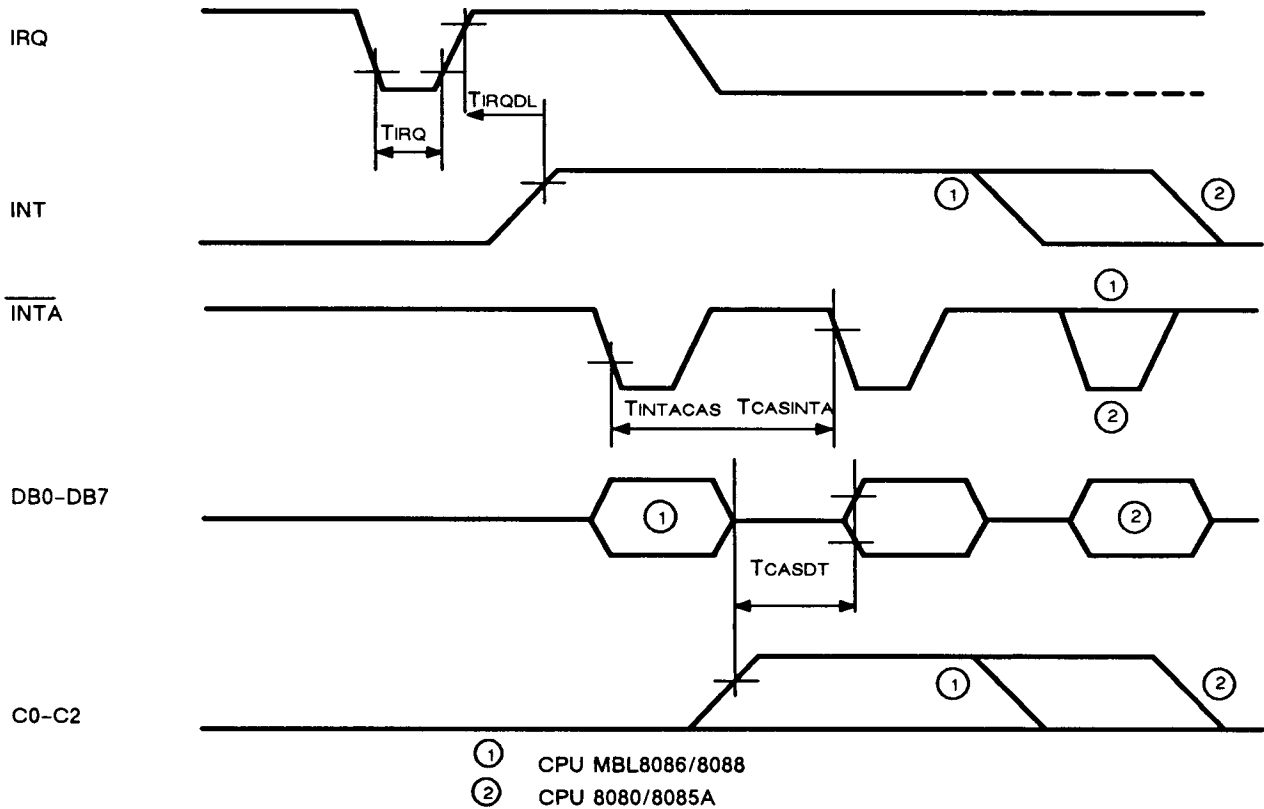
$\overline{EN}$ : SLCT  
EH: Buffer enable for SLCT

# MB89396

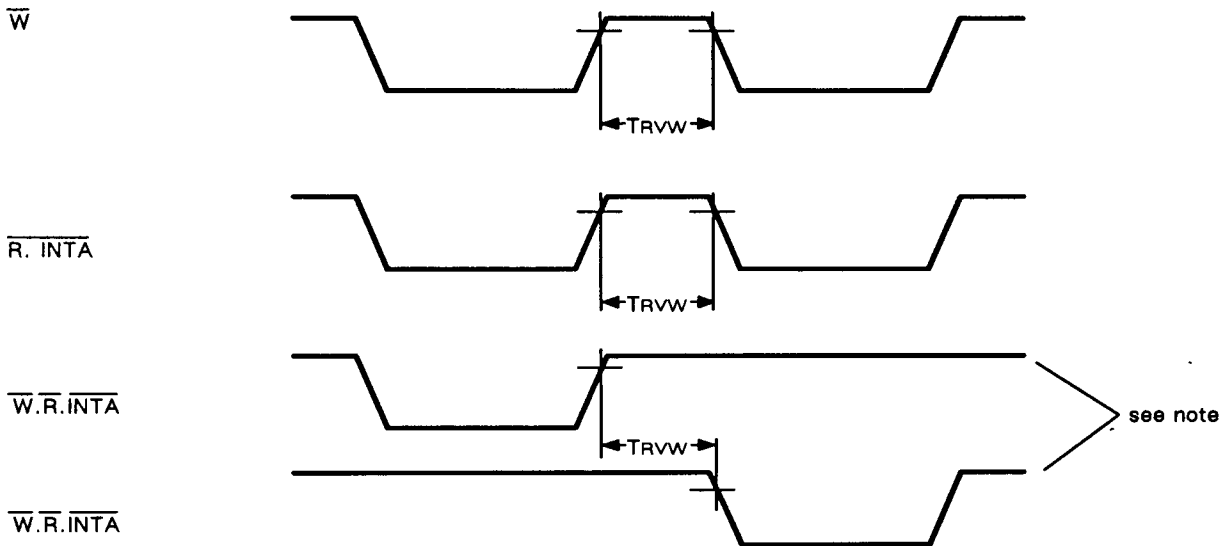
## AC CHARACTERISTICS

### Interrupt Controller Timing

Interrupt sequence mode



### Other Timings

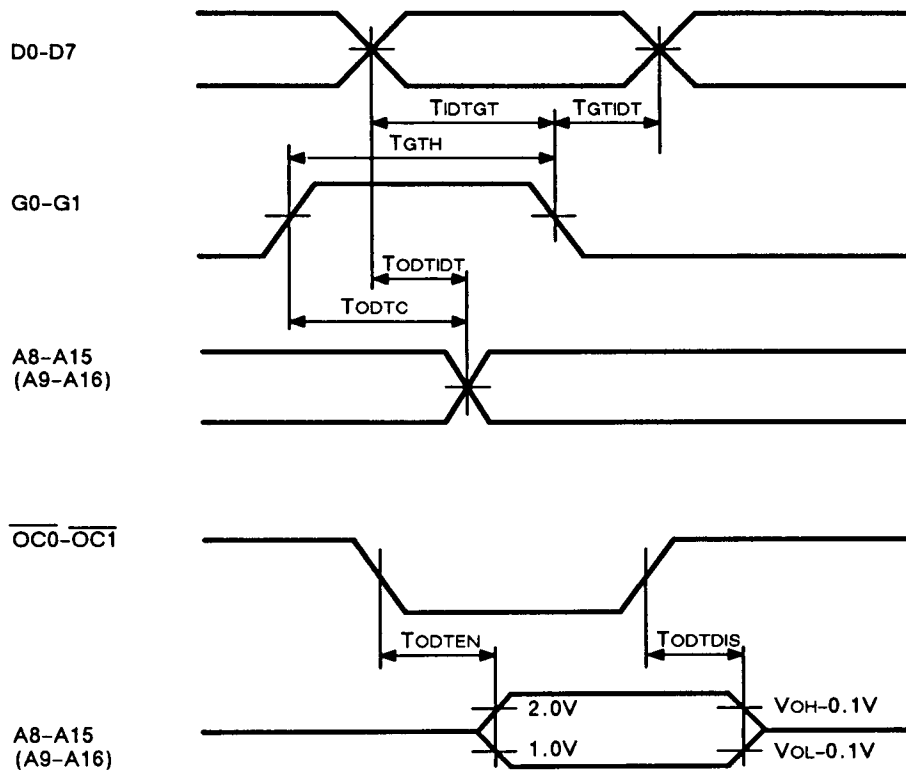


Note: If "waveform -1" is for write, then "waveform -2" is for read cycle, and vice versa.

**AC CHARACTERISTICS**

Address Latch  $V_{CC}=5V\pm 10\%$ ,  $GND=0V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$

Parameter	Symbol	Value		Unit
		Min	Max	
Input data set up time (to GT signal)	tODTDIS	5	30	ns
Input data hold time (to GT signal)	tODTEN	10	40	ns
Gate pulse width	tODTC	10	45	ns
Output data delay time (to data input)	tOUTIDT	5	35	ns
Output data delay time (to GT signal)	tGTH	15	—	ns
Output data enable time	tGTIDT	25	—	ns
Output data disable time	tIDTGT	0	—	ns



# MB89396

## AC CHARACTERISTICS

DMA Controller [Compatible with MB89237A]

Master Mode  $V_{CC}=5V \pm 10\%$ ,  $GND=0V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$

Parameter	Symbol	Min	Max	Unit
CLK Cycle Time	Tck	125		
CLK High Time (Transition $\leq 10$ ns)	Tckh	40		
CLK Low Time (Transition $\leq 10$ ns)	Tckl	60		
DMAREQ Setup Time (-> S1 CLK Low)	Tdreqs1	20		
DMAREQ Setup Time (-> S4 CLK Low)	Tdreqs2	20		
CLK High -> HLDREQ Valid Delay Time	Threq1		85	
	Threq2		85	
HLDACK Setup Time (-> CLK High)	Thack	50		
CLK High -> Address Active Delay Time	Tadd		100	
CLK High -> Address Float Delay Time	Tadfd		80	
Address Hold Time (-> W High)	Tadhwt	Tck-40		
Address Hold Time (-> R High)	Tadhrd	Tck-60		
CLK Low (S1) -> AEN High Delay Time	Tae1		100	
CLK High (S1) -> AEN Low Delay Time	Tae2		70	
CLK High -> Address Stable	Tadstb		100	
CLK High -> ADSTB High Delay Time	Tsthdl		80	
CLK High -> ADSTB Low Delay Time	Tstld1		70	
DB Setup Time (-> ADSTB Low)	Tdtastb	40		
DB Hold Time (-> ADSTB Low)	Tstdts	20		ns
CLK High -> DB Active Delay Time	Ttdtl		110	
CLK High -> DB Float Delay Time	Tdtf		120	
CLK Low -> DMAACK Valid Delay Time	Tdack1		140	
CLK Low -> DMAACK Low Delay Time	Tdack2		140	
CLK High -> R or W Low Delay Time	Trdwtdl		100	
CLK High (S4) -> R High Delay Time	Trddl		100	
CLK High (S4) -> W High Delay Time	Twt dl		75	
CLK High -> R or W Float	Tpf		80	
CLK High -> R or W Active	Tpdl		80	
Input Data Hold Time (-> MR High)	Tidth	0		
Input Data Setup Time (-> MR High)	Tidts	90		
Output Data Hold Time (-> MW High)	Todth	10		
Output Data Valid -> MW High	Todtv	65		
END Pulse Width	Tend	100		
END Low Setup Time (-> CLK Low)	Tends	25		
CLK High -> END High Delay Time	Tendh		90	
CLK High -> END Low Delay Time	Tendl		90	
READY Hold Time (-> CLK Low)	Trdyh	20		
READY Setup Time (-> CLK Low)	Trdys	40		

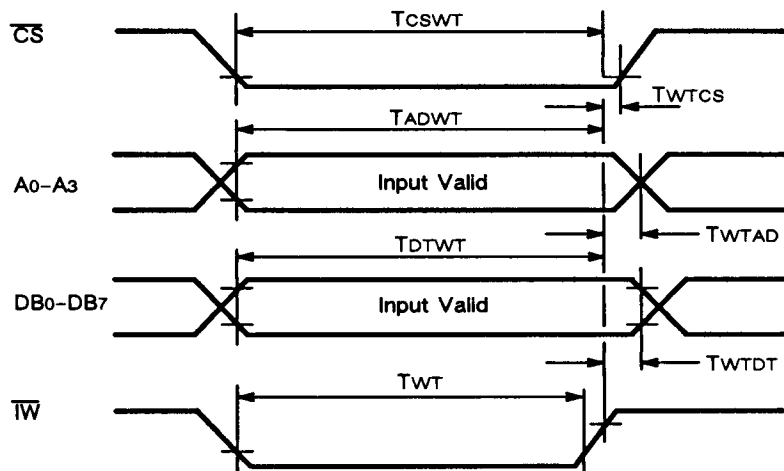
**AC CHARACTERISTICS**

DMA Controller

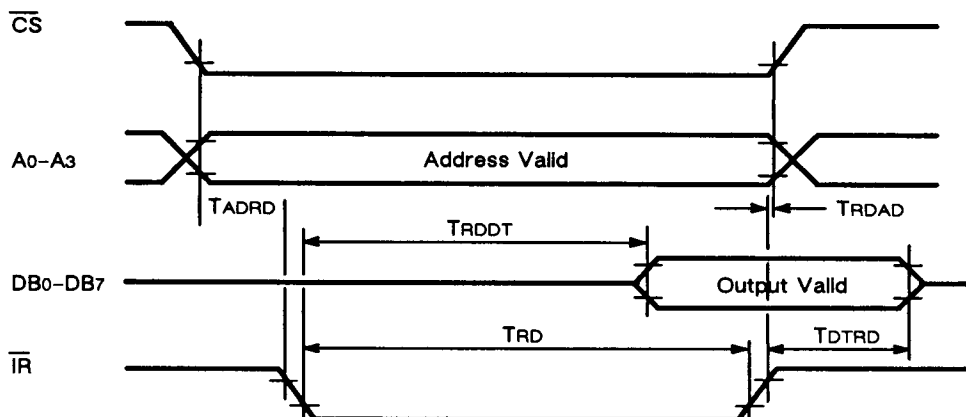
Slave Mode  $V_{CC} = +5V \pm 10\%$ ,  $GND = 0V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$

Parameter	Symbol	Min	Max	Unit
CS Low Setup Time (-> IW High)	Tcswt	90		ns
CS High Hold Time (-> IW High)	Twtcs	15		ns
Address Valid Setup Time (-> IW High)	Tadwt	80		ns
Address Hold Time (-> IW High)	Twtad	15		ns
Data Valid Setup Time (-> IW High)	Tdtwt	80		ns
Data Hold Time (-> IW High)	Twtadt	20		ns
IW Pulse Width	Twt	90		ns
Address Valid or CS Los -> IR Low	Tadrd	35		ns
Address or CS Hold Time (-> IR High)	Trdad	0		ns
IR Low -> Data Access	Trddt		120	ns
IR High -> DB Float	Tdtrd	0	80	ns
IR Pulse Width	Trd	150		ns
RST Pulse Width	Treset	200		ns
Power Supply High Setup Time (-> RST Low)	Tresetp	500		ns
RST -> First IR or IW	Tresets	2Tck		ns

Slave mode write



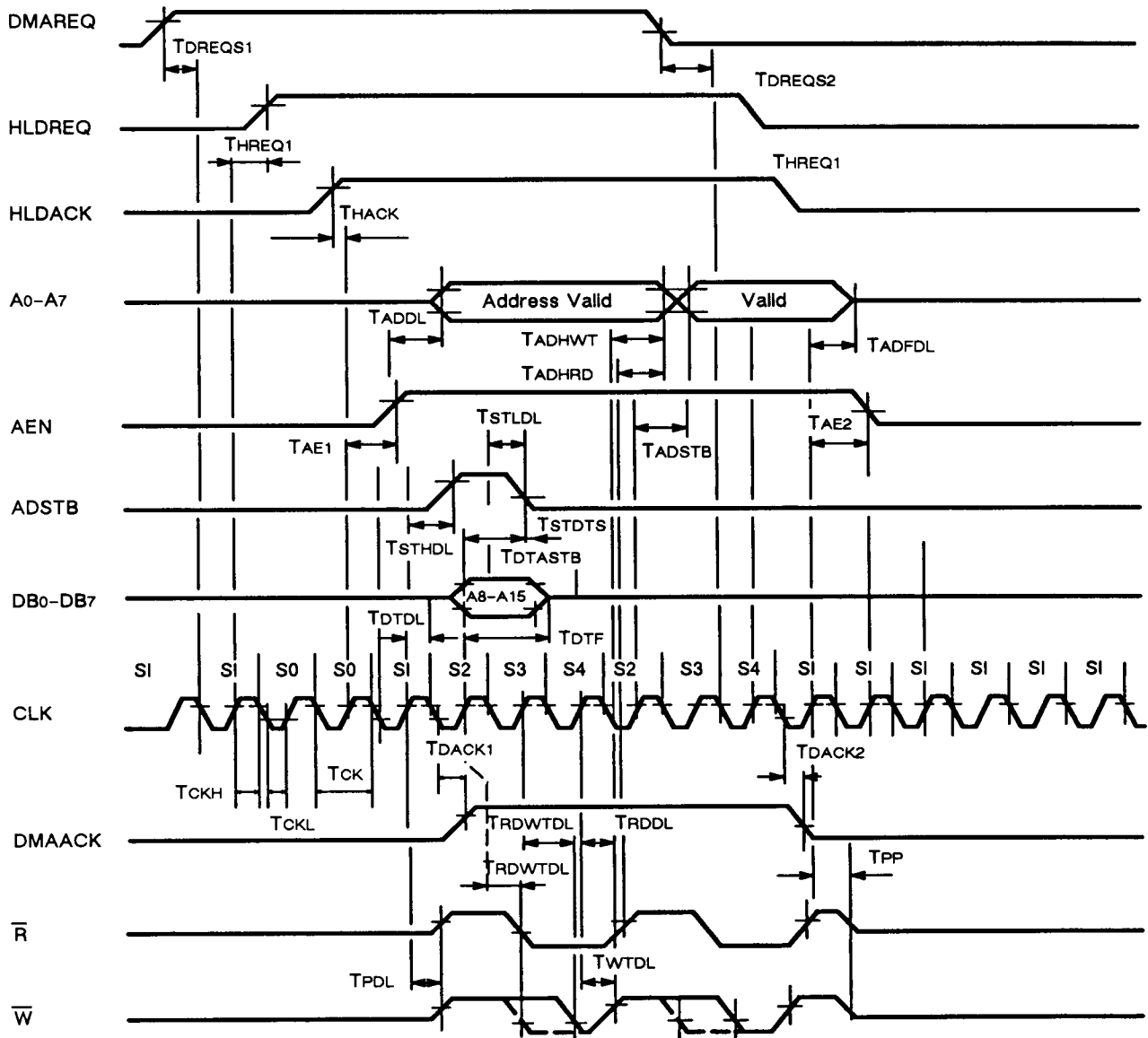
Slave mode read



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## AC CHARACTERISTICS DMA Controller Timing

DMA transfer

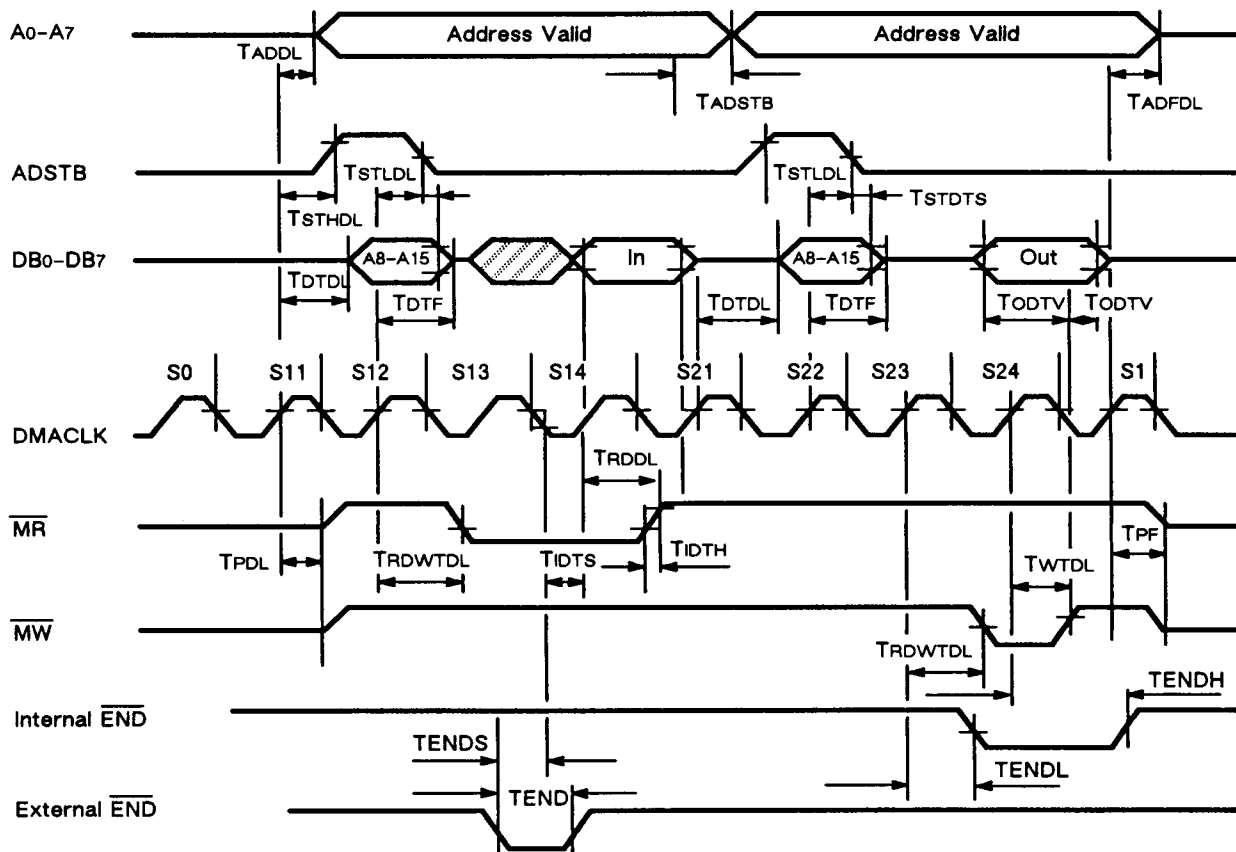


$\bar{R}$  :  $\bar{I}\bar{R}$  or  $\bar{M}\bar{R}$ ,  $\bar{W}$  :  $\bar{I}\bar{W}$  or  $\bar{M}\bar{W}$   
Broken lines show the case of extended write

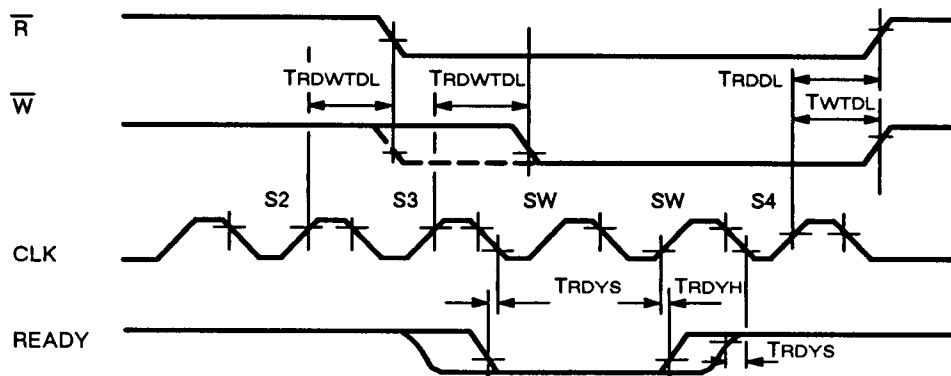
**AC CHARACTERISTICS**

DMA Controller Timing

**Memory-to-memory transfer**



**Not ready**



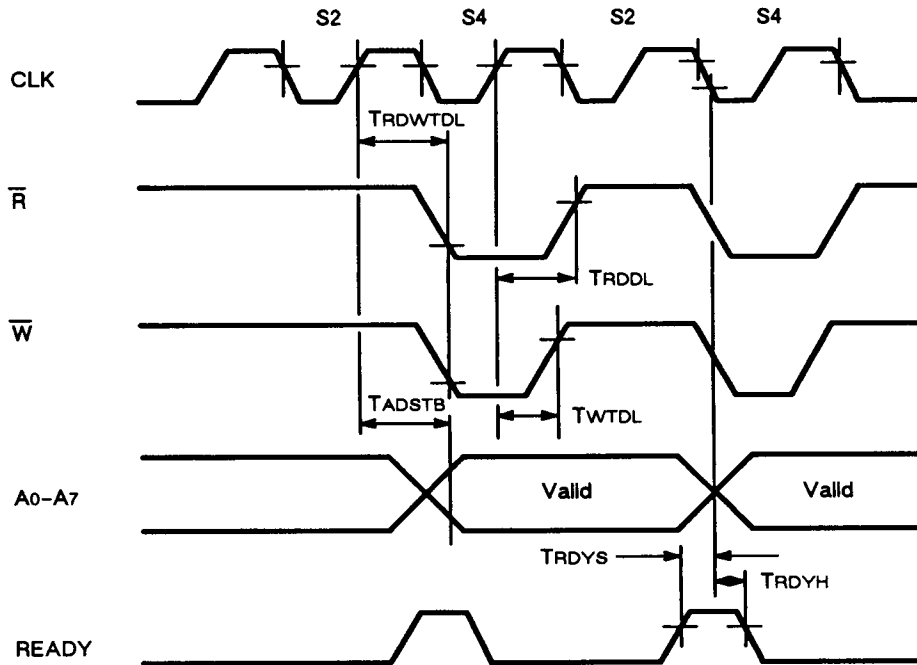
$\bar{R}$  :  $\bar{I}\bar{R}$  or  $\bar{M}\bar{R}$ ,  $\bar{W}$  :  $\bar{I}\bar{W}$  or  $\bar{M}\bar{W}$   
Broken lines show the case of extended write

# MB89396

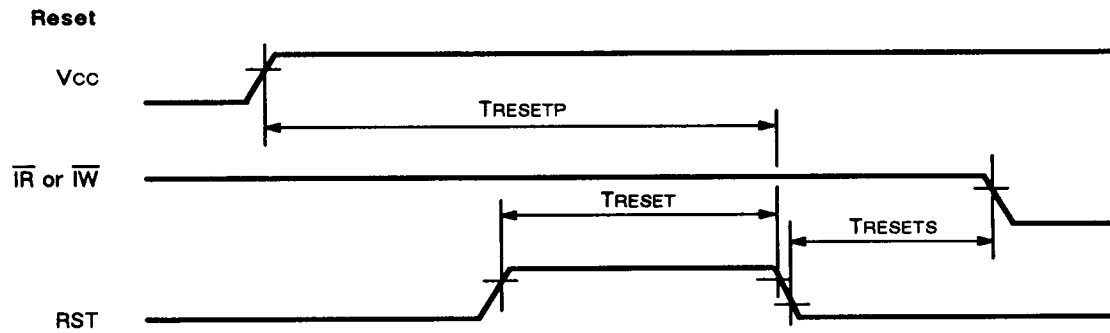
## AC CHARACTERISTICS

### DMA Controller Timing

#### Compress transfer



$\overline{R}$  :  $\overline{IR}$  or  $\overline{MR}$ ,  $\overline{W}$  :  $\overline{IW}$  or  $\overline{MW}$



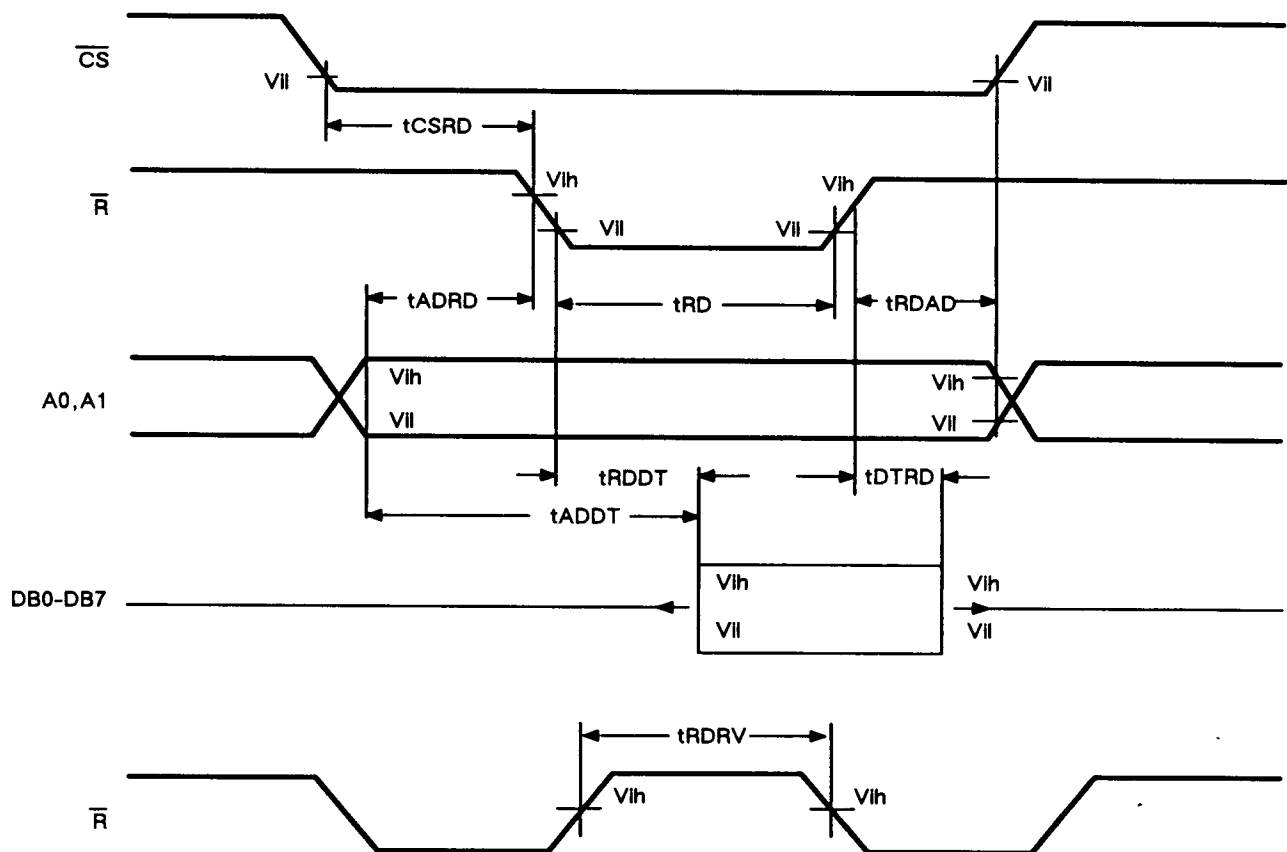


## AC CHARACTERISTICS

Interval Timer [Compatible with MB89254]

Read Timing  $V_{CC}=5V \pm 10\%$ ,  $GND=0V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ ,  $C_L=150pf$

Parameter	Symbol	Min	Max	Unit
$\bar{R}$ pulse width	tRD	150		ns
$\overline{CS}$ setup time to $\bar{R}$ falling edge	tCSR D	0		ns
Address setup time to $\bar{R}$ falling edge	tADR D	45		ns
Address hold time from $\bar{R}$ rising edge	tRDAD	0		ns
Data valid delay time from address valid	tADD T		220	ns
Data valid delay time from $\bar{R}$ falling edge	tRDD T		120	ns
Data hold time from $\bar{R}$ rising edge	tDTR D	5	90	ns
Read recovery time	tRDR V	200		ns



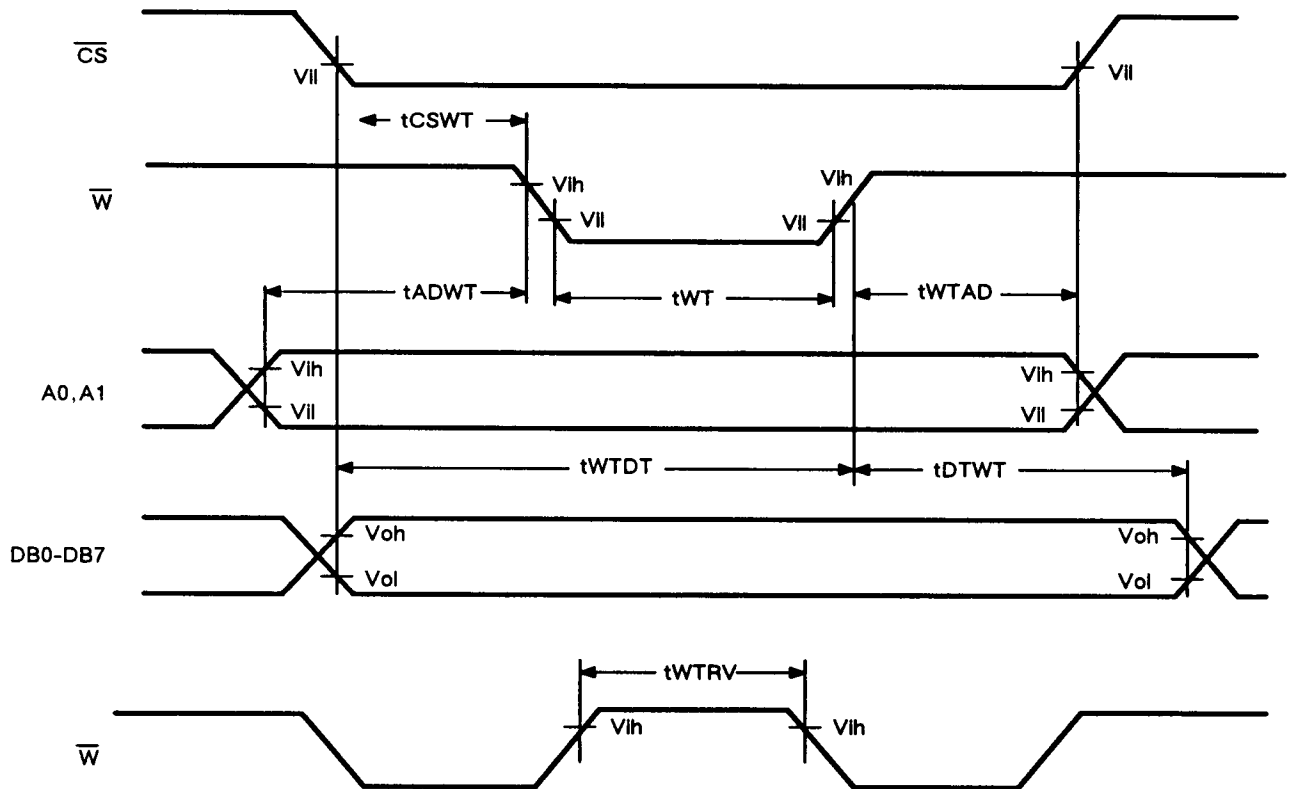
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## AC CHARACTERISTICS

### Interval Timer

Write Timing  $V_{CC}=5V\pm 10\%$ ,  $GND=0V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$ ,  $C_L = 50 \text{ pF}$

Parameter	Symbol	Min	Max	Unit
W pulse width	tWT	150		ns
CS setup time to W falling edge	tCSWT	0		ns
Address setup time to W falling edge	tADWT	0		ns
Address hold time from W rising edge	tWTAD	0		ns
Data setup time to W rising edge	tWTDT	100		ns
Data hold time from W rising edge	tDTWT	0		ns
Read recovery time	tWTRV	200		ns

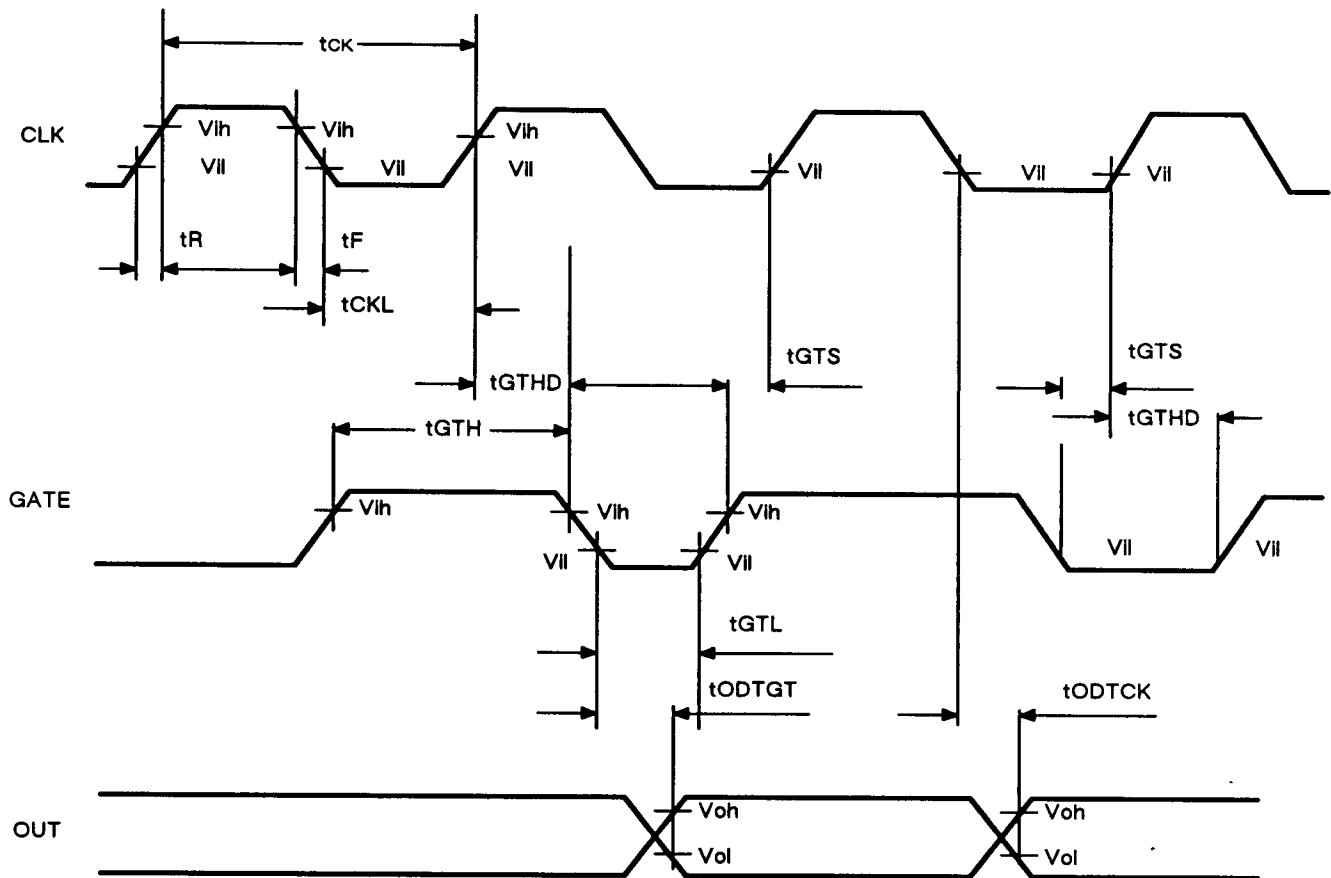


**AC CHARACTERISTICS**

Interval Timer

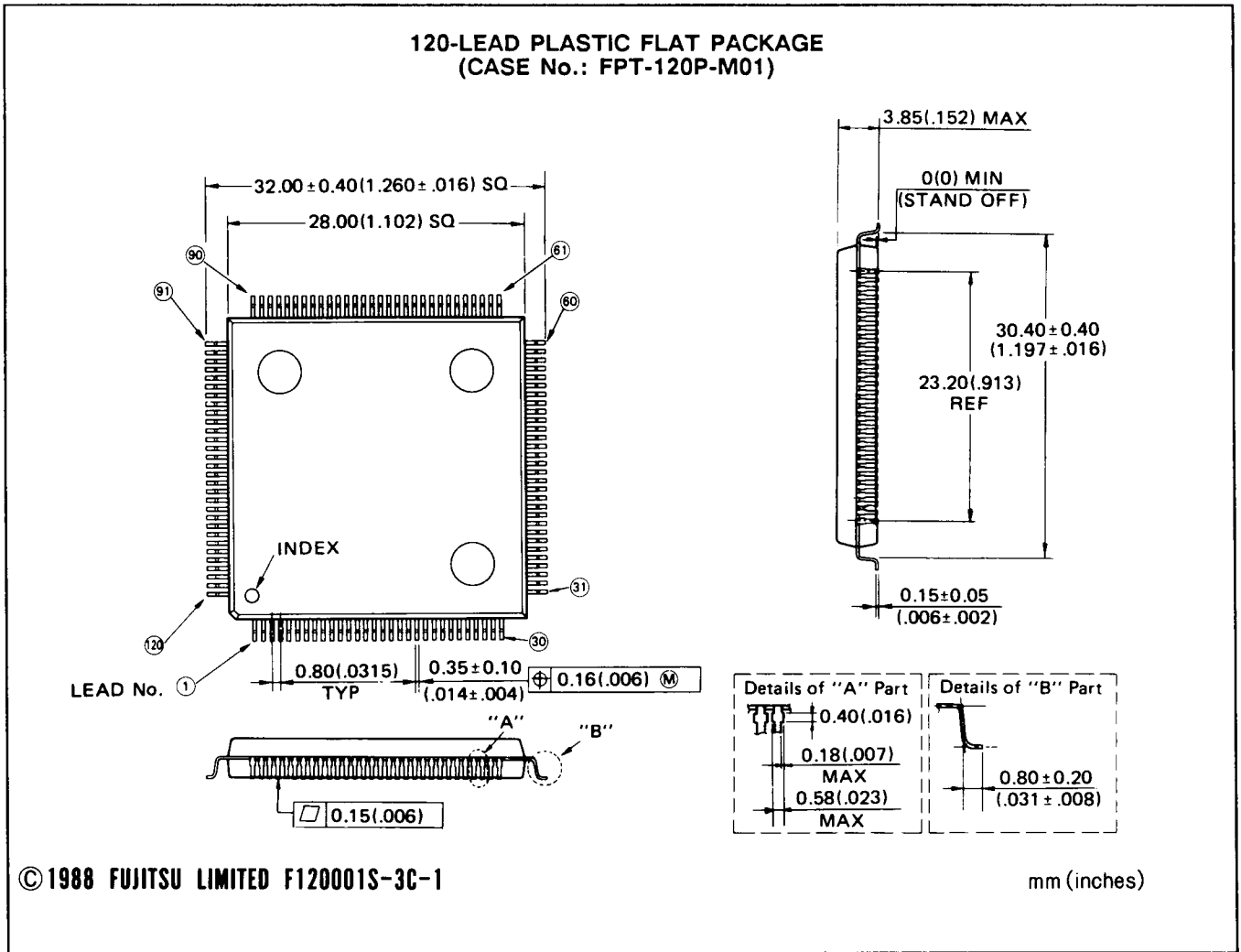
Clock and gate signals timing  $V_{CC}=5V\pm 10\%$ ,  $GND=0V$ ,  $0^{\circ}C \leq T_A \leq +70^{\circ}C$ ,  $C_L=150pf$

Parameter	Symbol	Min	Max	Unit
Clock "L" pulse width	tCKL	60		ns
Clock "H" pulse width	tCKH	60		ns
Clock cycle time	tCK	125		ns
Clock rising time	tR		100	ns
Clock falling time	tF		100	ns
Gate "H" pulse width	tGTH	50		ns
Gate "L" pulse width	tGTL	50		ns
Gate setup time to clock rising edge	tGTS	50		ns
Gate hold time from clock rising edge	tGTHD	50		ns
Output delay time from gate falling edge	tODTGT		120	ns
Output delay time from clock falling edge	tODTCK		150	ns



MB89396

# PACKAGE DIMENSIONS



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