TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 8-BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518128CPL/CSPL/CFL/CFWL/CFTL is a 1,048,578-bit CMOS pseudo static random access memory (PSRAM) organized as 131,072 words by 8 bits. It feature a one-transistor dynamic memory cell using CMOS peripheral circuitry to provide large capacity, high speed and low power. It uses a single 5 V ± 10% power supply. A $\overline{RFSH}$ input selects either auto or self refresh operation. This device family also features SRAM-like write functions whereby data is written to the memory cell rising edge of R/W signal, for easy interfacing to microprocessors. The TC518128CPL/CSPL/CFL/CFWL/CFTL meets the JEDEC CMOS SRAM pin-compatibility standard and is available in molded 32-pin standard 0.6-inch and 0.3-inch dual-inline plastic packages (DIP) and 0.45-inch and 0.525-inch small-outline plastic packages (SOP), and thin small-outline plastic package (TSOP).

FEATURES

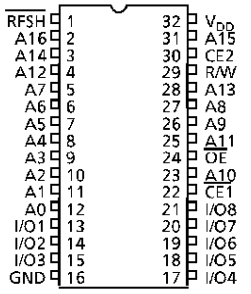
- Organized as 131,072 words by 8 bits (1,048,576 bits).
- Fast access time and low power dissipation.
- Single power supply voltage of 5 V ± 10%.

	TC518128C Family		
	-70	-80	-10
t_{CEA} $\overline{CE}$ Access Time	70 ns	80 ns	100 ns
t_{OEA} $\overline{OE}$ Access Time	25 ns	30 ns	40 ns
t_{RC} Cycle Time	115 ns	130 ns	160 ns
Power Dissipation	385 mW	330 mW	275 mW
Self Refresh Current	100 μA (L version) 50 μA (LL version)		

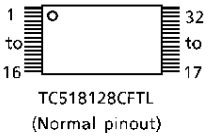
- Internal counter can be used for auto and self refresh operations.
- Internal timer can be used for self refresh operation.
- Auto refresh power down function.
- 512 refresh cycles per 8 ms.
- All inputs and outputs are TTL compatible.
- Pin compatible with 1M SRAM (JEDEC).
- Logic compatible with SRAM R/W pin.
- Packages:

DIP32-P-600-2.54 (CPL)	(Weight: 4.45 g typ)
SOP32-P-450-1.27 (CFL)	(Weight: 2.34 g typ)
DIP32-P-300-2.54 (CSPL)	(Weight: 0.86 g typ)
SOP32-P-525-1.27 (CFWL)	(Weight: 1.04 g typ)
TSOP I 32-P-0820-0.50 (CFTL)	(Weight: 0.32 g typ)

PIN ASSIGNMENT (TOP VIEW)

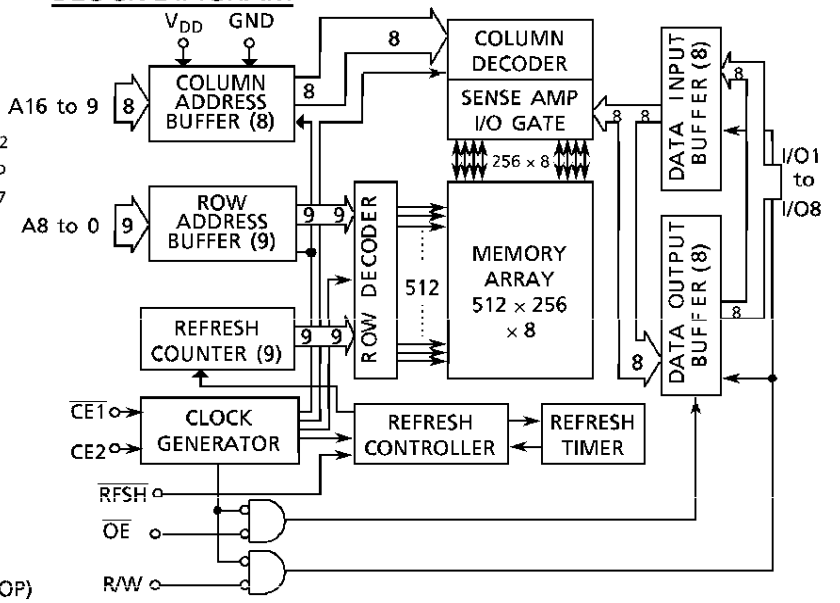


TC518128CPL/CFL/CSPL/CFWL



TC518128CFTL
(Normal pinout)

BLOCK DIAGRAM



PIN NAMES

A0 to A16	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable
I/O1 to I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	$\overline{RFSH}$	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

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TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 to A16	I/O1 to 8	CONDITION
L	H	L	H	×	××	OUT	Read
L	H	×	L	×	××	IN	Write
L	H	H	H	×	××	HZ	CE Only Refresh
H	×	×	×	L	×	HZ	Auto/Self Refresh
×	L	×	×	L	×	HZ	Auto/Self Refresh
H	×	×	×	H	×	HZ	Stand by
×	L	×	×	H	×	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5 V to V_{IH} min)
L ··· Low Level Input (V_{IN} = V_{IL} max to − 1.0 V)
× ··· Don't care
×× ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address are "IN", and at the other condition, the address are "×"
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT	NOTE
V_{IN}	Input Voltage	− 1.0 to 7.0	V	1
V_{OUT}	Output Voltage	− 1.0 to 7.0	V	
V_{DD}	Power Supply Voltage	− 1.0 to 7.0	V	
T_{OPR}	Operating Temperature	0 to 70	°C	
T_{STG}	Storage Temperature	− 55 to 150	°C	
T_{SOLDER}	Soldering Temperature (10 s)	260	°C	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	− 1.0	−	0.8	V	

DC CHARACTERISTICS (V_{DD} = 5 V ± 10%, Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	NOTE
I_{DDO}	Operating Current (Average Power Supply) $\overline{CE1}$, CE2, Address Cycling: t_{RC} = t_{RC} min	70 ns version	–	50	70	mA	3, 4
		80 ns version	–	40	60		
		100 ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, $\overline{RFSH}$ = V_{IH}		–	–	1	mA	
I_{DDS2}	Standby Current, $\overline{CE1}$ = V_{DD} − 0.2 V or CE2 = 0.2 V $\overline{RFSH}$ = V_{DD} − 0.2 V	L version	–	50	100	μA	
		LL version	–	35	50		
I_{DDF1}	Self Refresh Current (Average) $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, $\overline{RFSH}$ = V_{IL}		–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE1}$ = V_{DD} − 0.2 V or CE2 = 0.2 V, $\overline{RFSH}$ = 0.2 V	L version	–	50	100	μA	
		LL version	–	35	50		
I_{DDF3}	Auto Refresh Current (Average) ($\overline{RFSH}$ Cycling: t_{FC} = t_{FC} min)		–	–	2	mA	
I_{DDF4}	CE Only Refresh Current (Average) ($\overline{CE1}$, CE2, Address Cycling: t_{RC} = t_{RC} min)	70 ns version	–	50	70	mA	3
		80 ns version	–	40	60		
		100 ns version	–	35	50		
$I_{I(L)}$	Input Leakage Current 0 V ≦ V_{IN} ≦ V_{DD}, All Other Inputs Not Under Test = 0 V		− 10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0 V ≦ V_{OUT} ≦ V_{DD}		− 10	–	10	μA	
V_{OH}	Output High Level I_{OH} = − 1 mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 2.1 mA		–	–	0.4	V	

Note: For I_{DDS1} and I_{DDF1} with $\overline{CE1}$ = V_{IH} (CE2 = V_{IL}), these specification limits are guaranteed for the condition CE2 = V_{IH} or CE2 = V_{IL} ($\overline{CE1}$ = V_{IH} or $\overline{CE1}$ = V_{IL}). For I_{DDS2} and I_{DDF2} with $\overline{CE1}$ ≧ V_{DD} − 0.2 V (CE2 ≦ 0.2 V), these specification are guaranteed for the condition CE2 ≧ V_{DD} − 0.2 V or CE2 ≦ 0.2 V ($\overline{CE1}$ ≧ V_{DD} − 0.2 V or $\overline{CE1}$ ≦ 0.2 V).

CAPACITANCE (V_{DD} = 5 V, f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 to A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{I0}	Input/Output Capacitance	–	7	pF

Note: This parameter is periodically sampled and is not 100% tested.

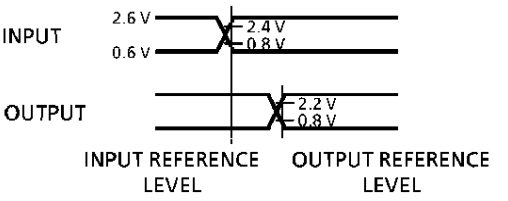
AC CHARACTERISTICS (V_{DD} = 5 V ± 10%, Ta = 0° to 70°C) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	–	130	–	160	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	160	–	180	–	220	–	ns	
t_{CE}	CE Pulse Width	70	10,000	80	10,000	100	10,000	ns	13
t_P	CE Precharge Time	35	–	40	–	50	–	ns	
t_{CEA}	CE Access Time	–	70	–	80	–	100	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	–	40	ns	
t_{CLZ}	CE to Output in Low-Z	20	–	20	–	20	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Setup Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Setup Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	20	–	25	–	30	–	ns	
t_{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	20	10,000	25	10,000	30	10,000	ns	
t_{DSW}	Data Setup Time from R/W	15	–	20	–	25	–	ns	10
t_{DSC}	Data Setup Time from CE	15	–	20	–	25	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from CE	0	–	0	–	0	–	ns	10
t_{ASC}	Address Setup Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	115	–	130	–	160	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	35	–	40	–	50	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	160	–	190	–	ns	12
t_{REF}	Refresh Period (512 cycles, A0 to A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t_{CES}	CE2 Low Setup Time	5	–	5	–	5	–	ns	14
t_{CEH}	CE2 Low Hold Time	5	–	5	–	5	–	ns	14

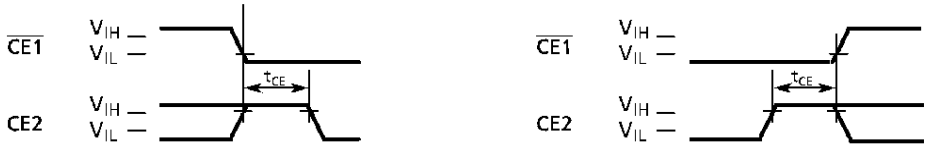
Notes:

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depend on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100 μs with $\overline{CE1}$ High or CE2 Low is required after power-up before proper device operation is achieved.
6) AC measurements assume t_T = 5 ns.
7) Timing reference levels

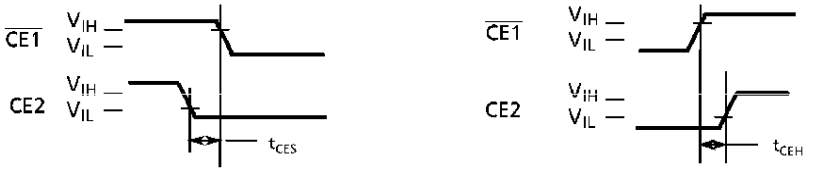
Input Level	:	V_{IH} = 2.6 V
		V_{IL} = 0.6 V
Input Reference Level	:	V_{IH} = 2.4 V
		V_{IL} = 0.8 V
Output Reference Level:		V_{OH} = 2.2 V
		V_{OL} = 0.8 V



8) Measured with a load equivalent to 1 TTL load and 100 pF.
9) Parameters t_{CHZ}, t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, input data is latched at the earlier of the R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore, input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched on the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore, all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operations—auto refresh and self refresh—are defined by the $\overline{RFSH}$ pulse width under the condition $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq t_{FAP}$ (max)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq t_{FAS}$ (min)
    The timing parameter (t_{FRS}) must be observed for proper device operation in accordance with the following conditions.
    - After self refresh
    - When $\overline{RFSH}$ = "L" after power-up
13) The timings t_{CE} (min) and t_{CE} (max) must be observed for proper device operation as follows.

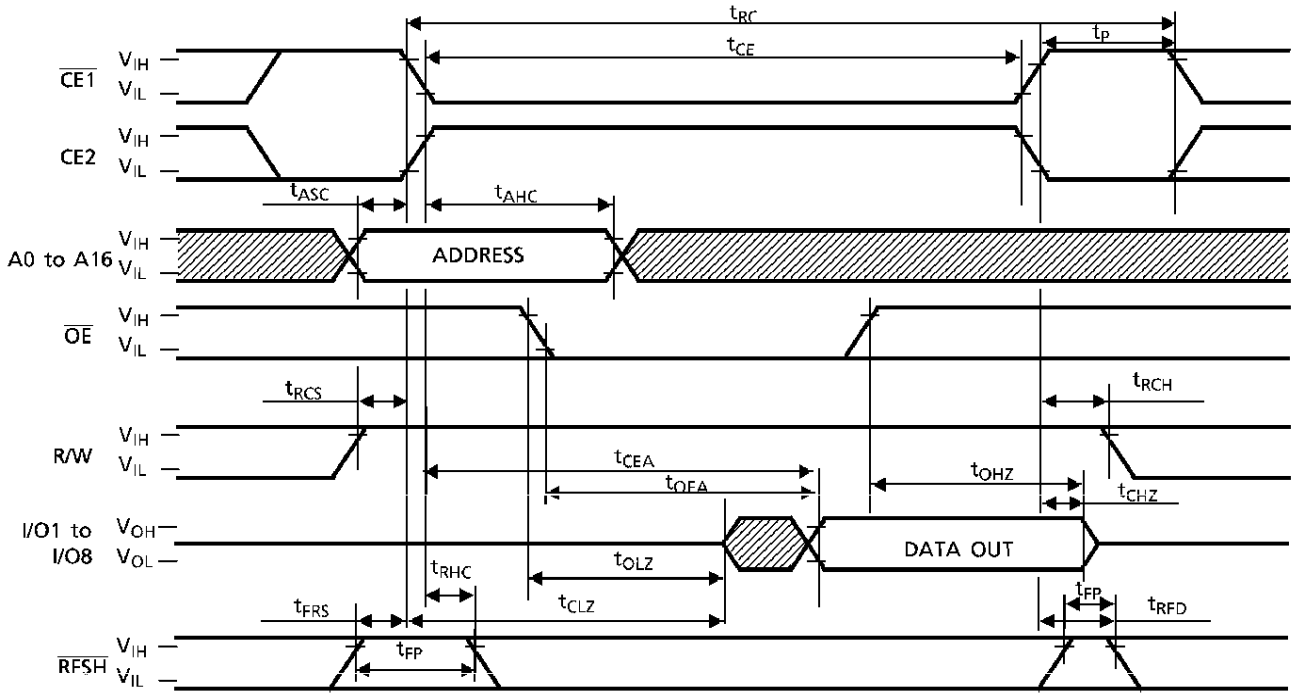


14) The timings t_{CES} (min) and t_{CEH} (min) must be observed for using $\overline{CE1}$ and CE2 on the same clock as follows.

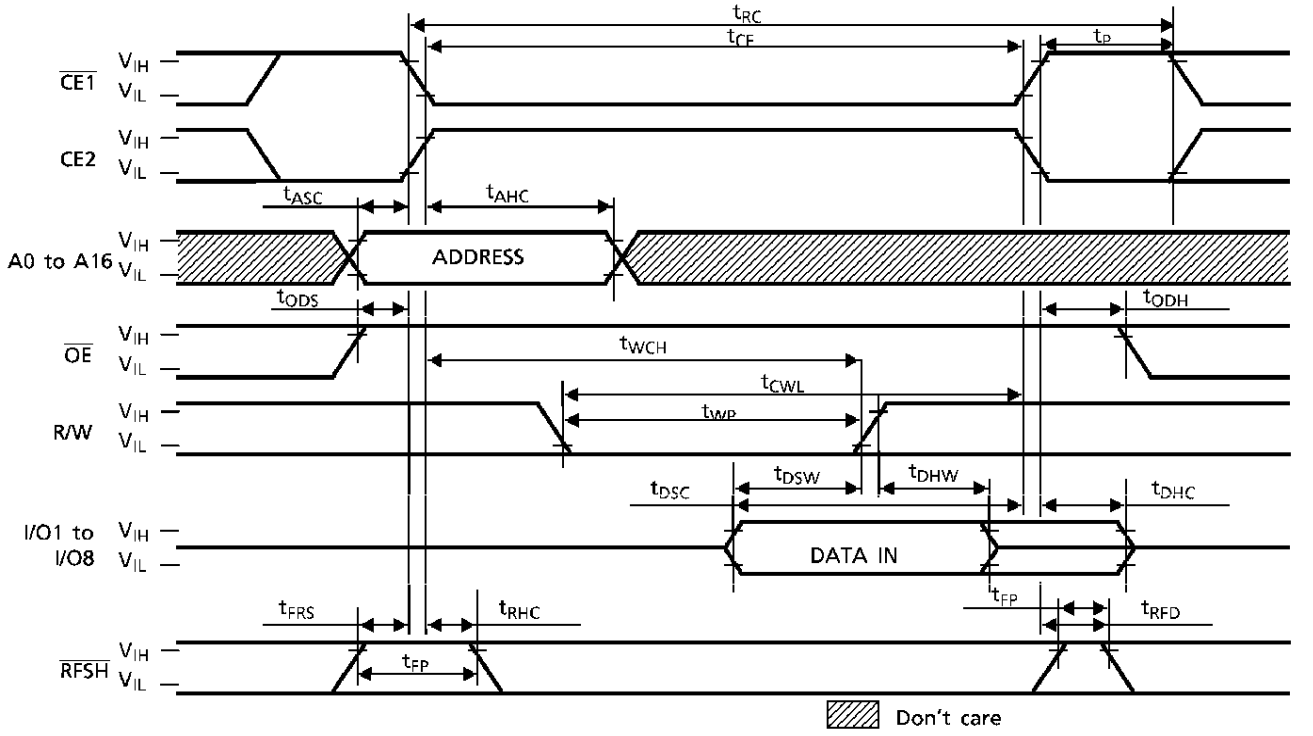


TIMING DIAGRAMS

READ CYCLE

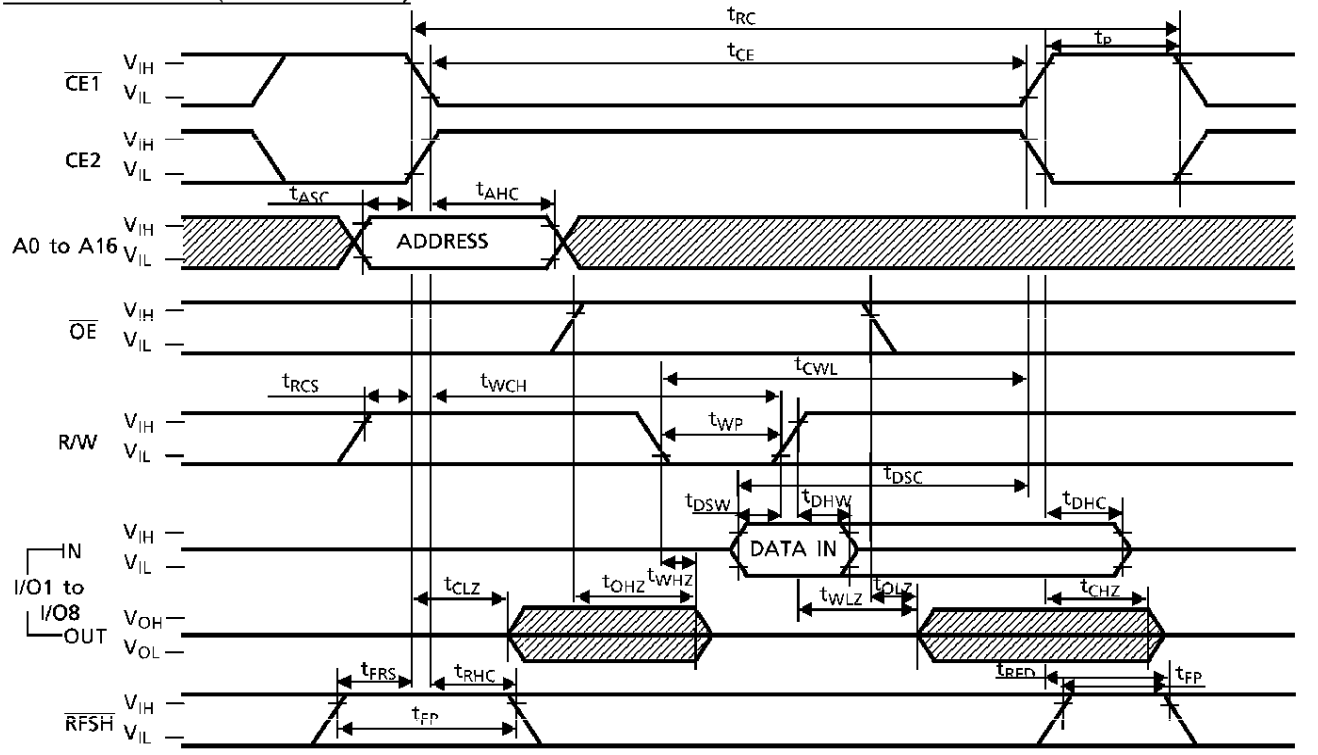


WRITE CYCLE 1 ($\overline{OE}$ HIGH)

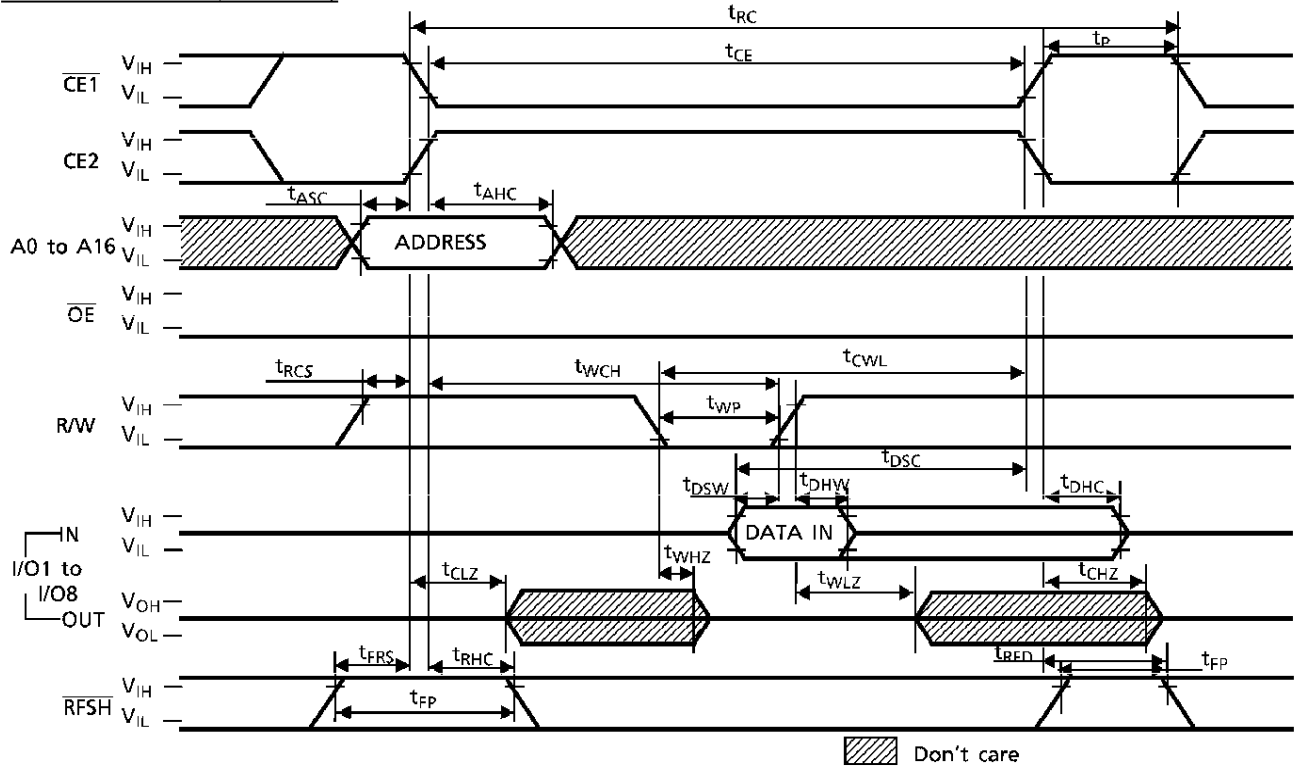


Note: The device can be operated by cycling the $\overline{CE1}$ (or CE2) pin only, provided that CE2 (or $\overline{CE1}$) is set to the V_{IH} (or V_{IL}) level.

WRITE CYCLE 2 ($\overline{OE}$ CLOCKED)

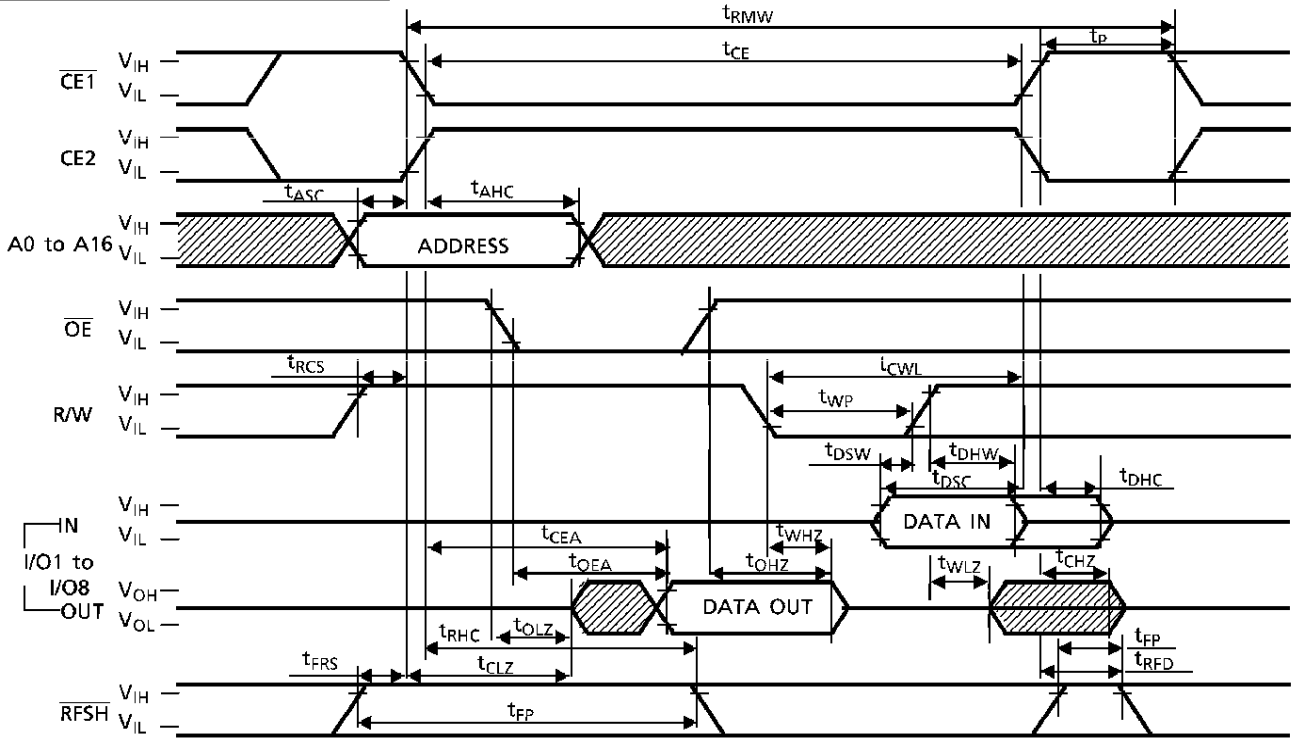


WRITE CYCLE 3 ($\overline{OE}$ LOW)

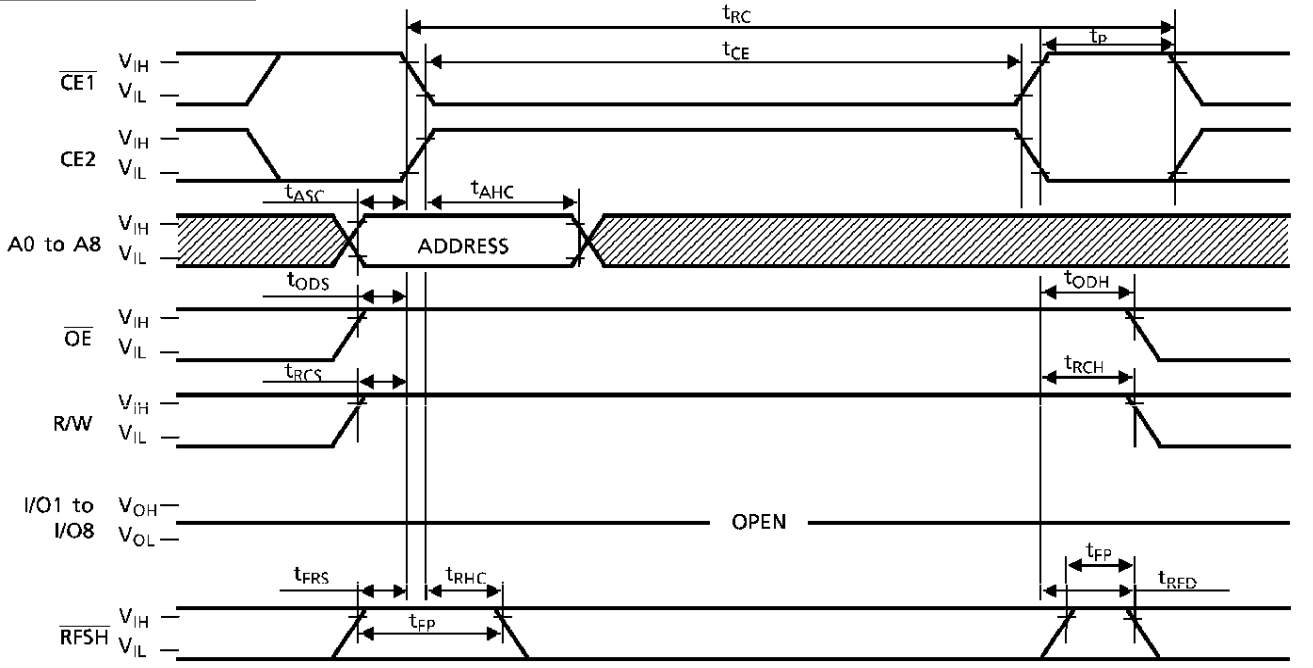


Note: The device can be operated by cycling the $\overline{CE1}$ (or CE2) pin only, provided that CE2 (or $\overline{CE1}$) is set to the V_{IH} (or V_{IL}) level.

READ-MODIFY-WRITE CYCLE



CE-ONLY REFRESH

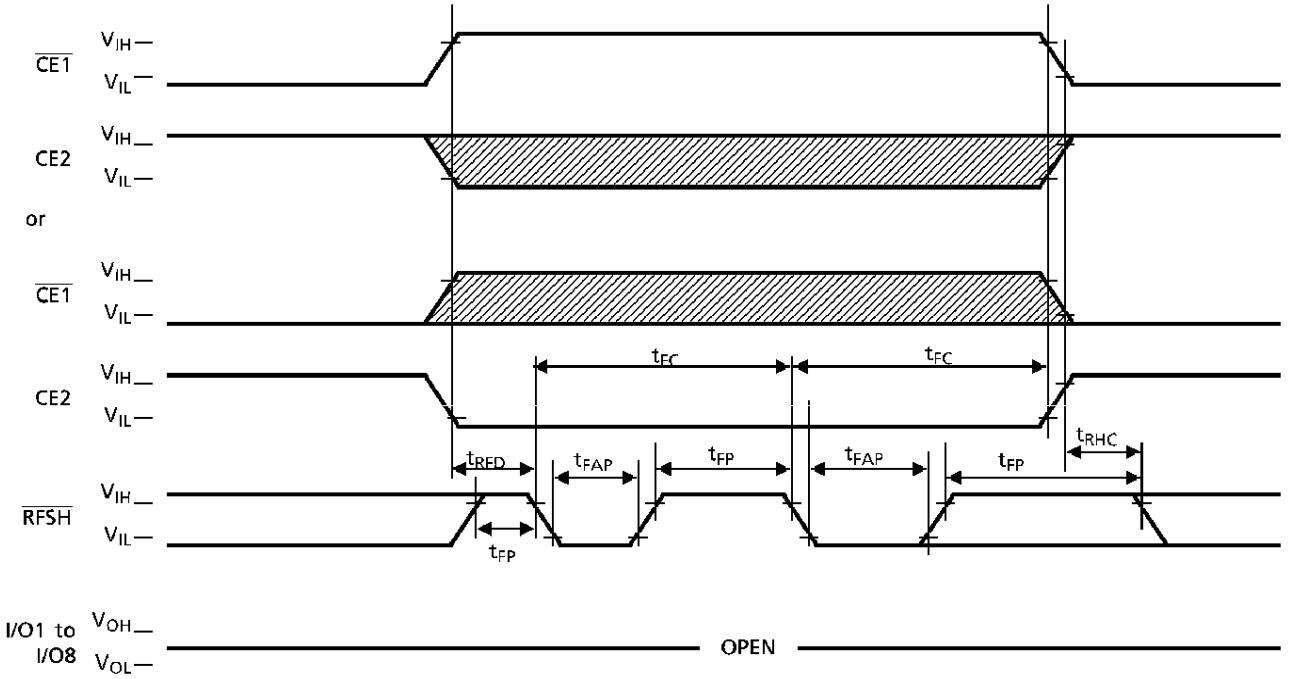


Note: A9 to A16 = Don't care.

Don't care

Note: The device can be operated by cycling the $\overline{CE1}$ (or CE2) pin only, provided that CE2 (or $\overline{CE1}$) is set to the V_{IH} (or V_{IL}) level.

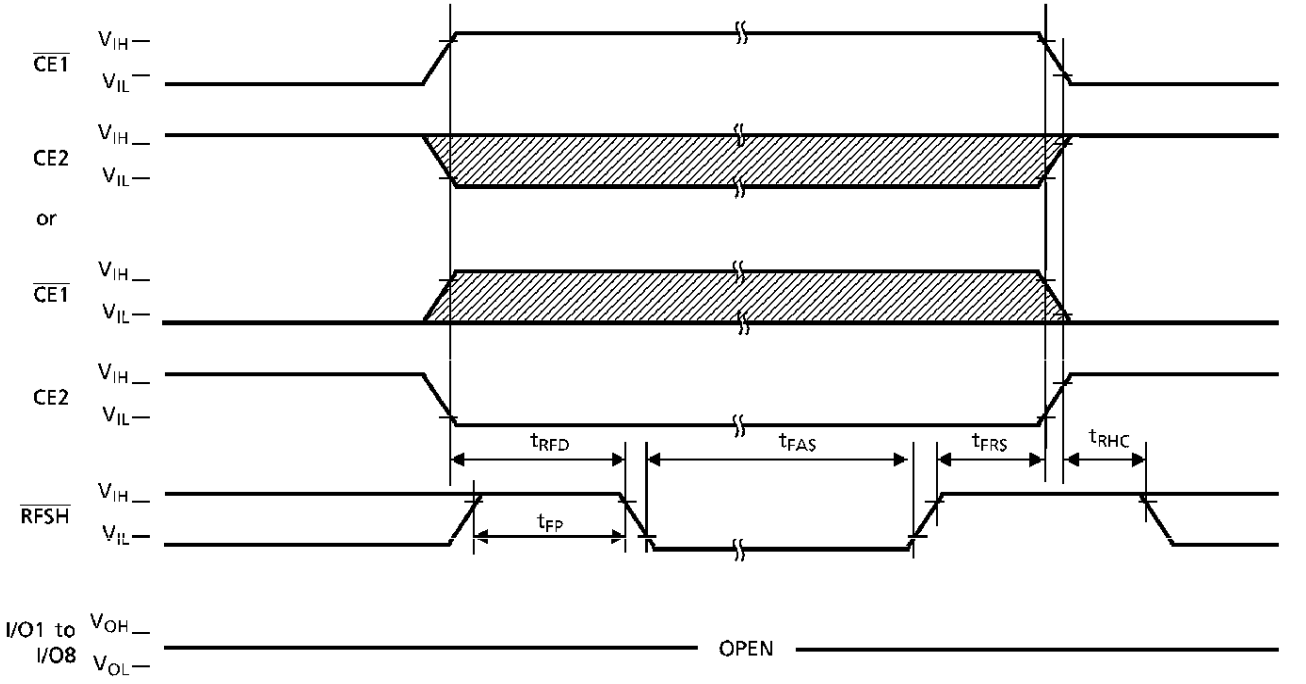
$\overline{\text{RFSH}}$ AUTO REFRESH



Note: $\overline{\text{OE}}$, R/W, A0 to A16 = Don't care.

Don't care

SELF REFRESH

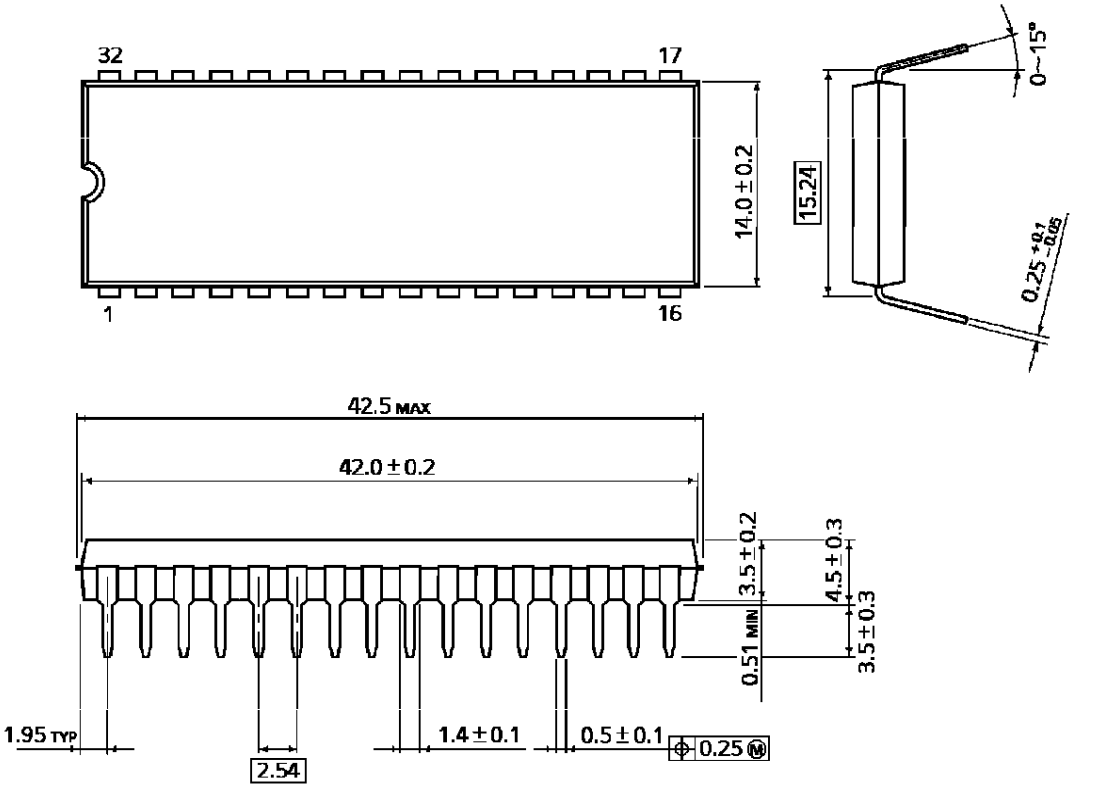


Note: $\overline{\text{OE}}$, R/W, A0 to A16 = Don't care.

Don't care

PACKAGE DIMENSIONS (DIP32-P-600-2.54)

Units in mm

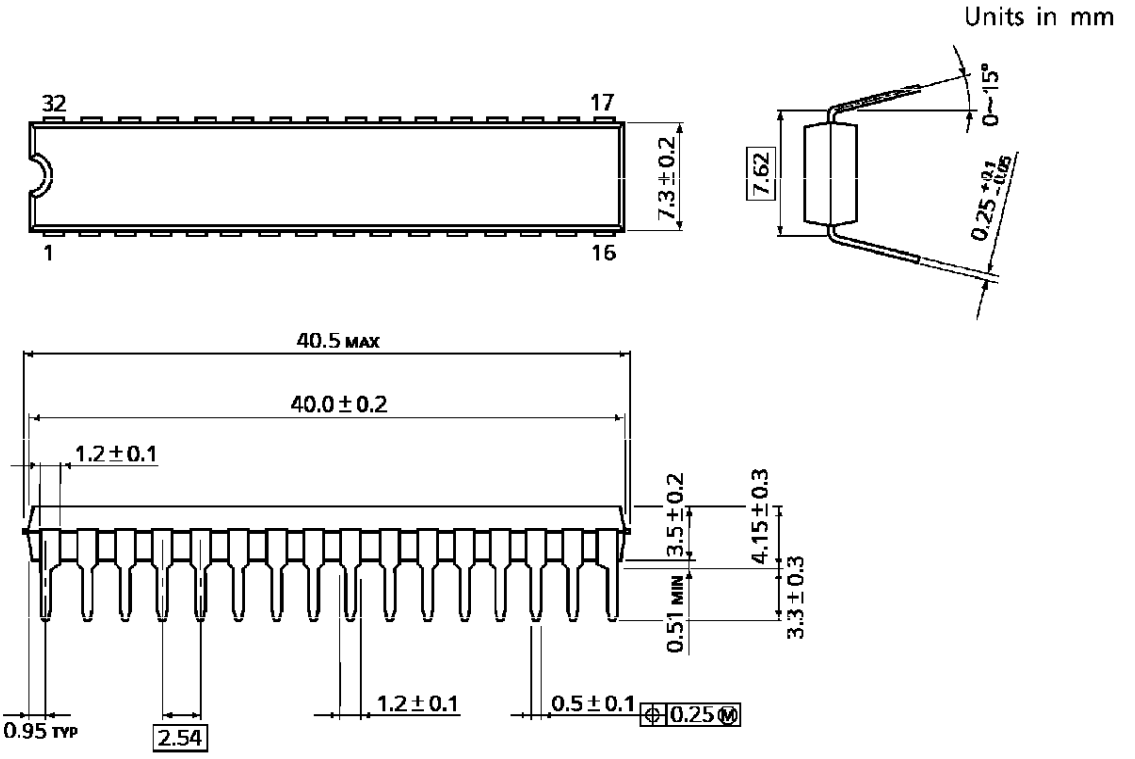


Weight: 4.45 g (typ)

TC518128CPL-70, -70L
TC518128CPL-80, -80L
TC518128CPL-10, -10L

PACKAGE DIMENSIONS (DIP32-P-300-2.54)

Units in mm

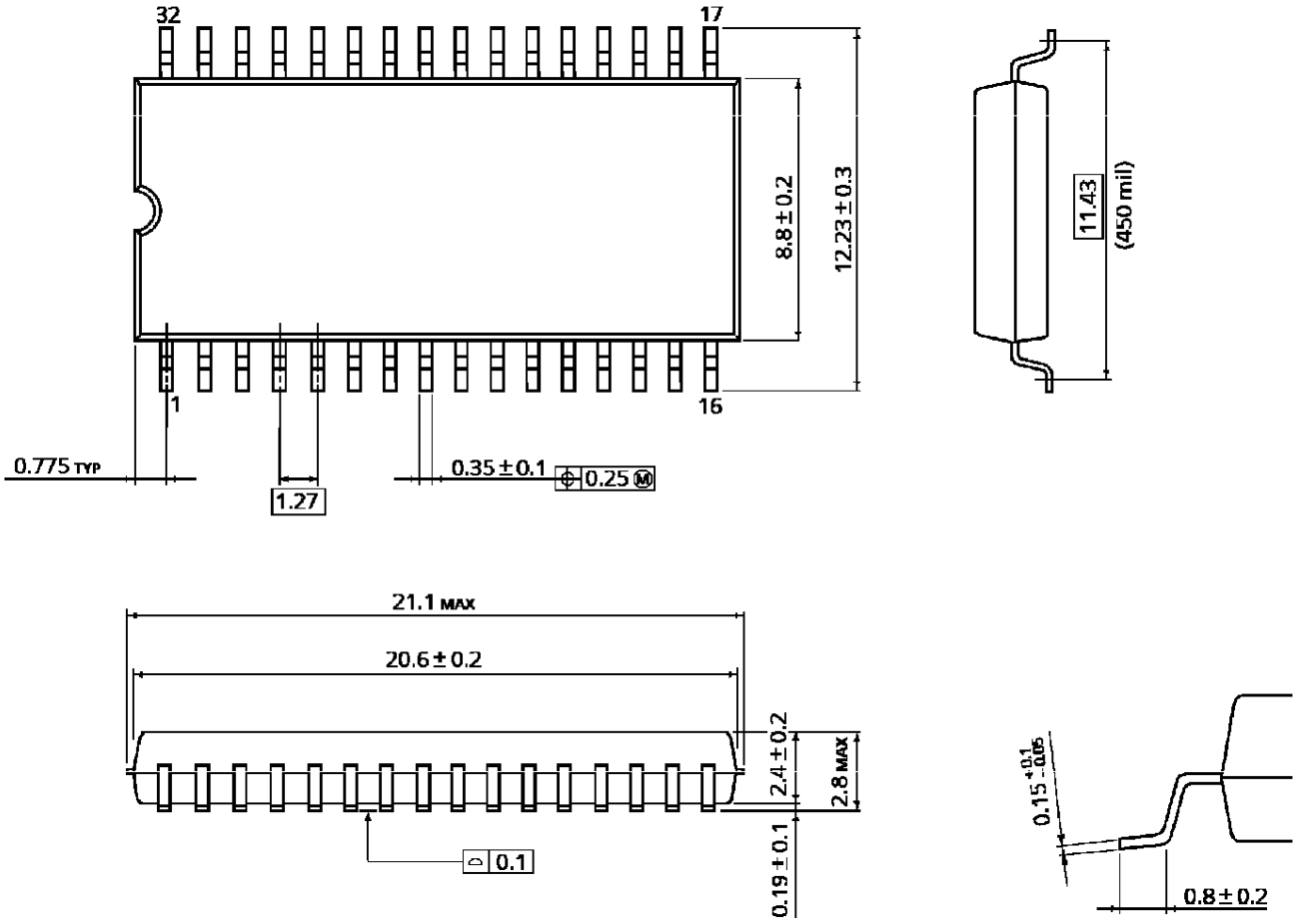


Weight: 2.34 g (typ)

TC518128CSPL-70, -70L
TC518128CSPL-80, -80L
TC518128CSPL-10, -10L

PACKAGE DIMENSIONS (SOP32-P-450-1.27)

Units in mm

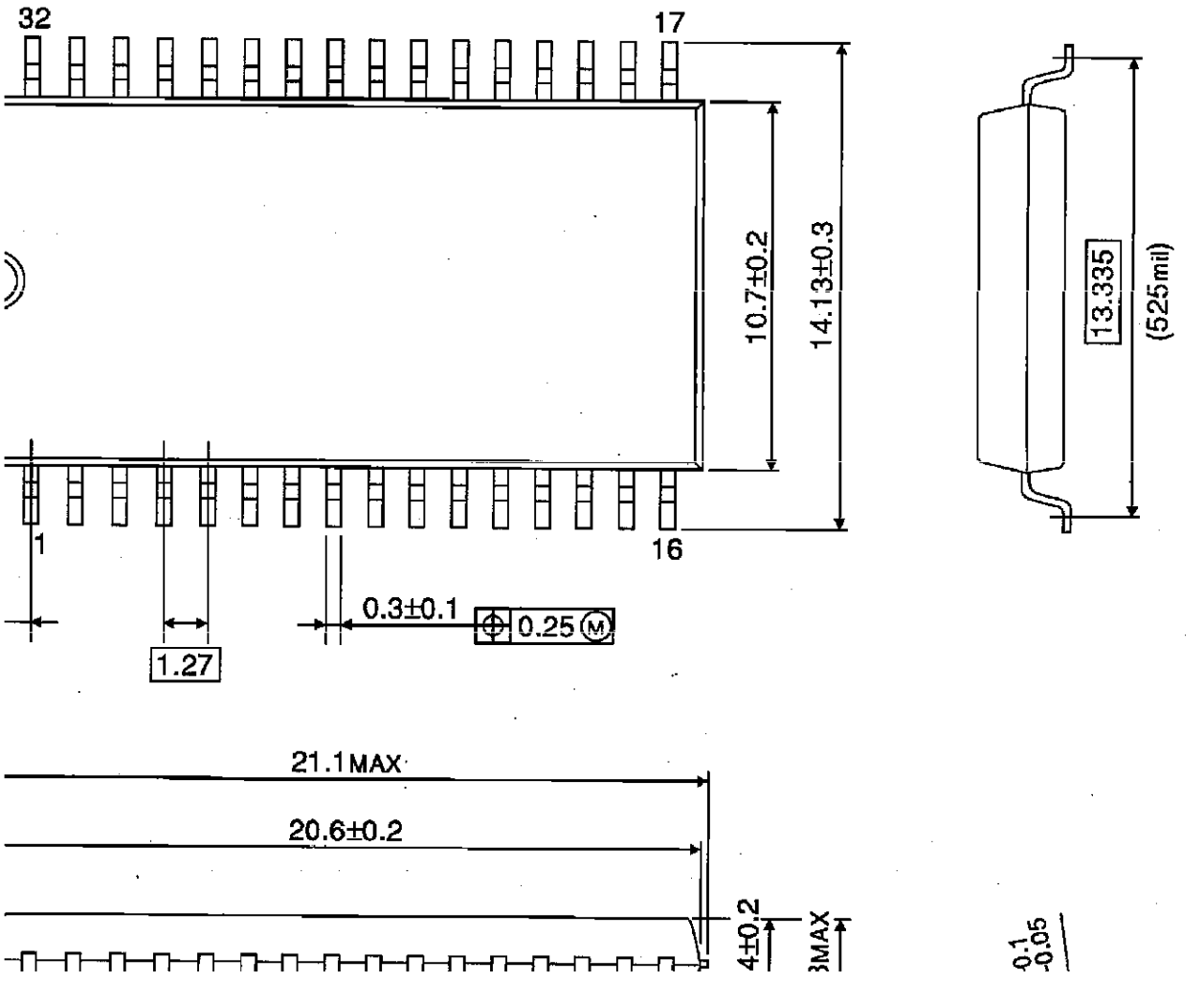


Weight: 0.86 g (typ)

TC518128CFL-70, -70L
TC518128CFL-80, -80L
TC518128CFL-10, -10L

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

Units in mm

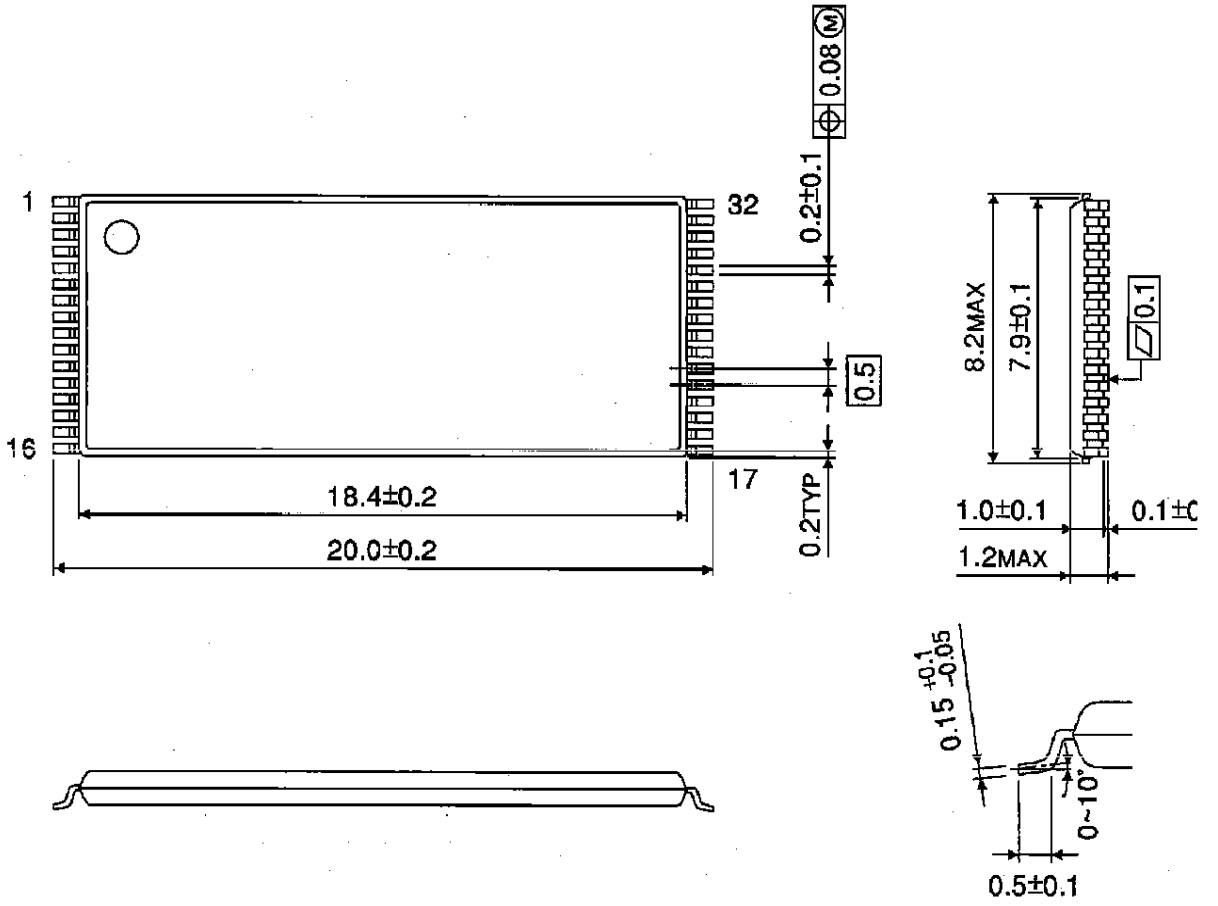


Weight: 1.04 g (typ)

TC518128CFWL-70, -70L
TC518128CFWL-80, -80L
TC518128CFWL-10, -10L

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50)

Units in mm



Weight: 0.32 g (typ)

TC518128CFTL-70, -70L
TC518128CFTL-80, -80L
TC518128CFTL-10, -10L